# Xicor ®

**512K**     **X28LC512/X28LC513**     **64K x 8 Bit**

## 3.3 Volt, Byte Alterable E$^2$PROM

### FEATURES

- **Low V$_{CC}$ Operation: V$_{CC}$ = 3.3V ±10%**
- **Access Time: 150ns**
- **Simple Byte and Page Write**
    - **—Self-Timed**
        - **—No Erase Before Write**
        - **—No Complex Programming Algorithms**
        - **—No Overerase Problem**
- **Low Power CMOS:**
    - **—Active: 25mA**
    - **—Standby: 150µA**
- **Software Data Protection**
    - **—Protects Data Against System Level Inadvertant Writes**
- **High Speed Page Write Capability**
- **Highly Reliable Direct Write™ Cell**
    - **—Endurance: 10,000 Write Cycles**
    - **—Data Retention: 100 Years**
- **Early End of Write Detection**
    - **—$\overline{\text{DATA}}$ Polling**
    - **—Toggle Bit Polling**
- **Two PLCC and LCC Pinouts**
    - **—X28LC512**
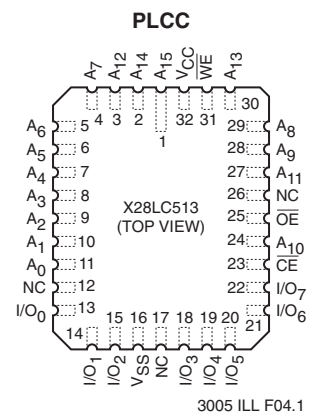        - **—X28LC010 E$^2$PROM Pin Compatible**
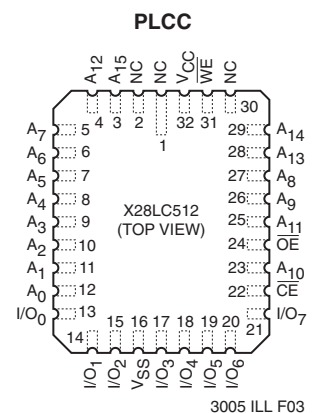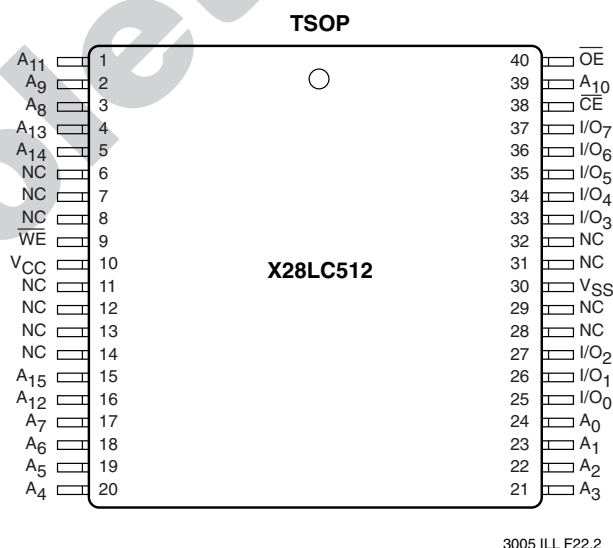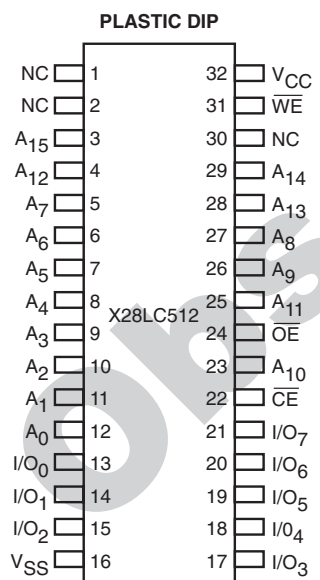    - **—X28LC513**
        - **—Compatible with Lower Density E$^2$PROMs**

### DESCRIPTION

The X28LC512/513 is a low-power 64K x 8 E$^2$PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. The X28LC512/513 features the JEDEC approved pinout for bytewide memories, compatible with industry standard EPROMS.

The X28LC512/513 supports a 128-byte page write operation, effectively providing a 39µs/byte write cycle and enabling the entire memory to be written in less than 2.5 seconds. The X28LC512/513 also features $\overline{\text{DATA}}$ Polling and Toggle Bit Polling, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28LC512/513 supports the Software Data Protection option.

### PIN CONFIGURATIONS



PLASTIC DIP

3005 ILL F02.1



TSOP

X28LC512

3005 ILL F22.2



PLCC

X28LC512 (TOP VIEW)

3005 ILL F03



PLCC

X28LC513 (TOP VIEW)

3005 ILL F04.1

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Characteristics subject to change without notice

# X28LC512/X28LC513

## PIN DESCRIPTIONS

### Addresses (A$_0$–A$_{15}$)

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ($\overline{\text{CE}}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{\text{CE}}$ is HIGH, power consumption is reduced.

### Output Enable ($\overline{\text{OE}}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

### Data In/Data Out (I/O$_0$–I/O$_7$)

Data is written to or read from the X28LC512/513 through the I/O pins.

### Write Enable ($\overline{\text{WE}}$)

The Write Enable input controls the writing of data to the X28LC512/513.

## PIN NAMES

| Symbol | Description |
|--------|-------------|
| A$_0$–A$_{15}$ | Address Inputs |
| I/O$_0$–I/O$_7$ | Data Input/Output |
| $\overline{\text{WE}}$ | Write Enable |
| $\overline{\text{CE}}$ | Chip Enable |
| $\overline{\text{OE}}$ | Output Enable |
| V$_{CC}$ | 3.3V $\pm$ 10% |
| V$_{SS}$ | Ground |
| NC | No Connect |

3005 PGM T01

## FUNCTIONAL DIAGRAM



3005 ILL F01

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# X28LC512/X28LC513

## DEVICE OPERATION

### Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

### Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28LC512/513 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

### Page Write Operation

The page write feature of the X28LC512/513 allows the entire memory to be written in 2.5 seconds. Page write allows two to one hundred twenty-eight bytes of data to be consecutively written to the X28LC512/513 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address ($A_7$ through $A_{15}$) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twenty-seven bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation.

Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

### Write Operation Status Bits

The X28LC512/513 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

**Figure 1.  Status Bit Assignment**
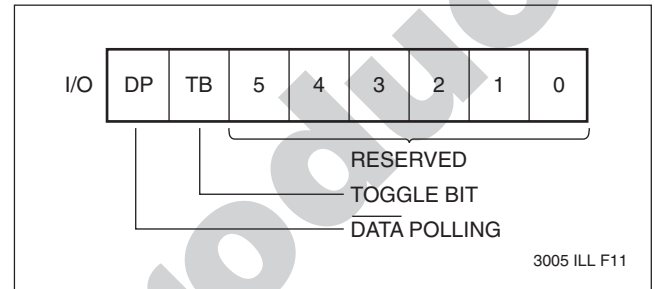


### $\overline{DATA}$ **Polling (I/O$_7$)**

The X28LC512/513 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28LC512/513, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O$_7$ (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O$_7$ will reflect true data.

### Toggle Bit (I/O$_6$)

The X28LC512/513 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle, I/O$_6$ will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

**$\overline{\text{DATA}}$ Polling I/O$_7$**
**Figure 2a. $\overline{\text{DATA}}$ Polling Bus Sequence**



3005 ILL F12

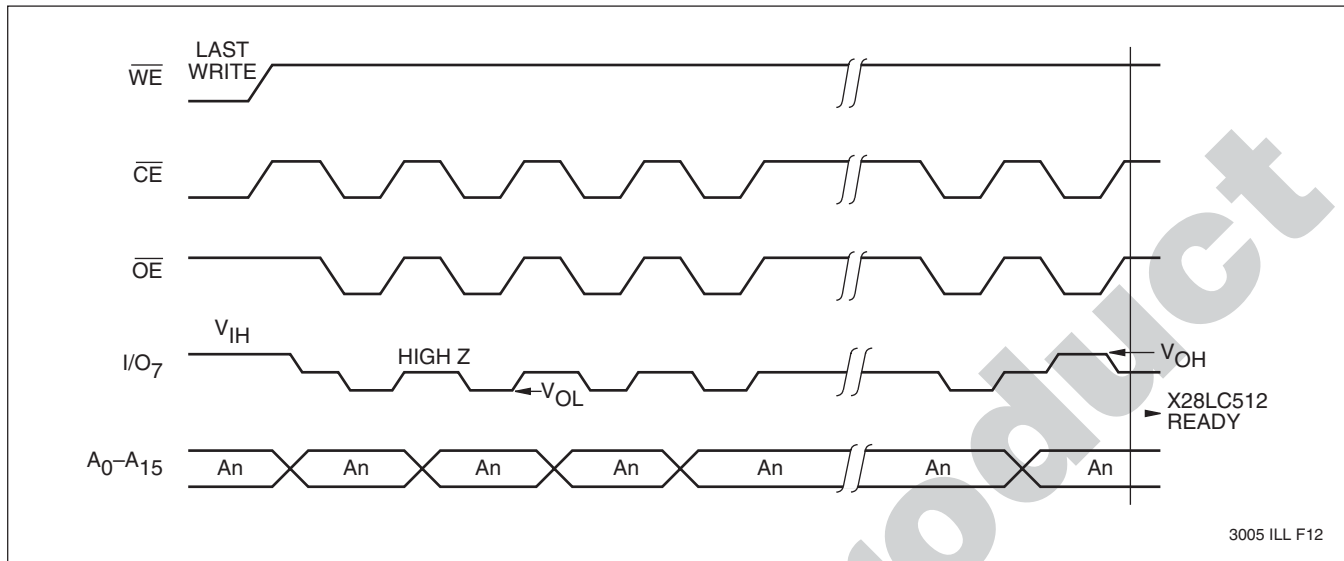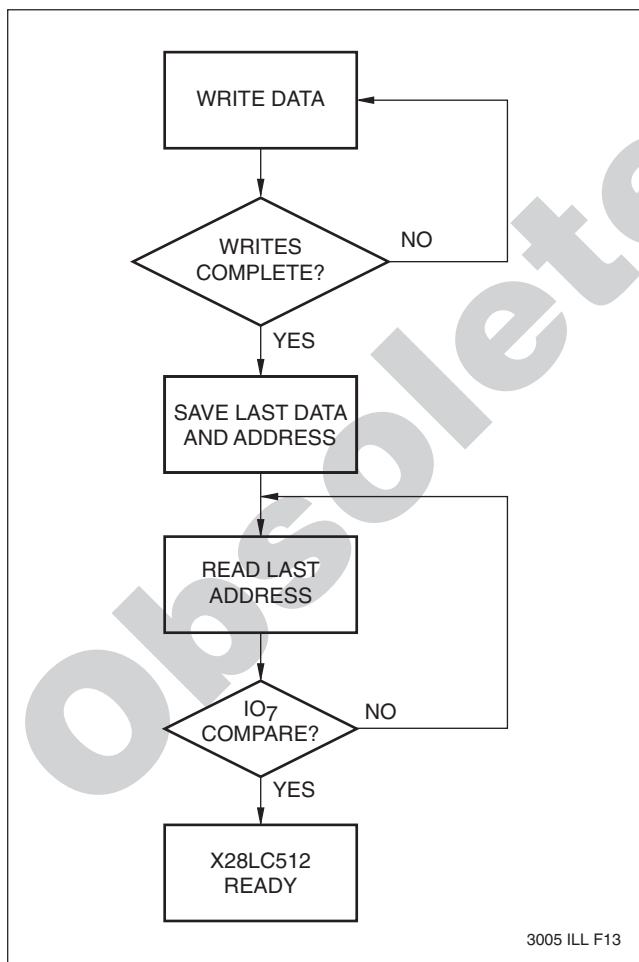**Figure 2b. $\overline{\text{DATA}}$ Polling Software Flow**



3005 ILL F13

$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the X28LC512/513. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

**The Toggle Bit I/O$_6$**
**Figure 3a. Toggle Bit Bus Sequence**



* Beginning and ending state of I/O$_6$ will vary.

3005 ILL F14
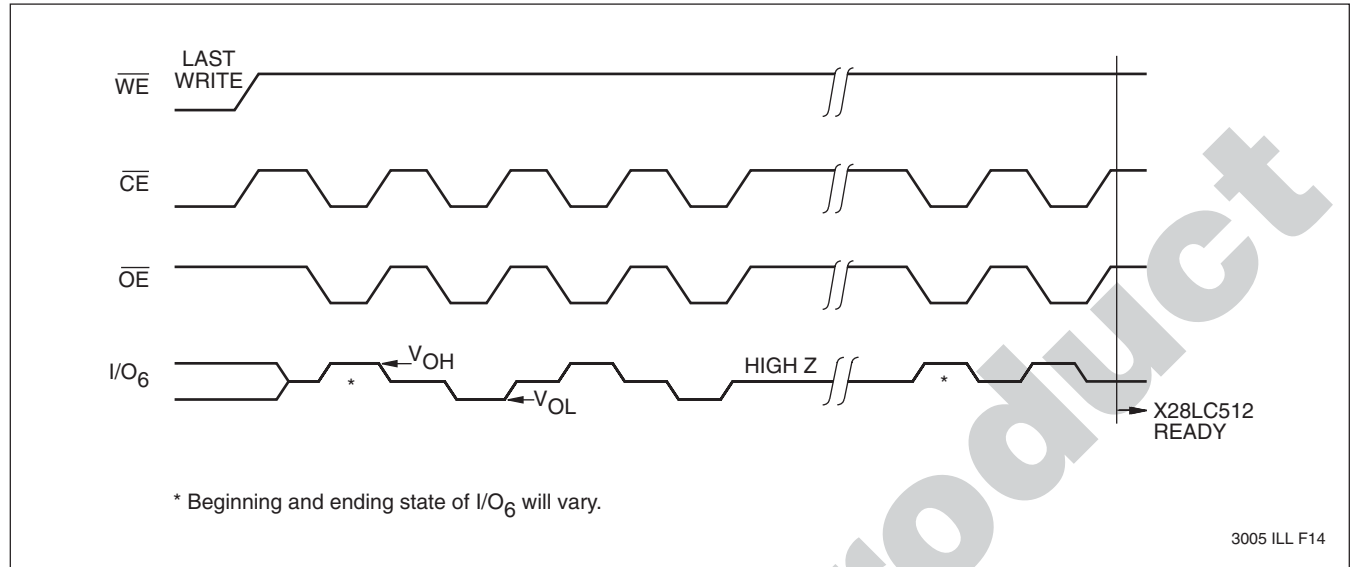
**Figure 3b.  Toggle Bit Software Flow**



3005 ILL F15
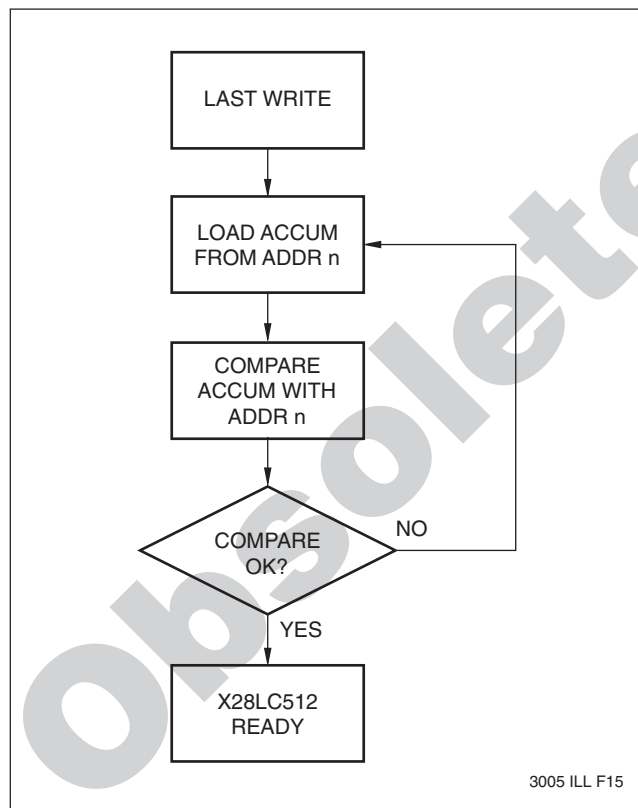
The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{\text{DATA}}$ Polling. This can be especially helpful in an array comprised of multiple X28LC512/513 memories that is frequently updated. Toggle Bit Polling can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for polling the Toggle Bit.

## HARDWARE DATA PROTECTION

The X28LC512/513 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse typically less than 10ns will not initiate a write cycle.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity. Write cycle timing specifications must be observed concurrently.

## SOFTWARE DATA PROTECTION

The X28LC512/513 offers a software controlled data protection feature. The X28LC512/513 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once $V_{CC}$ was stable.

The X28LC512/513 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28LC512/513 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device. Note: The data in the three-byte enable sequence is not written to the memory array.

## SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to one hundred twenty-eight bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

**Software Data Protection**
**Figure 4a. Timing Sequence—Software Data Protect Enable Sequence followed by Byte or Page Write**



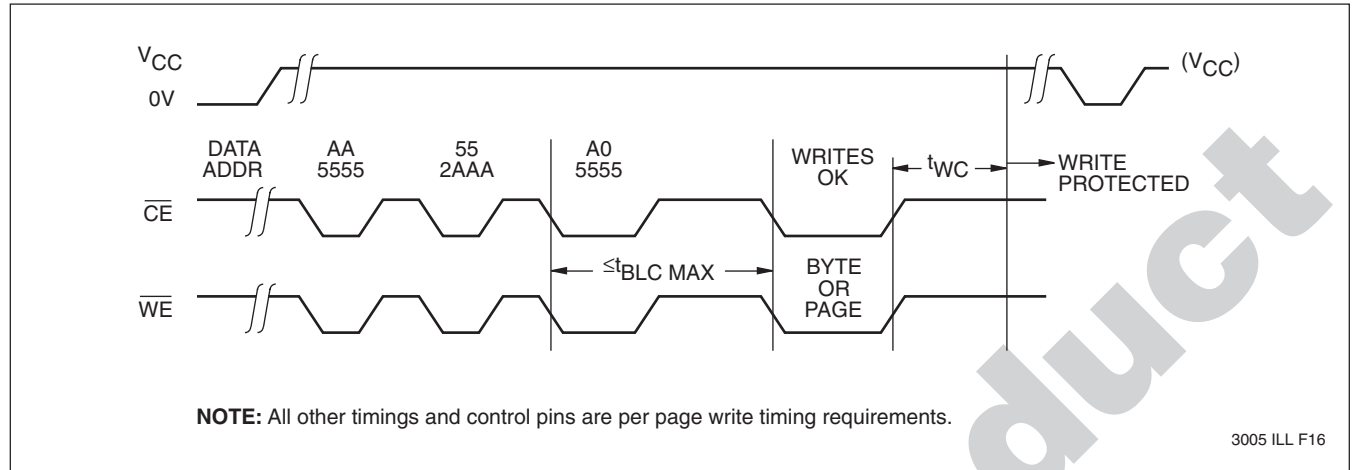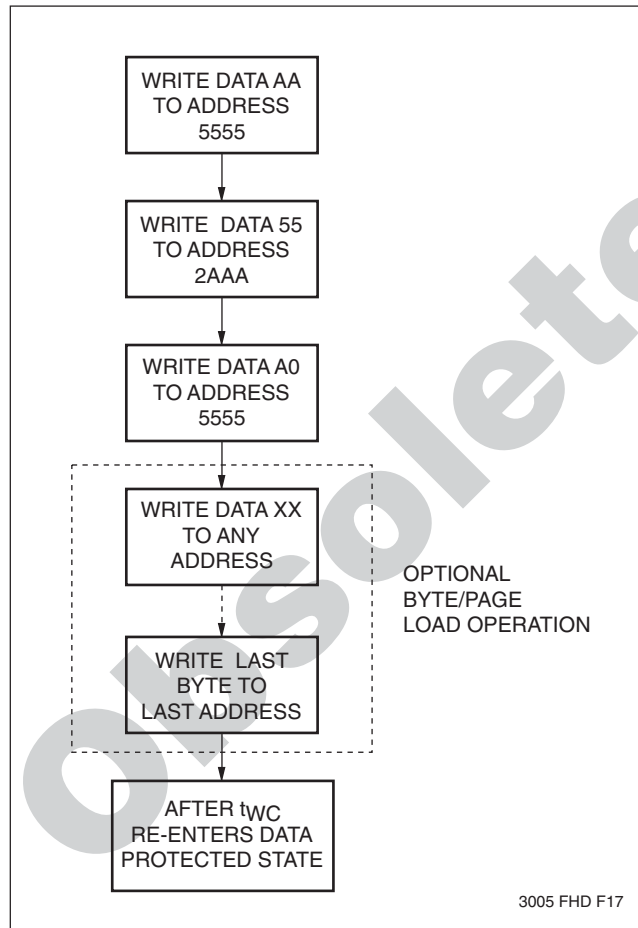**NOTE:** All other timings and control pins are per page write timing requirements.

3005 ILL F16

**Figure 4b.  Write Sequence for Software Data
Protection**



3005 FHD F17

Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28LC512/513 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28LC512/513 will be write protected during power-down and after any subsequent power-up. The state of $A_{15}$ while executing the algorithm is don't care.

*Note:  Once initiated, the sequence of write operations should not be interrupted.*

**Resetting Software Data Protection**
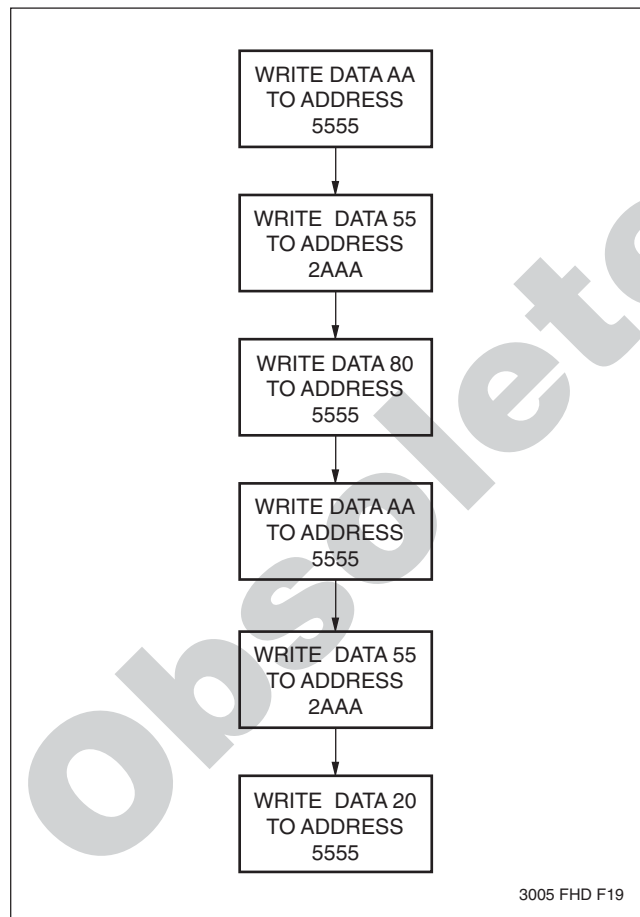**Figure 5a. Reset Software Data Protection Timing Sequence**



NOTE: All other timings and control pins are per page write timing requirements.

3005 ILL F18
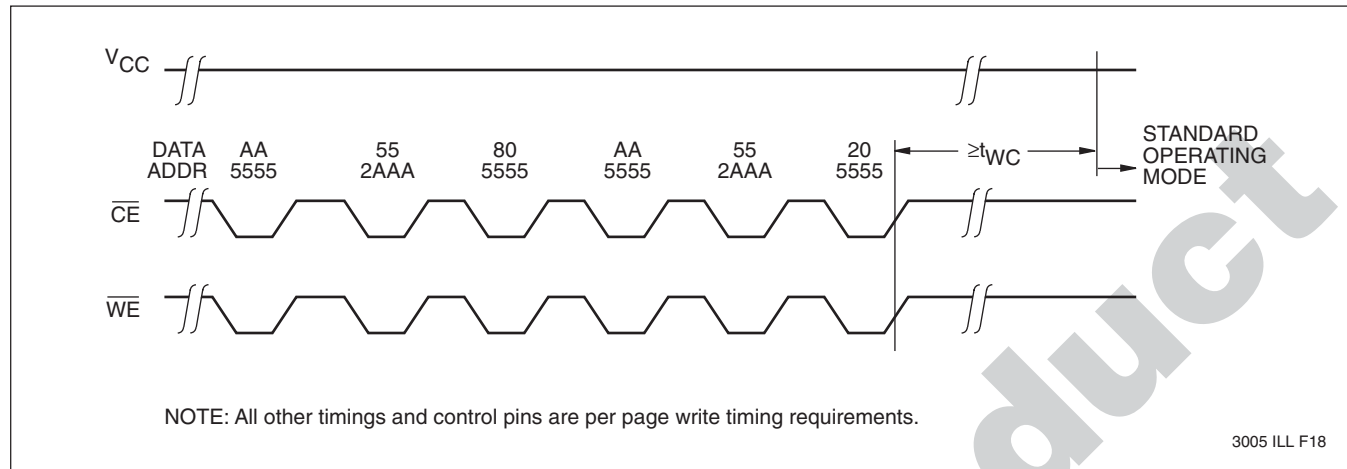
**Figure 5b.  Software Sequence to Deactivate Software Data Protection**



WRITE DATA AA TO ADDRESS 5555

WRITE  DATA 55 TO ADDRESS 2AAA

WRITE DATA 80 TO ADDRESS 5555

WRITE DATA AA TO ADDRESS 5555

WRITE  DATA 55 TO ADDRESS 2AAA

WRITE  DATA 20 TO ADDRESS 5555

3005 FHD F19

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E$^2$PROM programmer, the following six step algorithm will reset the internal protection circuit. After $t_{WC}$, the X28LC512/513 will be in standard operating mode.

*Note: Once initiated, the sequence of write operations should not be interrupted.*

## SYSTEM CONSIDERATIONS

Because the X28LC512/513 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28LC512/513 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between $V_{CC}$ and $V_{SS}$ at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between $V_{CC}$ and $V_{SS}$ for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.
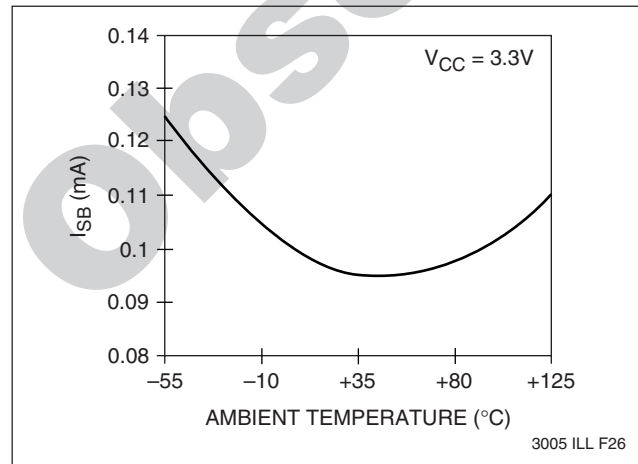
### Active Supply Current vs. Ambient Temperature



3005 ILL F25
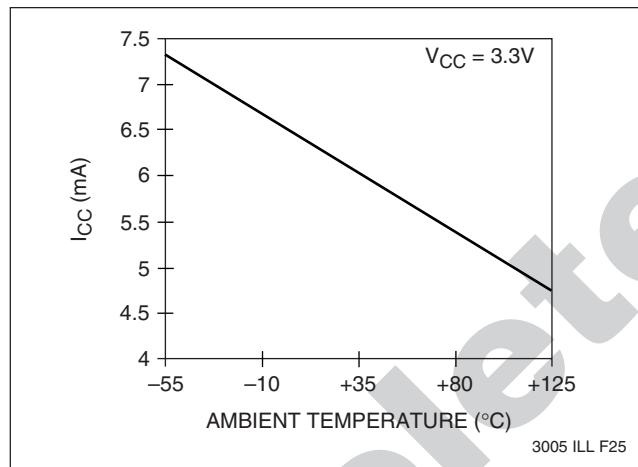
### $I_{CC}$ (RD) by Temperature over Frequency



3005 ILL F24
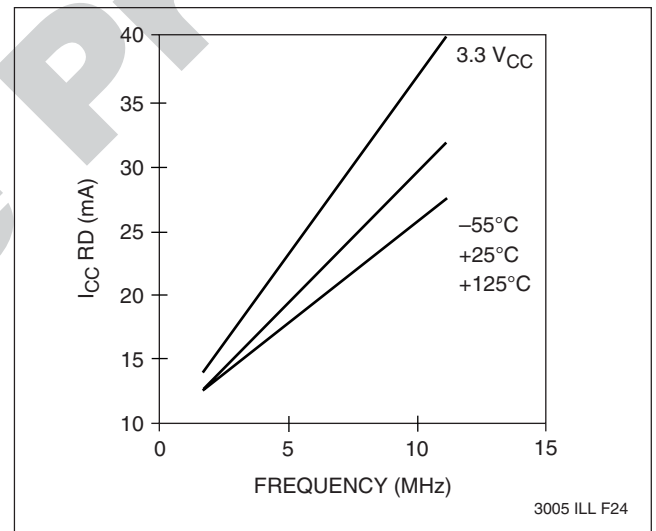
### Standby Supply Current vs. Ambient Temperature



3005 ILL F26

**ABSOLUTE MAXIMUM RATINGS***

Temperature under Bias
X28LC512/513 ............................ −10°C to +85°C
X28LC512I/X28LC513I .............. −65°C to +135°C
Storage Temperature ...................... −65°C to +150°C
Voltage on any Pin with
Respect to $V_{SS}$ ..................................... −1V to +7V
D.C. Output Current ............................................. 5mA
Lead Temperature
(Soldering, 10 seconds) .............................. 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMEND OPERATING CONDITIONS**

| Temperature | Min. | Max. |
|---|---|---|
| Commercial | 0°C | +70°C |
| Industrial | −40°C | +85°C |

3005 PGM T02

| Supply Voltage | Limits |
|---|---|
| X28LC512/513 | 3.3V ±10% |

3005 PGM T03.1

**D.C. OPERATING CHARACTERISTICS** (Over recommended operating conditions, unless otherwise specified.)

| Symbol | Parameter | Min. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|
| | | Limits | | | |
| $I_{CC}$ | $V_{CC}$ Current (Active) (CMOS Inputs) | | 25 | mA | $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, All I/O's = Open, Address Inputs = $0.1xV_{CC}/0.9xV_{CC}$ Levels @ f = 5MHz |
| $I_{SB}$ | $V_{CC}$ Current (Standby) (CMOS Inputs) | | 150 | μA | $\overline{OE} = V_{IL}$, $\overline{CE} = V_{CC} - 0.3V$ All I/O's = Open, Other Inputs = $V_{IH}$ |
| $I_{LI}$ | Input Leakage Current | | 10 | μA | $V_{IN} = V_{SS}$ to $V_{CC}$ |
| $I_{LO}$ | Output Leakage Current | | 10 | μA | $V_{OUT} = V_{SS}$ to $V_{CC}$, $\overline{CE} = V_{CC}$ |
| $V_{IL}$[1] | Input LOW Voltage | −1 | 0.6 | V | |
| $V_{IH}$[1] | Input HIGH Voltage | 2 | $V_{CC} + 0.5$ | V | |
| $V_{OL}$ | Output LOW Voltage | | 0.4 | V | $I_{OL} = 1mA$ |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | V | $I_{OH} = -200μA$ |

3005 PGM T04.2

**Notes:** (1) $V_{IL}$ min. and $V_{IH}$ max. are for reference only and are not tested.

## POWER-UP TIMING

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $t_{PUR}$[2] | Power-up to Read Operation | 100 | μs |
| $t_{PUW}$[2] | Power-up to Write Operation | 5 | ms |

3005 PGM T05

## CAPACITANCE $T_A = +25°C$, f = 1MHz, $V_{CC} = 3.3V$

| Symbol | Parameter | Max. | Units | Test Conditions |
|---|---|---|---|---|
| $C_{I/O}$[2] | Input/Output Capacitance | 10 | pF | $V_{I/O} = 0V$ |
| $C_{IN}$[2] | Input Capacitance | 10 | pF | $V_{IN} = 0V$ |

3005 PGM T06.1

## ENDURANCE AND DATA RETENTION

| Parameter | Min. | Max. | Units |
|---|---|---|---|
| Endurance | 10,000 | | Cycles per Byte |
| Data Retention | 100 | | Years |

3005 PGM T11

## A.C. CONDITIONS OF TEST

| | |
|---|---|
| Input Pulse Levels | 0V to 3V |
| Input Rise and Fall Times | 10ns |
| Input and Output Timing Levels | 1.5V |

3856 PGM T07.1

## MODE SELECTION

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | I/O | Power |
|---|---|---|---|---|---|
| L | L | H | Read | $D_{OUT}$ | Active |
| L | H | L | Write | $D_{IN}$ | Active |
| H | X | X | Standby and Write Inhibit | High Z | Standby |
| X | L | X | Write Inhibit | — | — |
| X | X | H | Write Inhibit | — | — |

3005 PGM T08

## EQUIVALENT A.C. LOAD CIRCUIT



3005 ILL F21.3
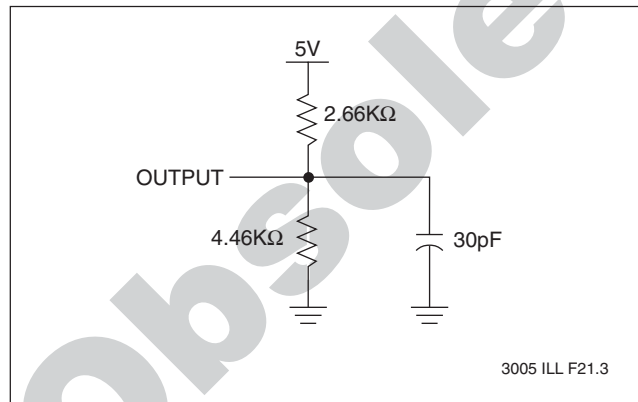
**Note:** (2) This parameter is periodically sampled and not 100% tested.

## SYMBOL TABLE

**A.C. CHARACTERISTICS** (Over the recommended operating conditions, unless otherwise specified.)

**Read Cycle Limits**

| Symbol | Parameter | X28LC512-15 X28LC513-15 Min. | Max. | X28LC512-20 X28LC513-20 Min. | Max. | X28LC512-25 X28LC513-25 Min. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{RC}$ | Read Cycle Time | 150 | | 200 | | 250 | | ns |
| $t_{CE}$ | Chip Enable Access Time | | 150 | | 200 | | 250 | ns |
| $t_{AA}$ | Address Access Time | | 150 | | 200 | | 250 | ns |
| $t_{OE}$ | Output Enable Access Time | | 80 | | 80 | | 80 | ns |
| $t_{LZ}$[3] | $\overline{CE}$ LOW to Active Output | 0 | | 0 | | 0 | | ns |
| $t_{OLZ}$[3] | $\overline{OE}$ LOW to Active Output | 0 | | 0 | | 0 | | ns |
| $t_{HZ}$[3] | $\overline{CE}$ HIGH to High Z Output | | 50 | | 50 | | 50 | ns |
| $t_{OHZ}$[3] | $\overline{OE}$ HIGH to High Z Output | | 50 | | 50 | | 50 | ns |
| $t_{OH}$ | Output Hold from Address Change | 0 | | 0 | | 0 | | ns |

3005 PGM T09.2

**Read Cycle**
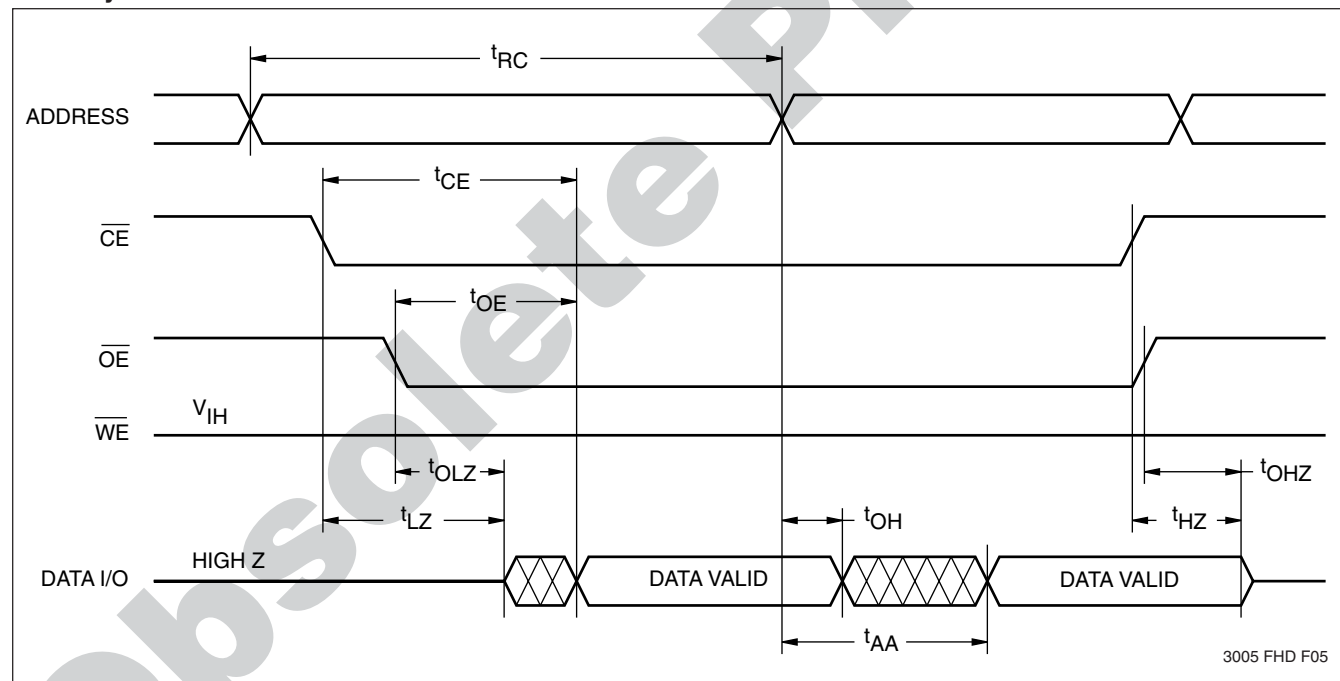


3005 FHD F05

**Notes:** (3) $t_{LZ}$ min., $t_{HZ}$, $t_{OLZ}$ min., and tOHZ are periodically sampled and not 100% tested. $t_{HZ}$ max. and $t_{OHZ}$ max. are measured, with $C_L$ = 5pF from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

## WRITE CYCLE LIMITS

| Symbol | Parameter | Min. | Max. | Units |
|--------|-----------|------|------|-------|
| $t_{WC}$[4] | Write Cycle Time | | 5 | ms |
| $t_{AS}$ | Address Setup Time | 0 | | ns |
| $t_{AH}$ | Address Hold Time | 50 | | ns |
| $t_{CS}$ | Write Setup Time | 0 | | ns |
| $t_{CH}$ | Write Hold Time | 0 | | ns |
| $t_{CW}$ | $\overline{CE}$ Pulse Width | 100 | | ns |
| $t_{OES}$ | $\overline{OE}$ HIGH Setup Time | 10 | | ns |
| $t_{OEH}$ | $\overline{OE}$ HIGH Hold Time | 10 | | ns |
| $t_{WP}$ | $\overline{WE}$ Pulse Width | 100 | | ns |
| $t_{WPH}$ | $\overline{WE}$ HIGH Recovery | 100 | | ns |
| $t_{DV}$ | Data Valid | | 1 | µs |
| $t_{DS}$ | Data Setup | 50 | | ns |
| $t_{DH}$ | Data Hold | 0 | | ns |
| $t_{DW}$ | Delay to Next Write | 10 | | µs |
| $t_{BLC}$ | Byte Load Cycle | 0.20 | 100 | µs |

3005 PGM T10.1

## $\overline{WE}$ Controlled Write Cycle
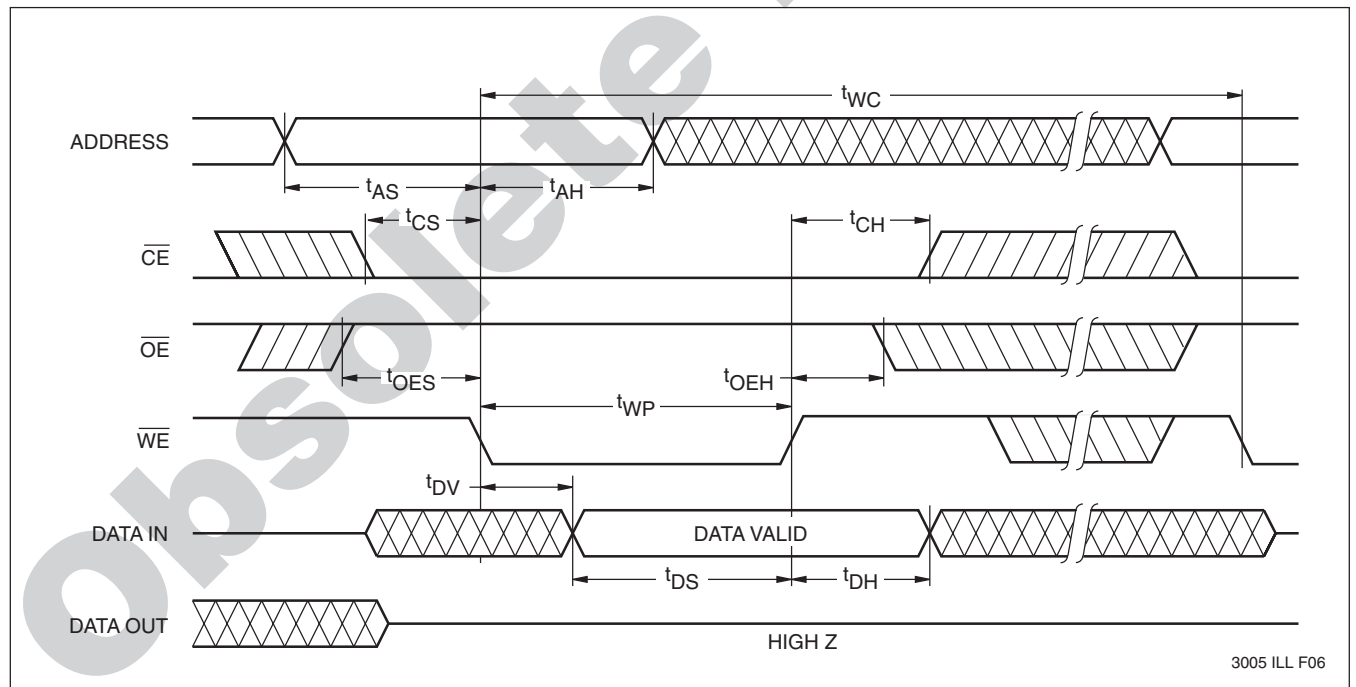


3005 ILL F06

**Notes:** (4) $t_{WC}$ is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete the internal write operation.

## $\overline{CE}$ Controlled Write Cycle



3005 ILL F07

## Page Write Cycle



*For each successive write within the page write operation, $A_7$–$A_{15}$ should be the same or writes to an unknown address could occur.
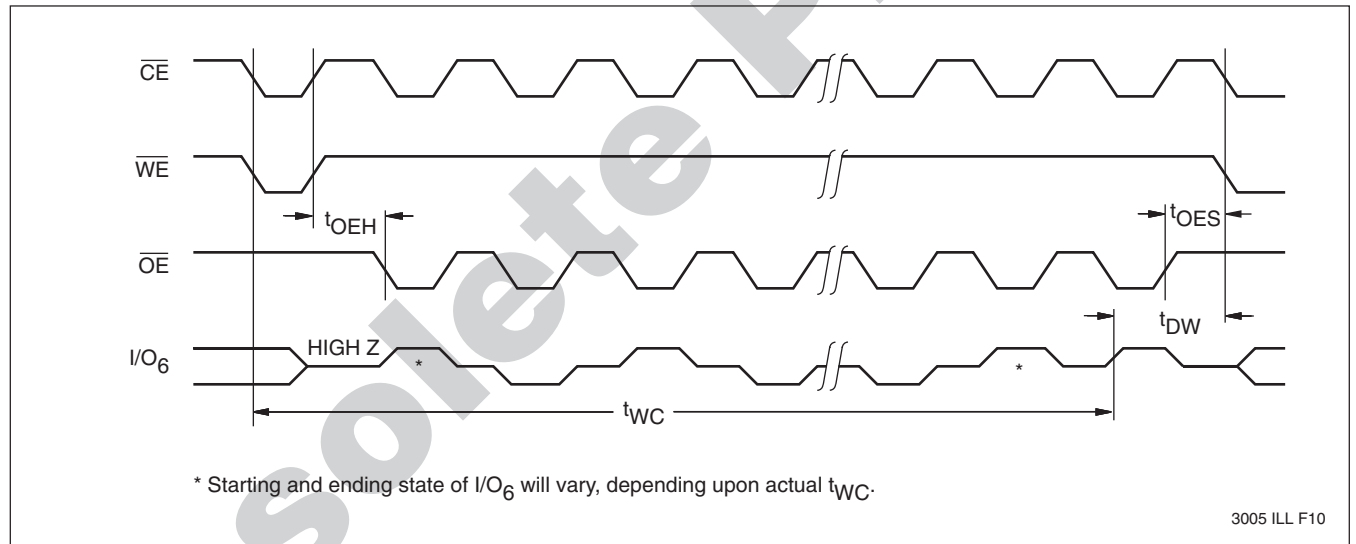
3005 ILL F08.1
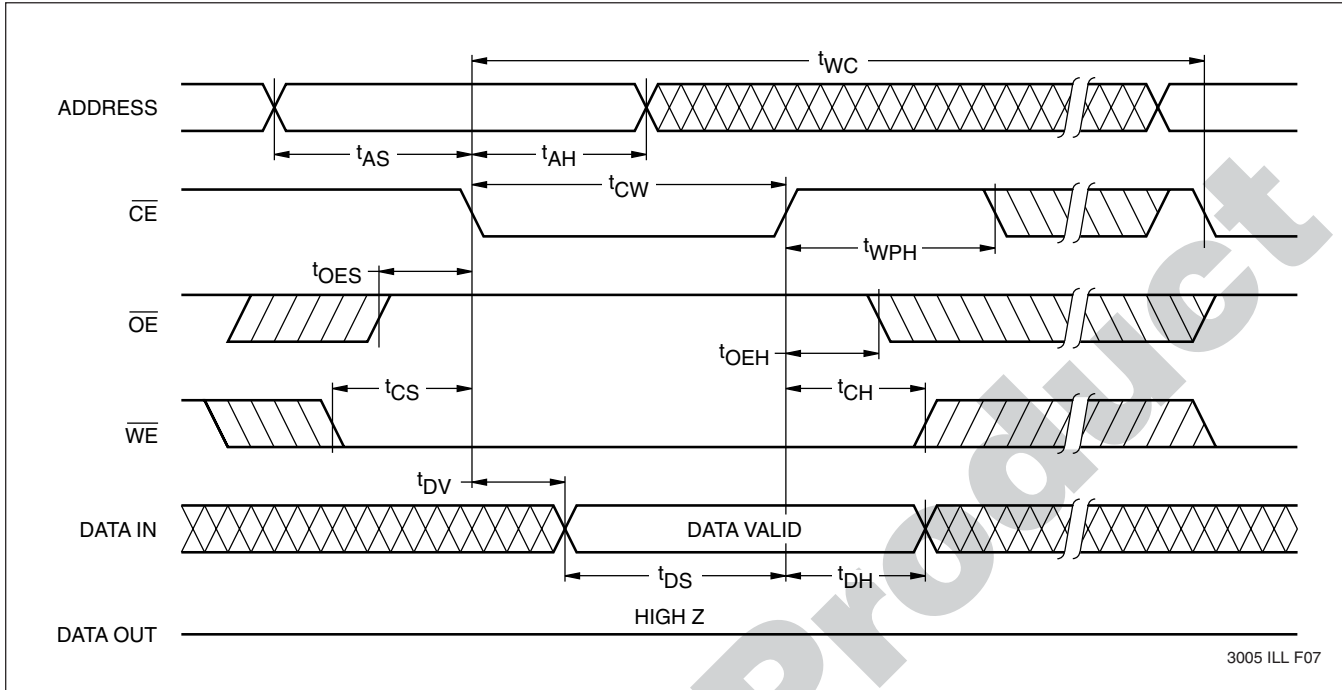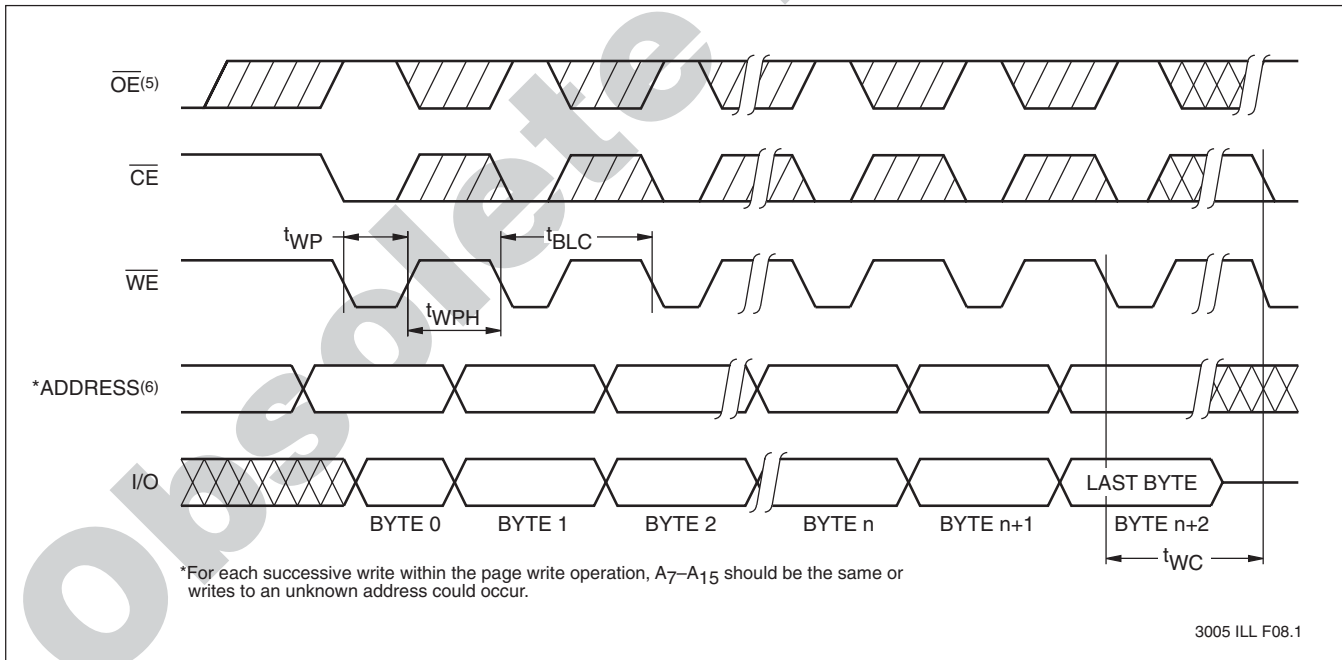
**Notes:** (5) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

## $\overline{\text{DATA}}$ **Polling Timing Diagram**[7]



ADDRESS $A_n$ $A_n$ $A_n$

$\overline{\text{CE}}$

$\overline{\text{WE}}$

$t_{OEH}$ $t_{OES}$

$\overline{\text{OE}}$

$t_{DW}$

$I/O_7$ $D_{IN}=X$ $D_{OUT}=\overline{X}$ $D_{OUT}=X$

$t_{WC}$

3005 ILL F09
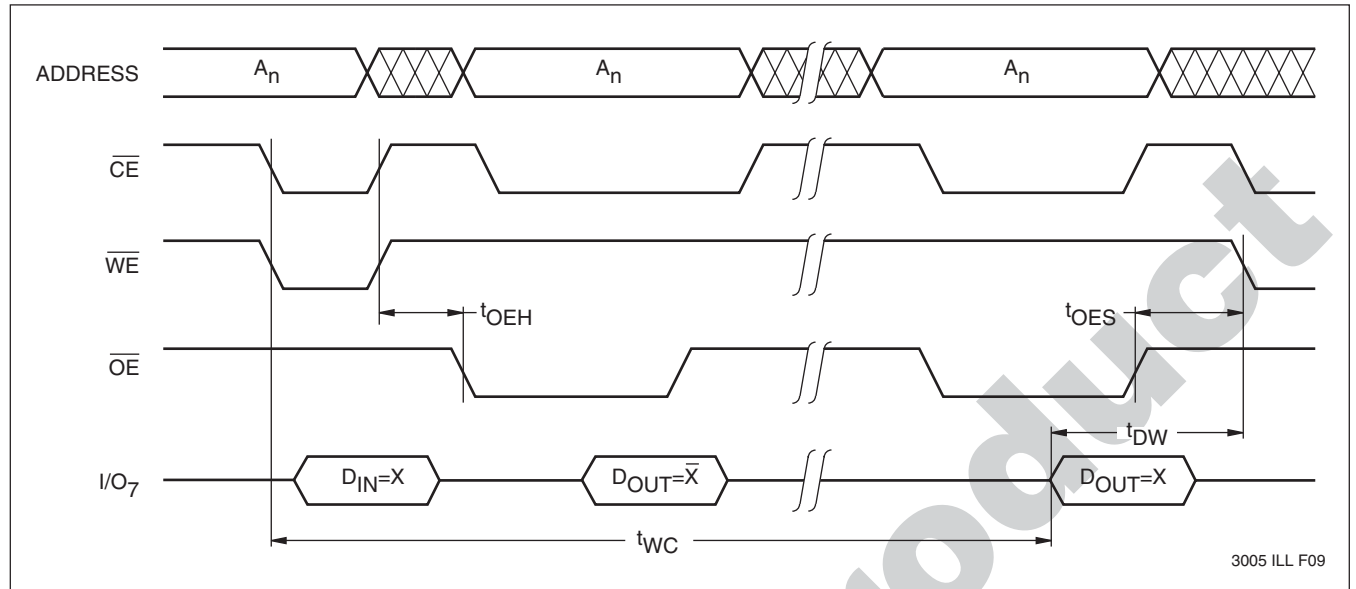
## **Toggle Bit Timing Diagram**



$\overline{\text{CE}}$

$\overline{\text{WE}}$

$t_{OEH}$ $t_{OES}$

$\overline{\text{OE}}$

$t_{DW}$

$I/O_6$ HIGH Z * *

$t_{WC}$

* Starting and ending state of $I/O_6$ will vary, depending upon actual $t_{WC}$.

3005 ILL F10

**Note:** (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

## PACKAGING INFORMATION

### 32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J

0.420 (10.67)

0.050 (1.27) TYP.

0.021 (0.53)
0.013 (0.33)
TYP. 0.017 (0.43)

0.045 (1.14) x 45°

SEATING PLANE
±0.004 LEAD
CO – PLANARITY

—
0.015 (0.38)

0.095 (2.41)
0.060 (1.52)

0.140 (3.56)
0.100 (2.45)
TYP. 0.136 (3.45)

0.048 (1.22)
0.042 (1.07)

0.495 (12.57)
0.485 (12.32)
TYP. 0.490 (12.45)

0.453 (11.51)
0.447 (11.35)
TYP. 0.450 (11.43)

0.300 (7.62)
REF.

PIN 1

0.595 (15.11)
0.585 (14.86)
TYP. 0.590 (14.99)

0.553 (14.05)
0.547 (13.89)
TYP. 0.550 (13.97)

0.400
(10.16) REF.

3° TYP.
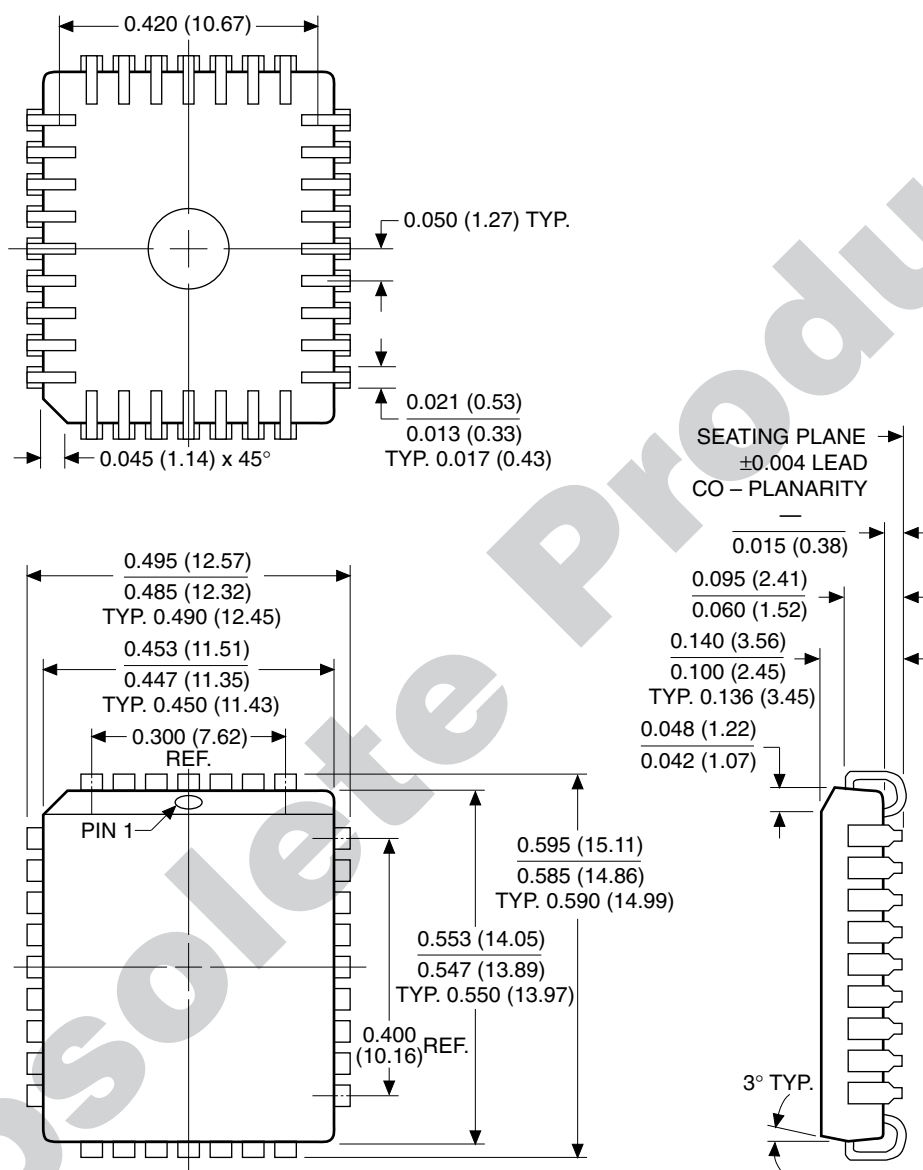
**NOTES:**
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

3926 FHD F13

## PACKAGING INFORMATION

### 32-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

1.665 (42.29)
1.644 (41.76)

0.557 (14.15)
0.510 (12.95)

PIN 1 INDEX

PIN 1

1.500 (38.10)
REF.

0.085 (2.16)
0.040 (1.02)

0.160 (4.06)
0.140 (3.56)

SEATING
PLANE

0.030 (0.76)
0.015 (0.38)

0.160 (4.06)
0.125 (3.17)

0.110 (2.79)
0.090 (2.29)

0.070 (17.78)
0.030 (7.62)

0.022 (0.56)
0.014 (0.36)

0.625 (15.88)
0.590 (14.99)

TYP. 0.010 (0.25)

0°
15°
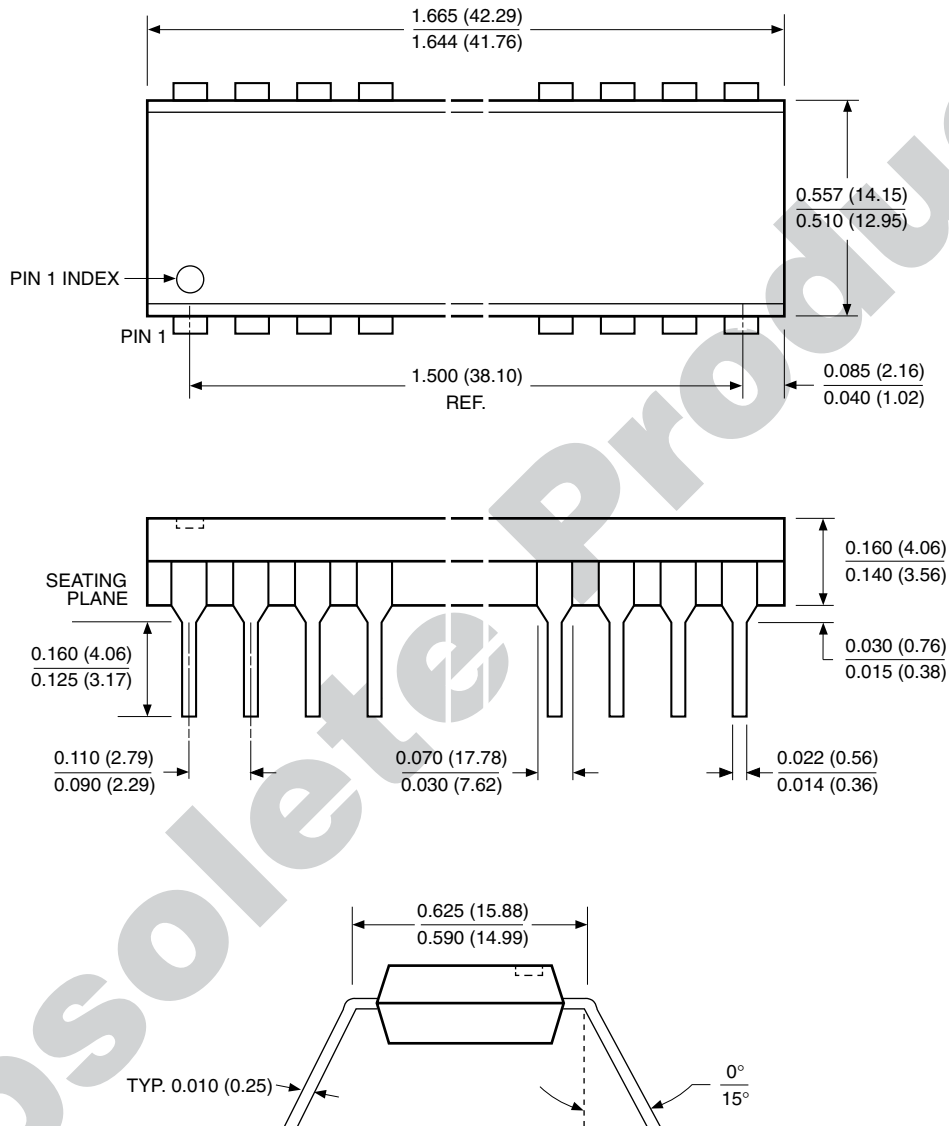
NOTE:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

3926 FHD F25

17

## PACKAGING INFORMATION

### 40-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) TYPE T

12.522 (0.493)
12.268 (0.483)

1.143 (0.045)
0.889 (0.035)

0.965
(0.038)

PIN #1 IDENT.
Ø 1.016 (0.040) X 0.127 (0.005) DP.
Ø 0.762 (0.030) 0.076 (0.003) DP.

1

10.058 (0.396)
9.957 (0.392)

1.219 (0.048)

0.500 (0.0197)

0.178 (0.007)

15° TYP.

SEATING
PLANE

0.254 (0.010)
0.152 (0.006)

1.016 (0.040)

A

0.065 (0.0025)

SEATING
PLANE

14.148 (0.557)
13.894 (0.547)

**DETAIL A**

0.813 (0.032) TYP.

0.432 (0.017)

0.152 (0.006)
TYP.

4° TYP.

0.508 (0.020) TYP.

0.432 (0.017)

14.80 ± 0.05
(0.583 ± 0.002)

0.30 ± 0.05
(0.012 ± 0.002)

SOLDER PADS

TYPICAL
40 PLACES

15 EQ. SPC. @ 0.50 ± 0.04
0.0197 ± 0.016 = 9.50 ± 0.06
(0.374 ± 0.0024) OVERALL
TOL. NON-CUMULATIVE

0.17 (0.007)
0.03 (0.001)

1.30 ± 0.05
(0.051 ± 0.002)

0.50 ± 0.04
(0.0197 ± 0.0016)

FOOTPRINT

**NOTE:**
**1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES IN PARENTHESES).**

3926 ILL F39.2

# X28LC512/X28LC513

## ORDERING INFORMATION

**X28LC512 X X -X**

Device ────

**Access Time**
−15 = 150ns
−20 = 200ns
−25 = 250ns

**Temperature Range**
Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C

**Package**
J = 32-Lead PLCC
P = 32-Lead Plastic Dip
T = 40-Lead TSOP

**X28LC513 X X -X**

Device ────

**Access Time**
−15 = 150ns
−20 = 200ns
−25 = 250ns

**Temperature Range**
Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C

**Package**
J = 32-Lead PLCC