54AC/74AC190 • 54AC/74AC191

Up/Down Counters with Preset and Ripple Clock

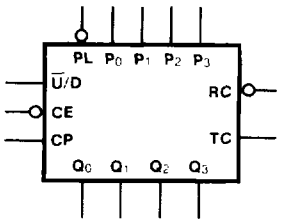
Description

The 'AC190 is a reversible BCD (8421) decade counter. The 'AC191 is a reversible modulo 16 binary counter. Both feature synchronous counting and asynchronous presetting. The preset feature allows the 'AC190 and 'AC191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

- **High-speed—120 MHz Typical Count Frequency**
- **Synchronous Counting**
- **Asynchronous Parallel Load**
- **Cascadable**
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 6

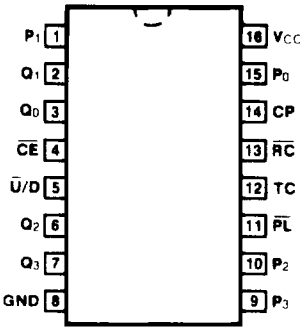
Logic Symbol



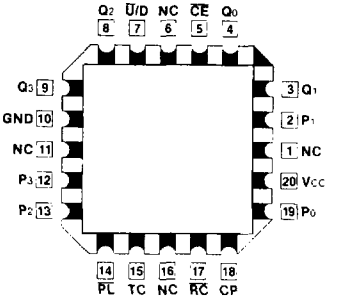
Pin Names

$\overline{CE}$	Count Enable Input
CP	Clock Pulse Input
P_0 - P_3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input
$\overline{U}$/D	Up/Down Count Control Input
Q_0 - Q_3	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output
TC	Terminal Count Output

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Functional Description

The 'AC190/'AC191 are synchronous up/down counters. The 'AC190 is a BCD decade counter while the 'AC191 is organized as a 4-bit binary counter. Both contain four edge-triggered flip-flops with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Load inputs (P_0 - P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The terminal count (TC) output is normally LOW. It goes HIGH when the circuits reach zero in the count down mode or 9 ('AC190) or 15 ('AC191) in the count up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures a and b. In Figure a, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of

Mode Select Table

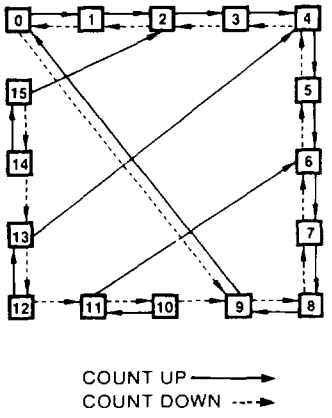
Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

$\overline{RC}$ Truth Table

Inputs			Outputs
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⌐⌙	⌐⌙
H	X	X	H
X	L	X	H

*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

State Diagram



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this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The $\overline{CE}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

Figure a: N-Stage Counter Using Ripple Clock

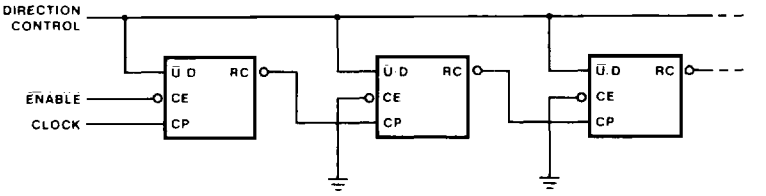


Figure b: Synchronous N-Stage Counter Using Ripple Carry/Borrow

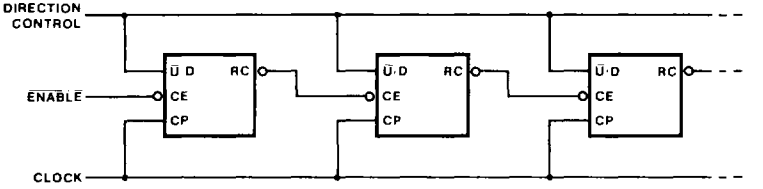
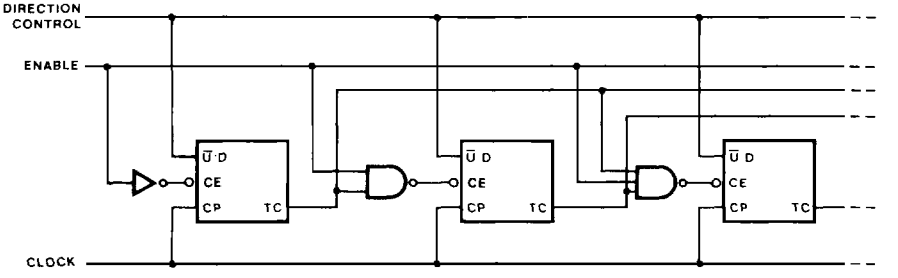
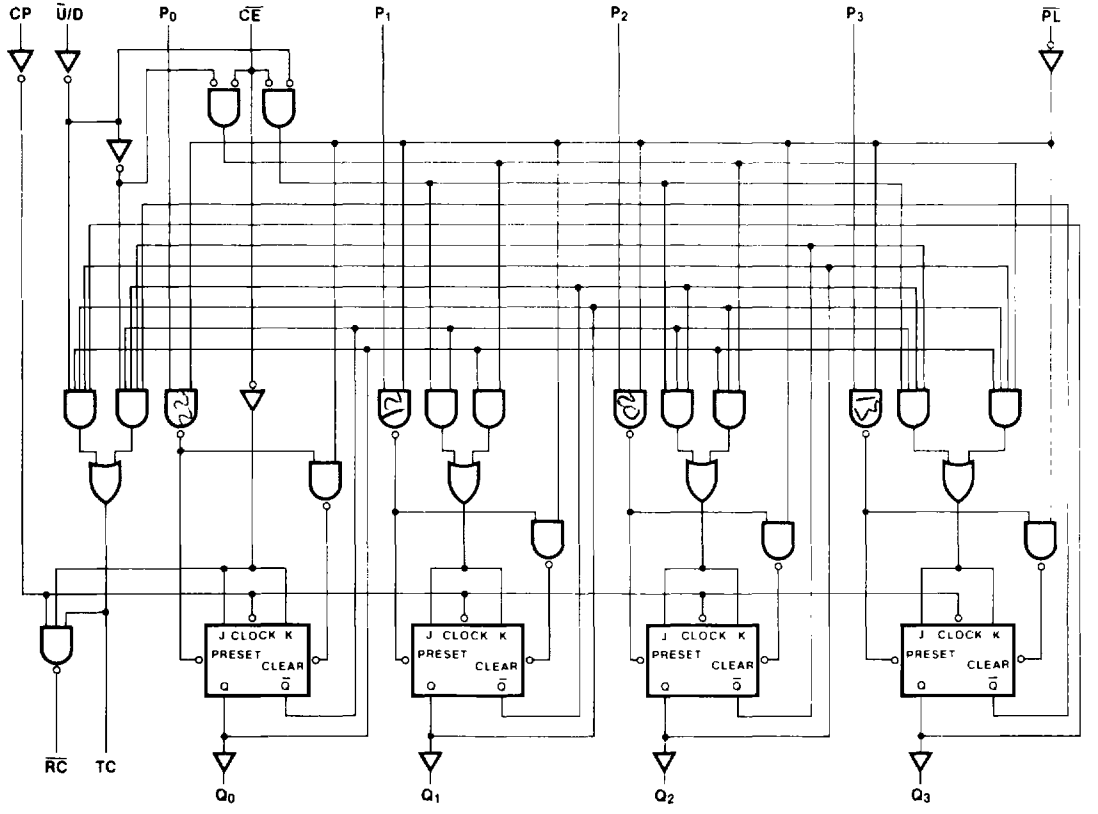


Figure c: Synchronous N-Stage Counter With Parallel Gated Carry/Borrow



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC190 $T_A = +25°C$, $C_L = 50$ pF			54AC190 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC190 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0		88 120						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0		10.5 7.5						ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0		15.0 11.0						ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0		13.0 9.5						ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{RC}$	3.3 5.0		9.0 6.5						ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{RC}$	3.3 5.0		9.5 7.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3 5.0		8.5 6.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{U}/D$ to $\overline{RC}$	3.3 5.0		11.0 8.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{U}/D$ to $\overline{RC}$	3.3 5.0		10.5 7.5						ns	3-6
t_{PLH}	Propagation Delay $\overline{U}/D$ to TC	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{U}/D$ to TC	3.3 5.0		9.5 7.0						ns	3-6
t_{PLH}	Propagation Delay P_n to Q_n	3.3 5.0		10.5 7.5						ns	3-6
t_{PHL}	Propagation Delay P_n to Q_n	3.3 5.0		9.5 7.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0		11.5 8.5						ns	3-6
t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0		11.5 8.5						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC190 $T_A = +25°C$ $C_L = 50$ pF		54AC190 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC190 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	4.5 3.0				ns	3-9
t_h	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	−0.5 −0.5				ns	3-9
t_s	Setup Time, LOW $\overline{CE}$ to CP	3.3 5.0	7.0 5.0				ns	3-9
t_h	Hold Time, LOW $\overline{CE}$ to CP	3.3 5.0	−1.5 −1.0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{U}/D$ to CP	3.3 5.0	7.0 5.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{U}/D$ to CP	3.3 5.0	−1.5 −1.0				ns	3-9
t_w	$\overline{PL}$ Pulse Width, LOW	3.3 5.0	5.5 6.0				ns	3-6
t_w	CP Pulse Width, LOW	3.3 5.0	5.5 6.0				ns	3-6
t_{rec}	Recovery Time $\overline{PL}$ to CP	3.3 5.0	4.5 3.0				ns	3-9

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC191 $T_A = +25°C$, $C_L = 50$ pF			54AC191 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC191 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	70 90	105 133		60 80		65 85		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0	3.0 2.0	8.5 6.0	15.0 11.0	1.0 1.0	17.5 13.0	1.0 1.0	16.0 12.0	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0	3.0 2.0	8.5 6.0	14.5 10.5	1.0 1.0	17.5 12.5	1.0 1.0	16.0 11.5	ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	4.0 3.0	10.5 7.5	18.0 12.0	1.0 1.0	22.0 15.5	1.0 1.0	20.0 14.0	ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	4.5 3.0	10.5 7.5	17.5 12.5	1.0 1.0	20.5 15.0	1.0 1.0	19.0 13.5	ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{RC}$	3.3 5.0	3.0 2.5	7.5 5.5	12.0 9.5	1.0 1.0	14.5 11.0	1.0 1.0	13.5 10.5	ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{RC}$	3.3 5.0	2.5 2.0	7.0 5.0	11.5 8.5	1.0 1.0	14.0 10.0	1.0 1.0	12.5 9.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3 5.0	2.5 1.5	7.0 5.0	12.0 8.5	1.0 1.0	15.0 10.5	1.0 1.0	13.5 9.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3 5.0	2.5 1.5	6.5 5.0	11.0 8.0	1.0 1.0	14.0 10.0	1.0 1.0	12.5 9.0	ns	3-6
t_{PLH}	Propagation Delay $\overline{U}/D$ to $\overline{RC}$	3.3 5.0	2.5 1.5	6.5 5.0	12.5 9.0	1.0 1.0	16.0 11.5	1.0 1.0	14.5 10.0	ns	3-6
t_{PHL}	Propagation Delay $\overline{U}/D$ to $\overline{RC}$	3.3 5.0	2.5 1.5	7.0 5.0	12.0 8.5	1.0 1.0	15.5 11.0	1.0 1.0	13.5 10.0	ns	3-6
t_{PLH}	Propagation Delay $\overline{U}/D$ to TC	3.3 5.0	2.5 2.0	7.0 5.0	11.5 8.5	1.0 1.0	14.5 10.5	1.0 1.0	13.5 9.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{U}/D$ to TC	3.3 5.0	2.5 1.5	6.5 5.0	11.0 8.5	1.0 1.0	13.5 10.5	1.0 1.0	12.5 9.5	ns	3-6
t_{PLH}	Propagation Delay P_n to Q_n	3.3 5.0	3.0 2.0	8.0 5.5	13.5 9.5	1.0 1.0	17.0 11.5	1.0 1.0	15.5 10.5	ns	3-6
t_{PHL}	Propagation Delay P_n to Q_n	3.3 5.0	3.0 2.0	7.5 5.5	13.0 9.5	1.0 1.0	16.5 11.5	1.0 1.0	14.5 10.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0	3.5 2.0	9.5 5.5	14.5 9.5	1.0 1.0	19.0 11.5	1.0 1.0	17.5 10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0	3.0 2.0	8.0 6.0	13.5 10.0	1.0 1.0	16.5 12.0	1.0 1.0	15.5 11.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC191 $T_A = +25°C$ $C_L = 50$ pF	54AC191 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC191 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	1.0 0.5	3.0 2.0	3.5 3.0	3.0 2.5	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	-1.5 -0.5	0.5 1.0	1.0 1.0	1.0 1.0	ns	3-9
t_s	Setup Time, LOW $\overline{CE}$ to CP	3.3 5.0	3.0 1.5	6.0 4.0	7.5 5.0	7.0 4.5	ns	3-9
t_h	Hold Time, LOW $\overline{CE}$ to CP	3.3 5.0	-4.0 -2.5	-0.5 0	-0.5 0	-0.5 0	ns	3-9
t_s	Setup Time, HIGH or LOW, $\overline{U}$/D to CP	3.3 5.0	4.0 2.5	8.0 5.5	10.5 7.0	9.0 6.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{U}$/D to CP	3.3 5.0	-5.0 -3.0	0 0.5	0 0.5	0 0.5	ns	3-9
t_w	$\overline{PL}$ Pulse Width, LOW	3.3 5.0	2.0 1.0	3.5 1.0	4.5 1.0	4.0 1.0	ns	3-6
t_w	CP Pulse Width, LOW	3.3 5.0	2.0 2.0	3.5 3.0	4.5 4.0	4.0 4.0	ns	3-6
t_{rec}	Recovery Time $\overline{PL}$ to CP	3.3 5.0	-0.5 -1.0	0 0	0 0	0 0	ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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Capacitance

Symbol	Parameter	54/74AC Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	75.0	pF	$V_{CC} = 5.5$ V