High Speed ±100V 2A Integrated Ultrasound Pulser Demo Board

Introduction

The HV732 is a complete, high-speed, high voltage, ultrasound transmitter pulser. This integrated high performance circuit is in a single 7x7x0.9mm 44-lead, multi-die, QFN package.

The HV732 can deliver up to ±2A source and sink current to a capacitive transducer. It is designed to be used as a high voltage pulser or transmitter in medical ultrasound imaging and ultrasound material NDT applications. It can also be used for other piezoelectric or capacitive MEMS transducers as a high voltage driver, or for ATE systems and pulse signal generators as a signal source.

The HV732 has built-in damping circuits to generate fast return-to-zero waveforms. It also has built-in, high voltage MOSFET gate-clamping functions to quickly change the output waveform amplitude.

HV732 circuitry consists of controller logic circuits, level translators, a MOSFET driving buffer, gate-clamp circuits and MOSFET transistors as the high current and high voltage output stage. There are two pairs of MOSFETs in the output stage. Each pair is consists of a P-channel and an N-channel MOSFET. In each pair of MOSFETs, the P-FET and N-FET are designed to have the same impedance and can provide peak currents of over 2 amps. In the MOSFET gate-driver circuits, the output of the driver can swing from 0 to 9V~12V on P_{DR} and N_{DR} pins, and the P-channel damping output swings from 0V to –5V on the DMPO pin. HV732 can generate ±100V NRZ, RZ and PW pulses and low voltage CW waveforms. The up frequency limit of this IC is as high as 35MHz to 40MHz dependent on the load capacitance.

Designing a Pulser with HV732

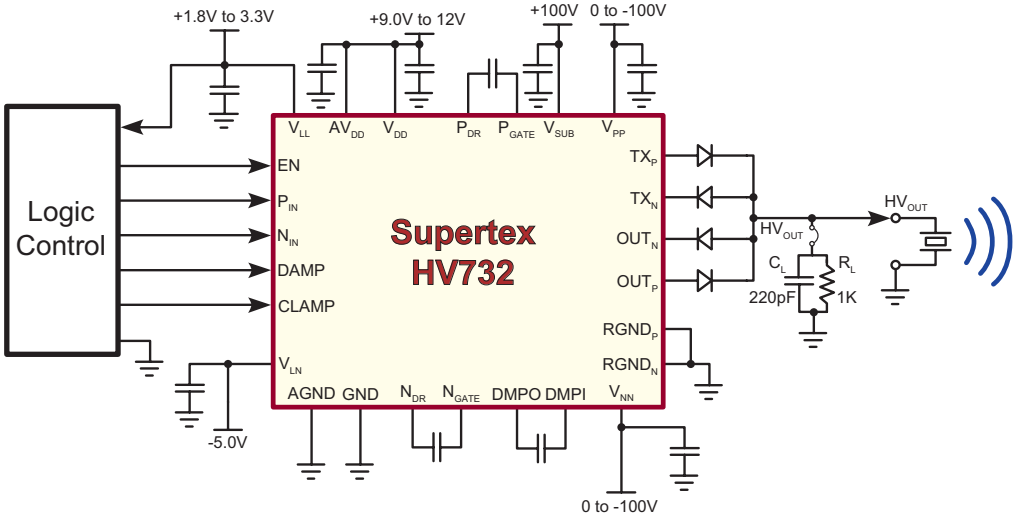
This demo board data sheet describes how to use the HV732DB1 to generate the basic high voltage pulses for an ultrasound transmitter with a RTZ feature.

The HV732 circuit uses the capacitor-coupling method in its level translators, except for the one driving the N-channel damping MOSFET, which is DC coupled. There are three 10nF 200V ceramic capacitors connecting the driver output to the MOSFET's gate for the coupling purposes.

The input stage of the HV732 has high-speed level translators that are able to operate with logic signals of 1.8V, 2.5V or 3.3V. In this demo board, the control logic signals are connected to a high-speed ribbon cable connector. The control signal logic-high voltage should be same as the V_{CC} voltage of the demo board, and the logic-low should be referenced to GND.

The HV732DB1 output waveforms can be displayed using an oscilloscope directly by connecting the scope probe to the test point HV_{OUT} and GND. The soldering jumper R1 can select whether or not to connect the on-board equivalent-load, a 220pF, 200V capacitor, parallel with a 1kΩ, 1W resistor. A coaxial cable can also be used to connect the user's transducer to be driven and evaluated with this HV732 transmitter pulser directly and easily.

Schematic Block Diagram



The PCB Layout Techniques

The big thermal pad at the bottom of the HV732 package is connected to the V_{SUB} pin to make sure that in any condition it always has the highest potential of the chip. V_{SUB} is the connection of the IC's substrate. The other two smaller pieces of the slab at the bottom of the chip are the drains of the high voltage output P-channel and N-channel MOSFETs. They are connected to high voltage outputs. PCB designers need to pay attention to the connecting the traces as high-voltage and high-speed traces. In particular, low capacitance to the ground plane and more trace spacing needs to be applied in this situation.

High-speed PCB trace design practices that are compatible with about 50MHz to 100MHz operating speed are used for the demo board PCB layout. The internal circuitry of the HV732 can operate at a quite high frequency, with the primary speed limitation being load capacitance. Because of this high speed and the high transient currents that result when driving capacitive loads, the supply voltage bypass capacitors and the driver to the FET's gate-coupling capacitors should be as close to the pins as possible. The GND and AGND pin pads should have low inductance feed-through connections that are connected directly to a solid ground plane. The V_{PP} and V_{NN} supplies can draw fast transient currents of up to 2.0A, so they should be provided with a low-impedance bypass capacitor at the chip's pins. A ceramic capacitor of 0.47µF to 1.0µF may be used. Minimize the trace length to the ground plane, and insert a ferrite bead in the power supply lead to the capacitor to prevent resonance in the power supply lines. For applications that are sensitive to jitter and noise and are using multiple HV732 ICs, insert another ferrite bead between V_{DD} and decouple each chip supply separately.

Pay particular attention to minimizing trace lengths and using sufficient trace width to reduce inductance. Surface mount components are highly recommended. Since the output impedance of HV732's high voltage power stages are very low, in some cases it may be desirable to add a small value resistor in series with the output TX_P and TX_N to obtain better waveform integrity at the load terminals. This will, of course, reduce the output voltage slew rate at the terminals of a capacitive load. The same technique can be applied to the driver output to P_{GATE} and N_{GATE}, if necessary.

Be aware of the parasitic coupling from the outputs to the input signal terminals of HV732. This feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.8V, even small coupling voltages may cause problems. Use of a solid ground plane and good power and signal layout practices will prevent this problem. Also ensure that the circulating ground return current from a capacitive load cannot react with common inductance to create noise voltages in the input logic circuitry.

Testing the Integrated Pulser

This HV732 pulser demo board should be powered up with multiple lab DC power supplies with current limiting functions. The following power supply voltages and current limits have been used in the testing: V_{SUB}/ V_{PP} = +15V to +100V 2.0mA, V_{NN} = 0V to -100V 2.0mA, V_{DD} = +9V to +12V 10mA, V_{LN} = -5V 5.0mA. V_{CC} = +3.3V 5.0mA. V_{SUB} and V_{PP} generally need to be connected to the same voltage. If the V_{CC} current needs to be included in the V_{CC} current of the user's logic circuits, then a higher current limit should be set.

The power-up or down sequences of the voltage supply ensure that the HV732 chip substrate, V_{SUB} and V_{PP}, are always at the highest potential of all the voltages supplied to the IC.

The on-board dummy load 220pF/1kΩ should be connected to the high voltage pulser output through the solder jumper when using an oscilloscope high impedance probe to meet the typical loading conditions. For looking into the different loading conditions, one may change the values of RC within the current and power limit of the device.

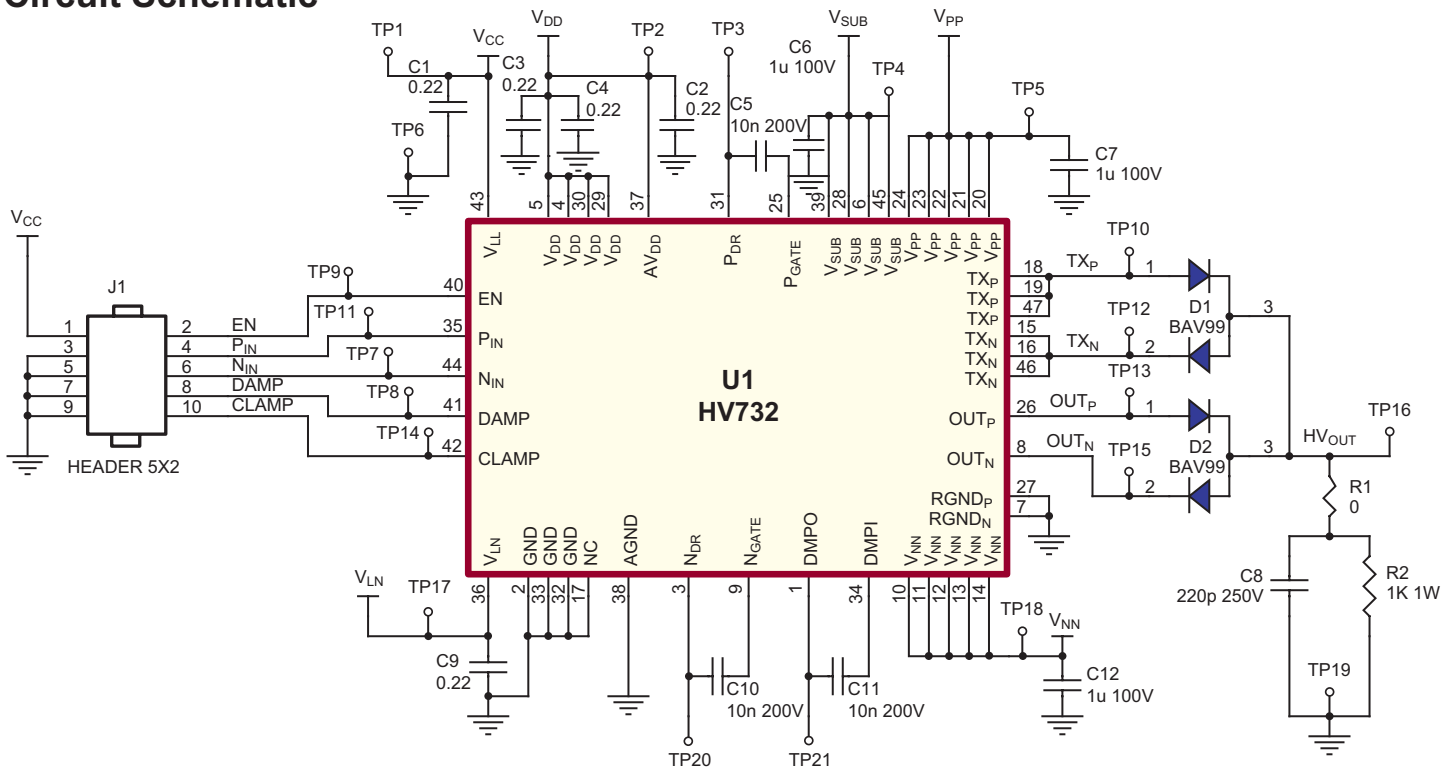
In order to drive piezo transducers with a cable, one should match the output load impendence properly to avoid cable and large transducer reflections. A 70Ω to 75Ω coaxial cable is recommended. The coaxial cable end should be soldered to the HV_{OUT} and GND directly with very short wire length leads.

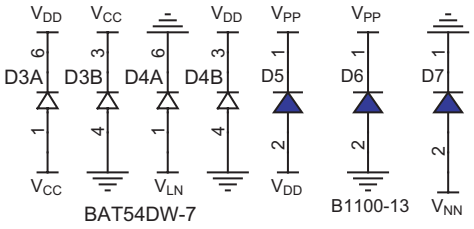
All the on-board test points are designed to work with the high impedance probe of the oscilloscope. Some probes may have limited input voltage. When using the probe on these high voltage test-points, make sure that V_{PP}/V_{NN} does not exceed the probe limit. Using the high impendence oscilloscope probe for the on-board test points, it is important that the ground leads to the circuit board ground plane are as short as possible.

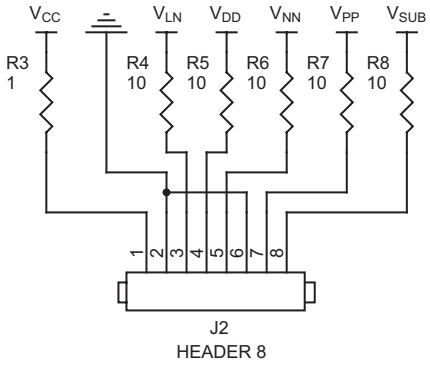
There are examples of the HV732 output waveforms and pulser input shown in the diagrams on pages 5-8.

Precautions need be applied to not overlap the logic-high time periods of the control signals. Permanent damage to the device may occur when cross-conduction or shoot-through currents exceed the device maximum limits. The input logic pins should connect to the low impedance CMOS logic control circuit outputs or 1kΩ pull-up or pull-down resistors during the test. Leave these pins floating or logic state unknown may damage the device.

Circuit Schematic

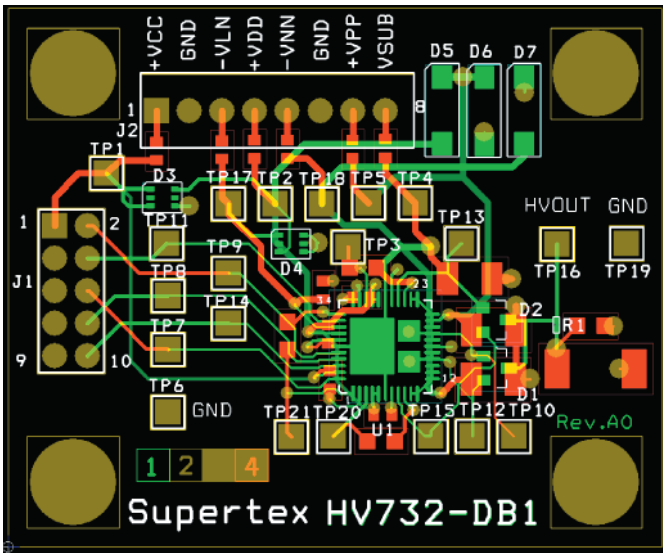






V_{SUB}/V_{PP} = +15 to +100V
V_{DD} = +9.0 to +12V
V_{LN} = -5V
V_{CC} = +1.8 to +3.3V
V_{NN} = 0 to -100V

PCB Layout



Board Voltage Supply Power-Up Sequence

1	V_{CC}	+15V to +100V the substrate and positive high voltages (1)
2	V_{DD}	+9V to +12V positive drive supply voltage
3	V_{SUB} /V_{PP}	+1.8V to 3.3V positive logic supply voltage
4	V_{LN}	-5V negative bias supply voltage
5	V_{NN}	0V to +/-100V negative high voltage (1)
6	Logic Active	Any logic control active high signals

Connector and Test Pin Description

Logic Control Signal Input Connector

1	V_{CC}	Logic-high reference voltage supply V_{LL}, +1.8V to 3.3V
2	EN	Pulser output enable logic signal input, active high
3	GND	Logic signal ground, 0V (3)
4	P_{IN}	Pulser positive high voltage pulse output control logic signal input, active high. (2)
5	GND	Logic signal ground, 0V (3)
6	N_{IN}	Pulser negative high voltage pulse output control logic signal input, active high. (2)
7	GND	Logic signal ground, 0V (3)
8	DAMP	Pulser high voltage pulse output zero-damping control logic signal input, active high. (2)
9	GND	Logic signal ground, 0V (3)
10	CLAMP	Output stage P and N-MOSFETs gate-clamping control logic signal input, active high. (2)

Power Supply Connector

1	V_{CC}	Logic-high reference voltage supply, +1.8V to 3.3V.with current limit to 5.0mA
2	GND	Low voltage power supply ground, 0V
3	V_{LN}	-5V negative bias supply with current limit to 5.0mA
4	V_{DD}	+9V to 12V positive driver voltage supply with current limit to 10mA
5	V_{NN}	0V to -100V Negative high voltage supply with current limit to 2.0mA (4)
6	GND	High voltage power supply ground, 0V
7	V_{PP}	+15V to +100V positive high voltage supply with current limit to 2.0mA (4)
8	V_{SUB}	Chip substrate bias voltage, must be same as V_{PP} with current limit to 2.0mA (4)

Note:

(1) Turn on or off with V_{SUB}/V_{PP} = +25V, V_{NN} = -25V is recommend. Then ramp V_{PP} or V_{NN} up or down slowly if without CLAMP control signal is Hi. V_{SUB}/V_{PP} = +100V and V_{NN} = -100V are maximum.

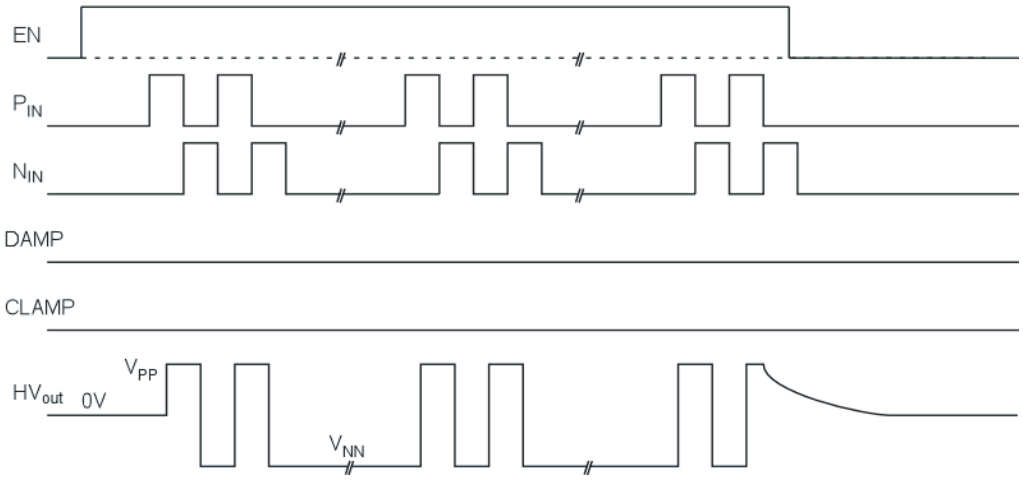
(2) Overlap control signal logic-high periods may cause the device permanent damage

(3) Due to the high speed control signal, every GND wire in the ribbon cable need connect to signal ground.

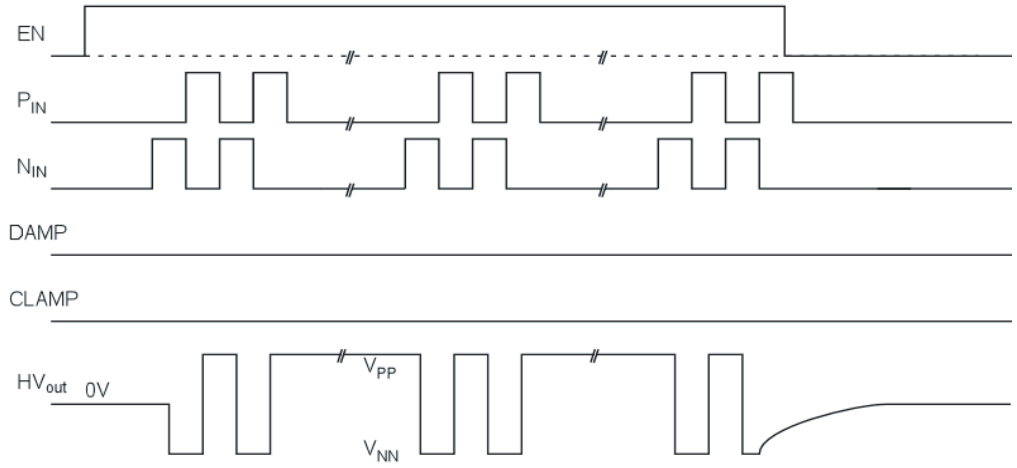
(4) It is important to note that some the high voltage capacitors and diodes on board are only rated at 100V, if need test unipolar conditions like V_{SUB}/V_{PP} = +150V and V_{NN} = -50V, or V_{SUB}/V_{PP} = +200V and V_{NN} = 0V etc., their voltage ratings need to be upgraded.

Input and Output Waveform Examples

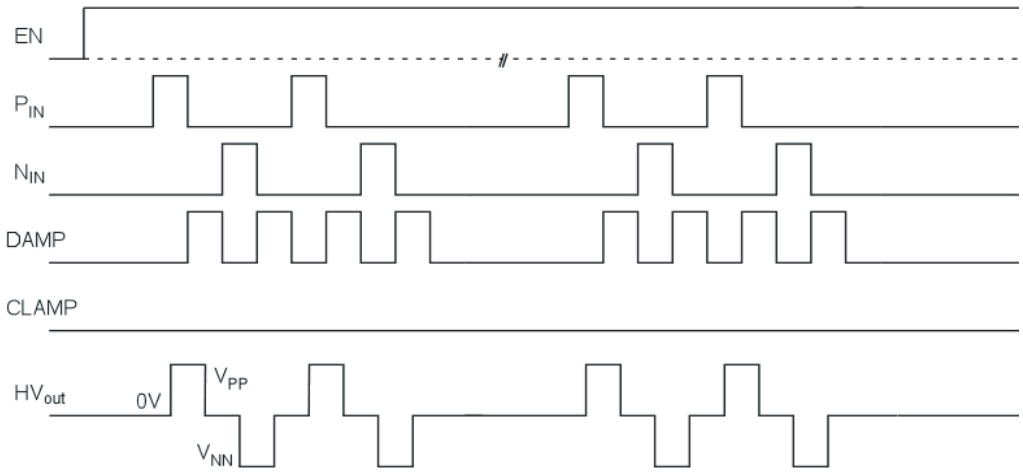
Demo Waveform A: NRZ Pulses with EN=Hi / Low



Demo Waveform B: NRZ Pulses with EN=Hi / Low

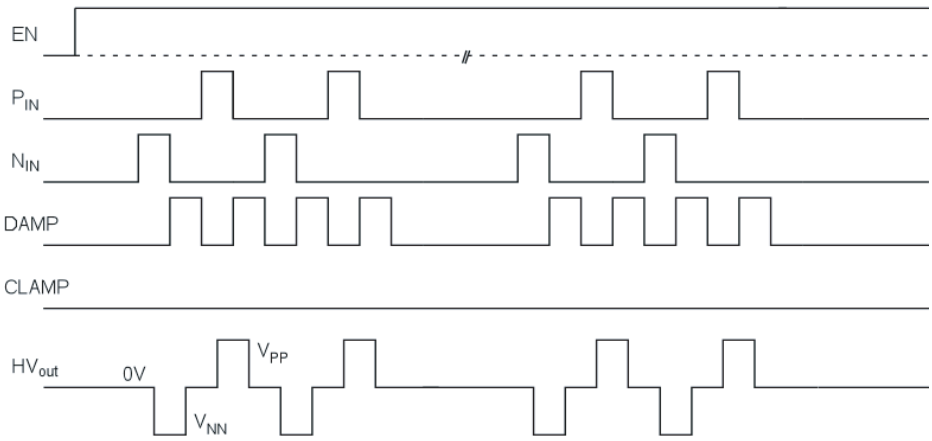


Demo Waveform C: RZ Pulses with Use of Damp

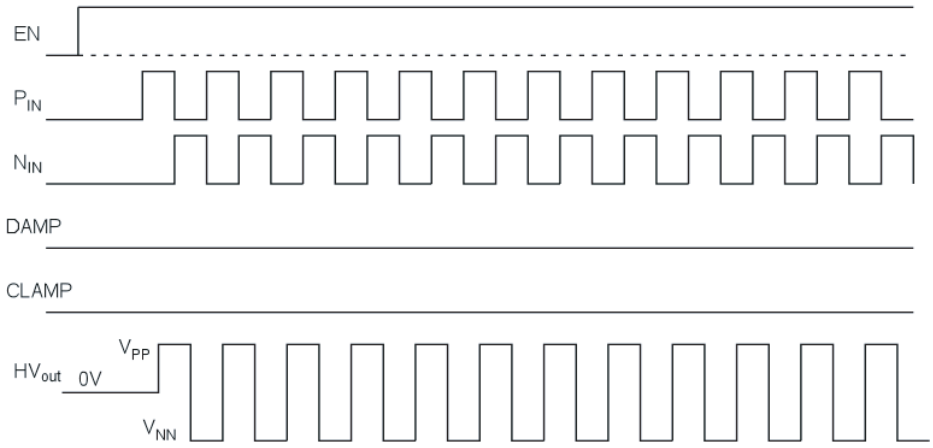


Input and Output Waveform Examples *(cont.)*

Demo Waveform D: RZ Pulses with Use of Damp



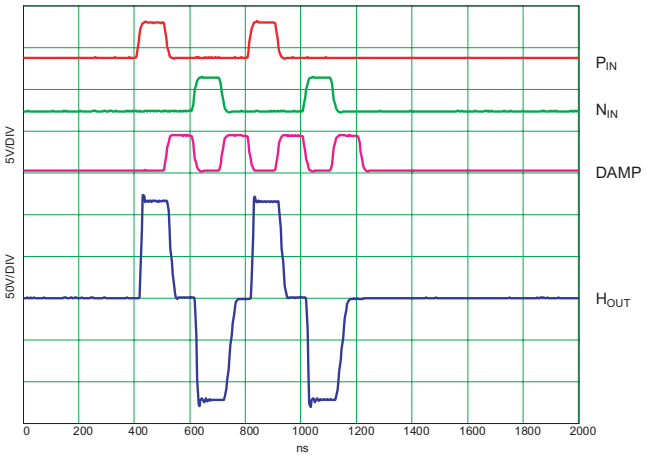
Demo Waveform E: CW Pulses



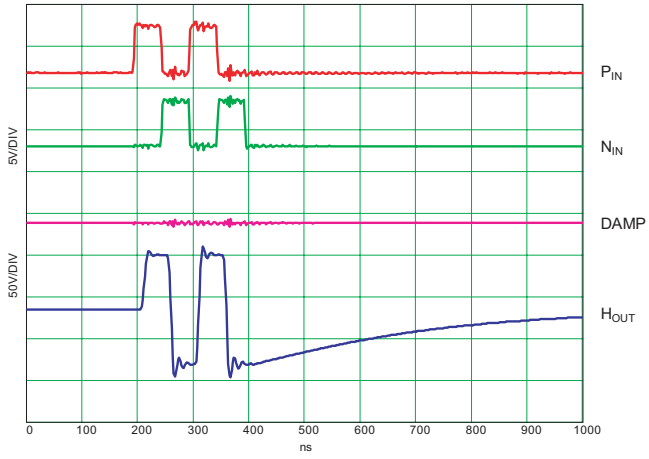
Note: The duty cycle of CW or PW burst is set to about 0.1% for the power dissipation limit of the load resistor.

Pulser Oscilloscope Waveforms

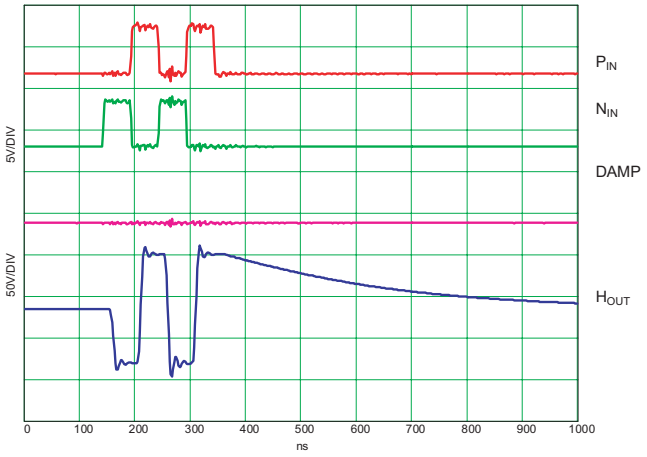
HV732-DB1 Waveform with 220PF//1k Load



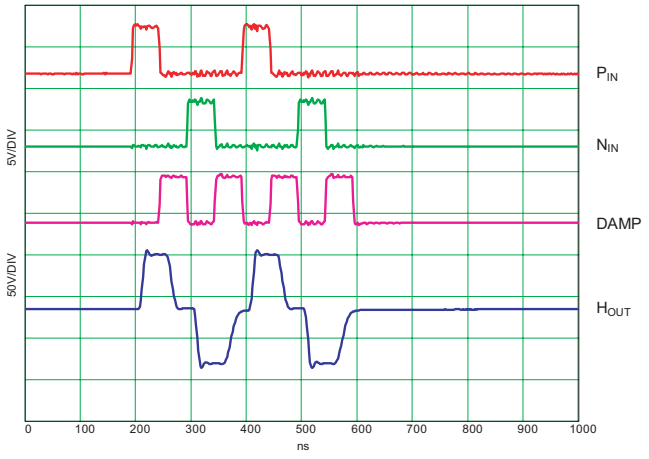
HV732-DB1 Waveform A with 220PF//1k Load



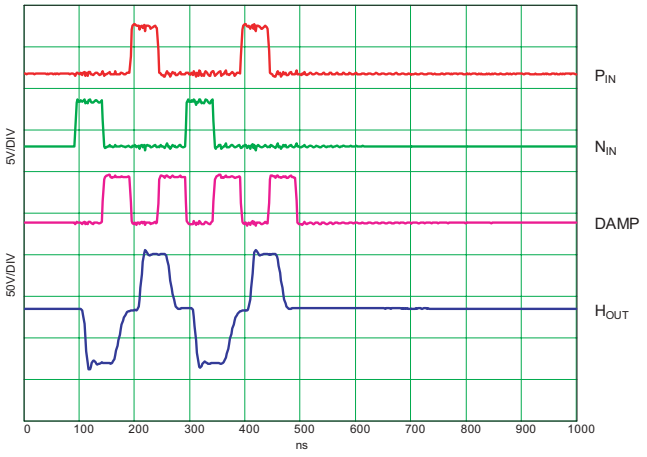
HV732-DB1 Waveform B with 220PF//1k Load



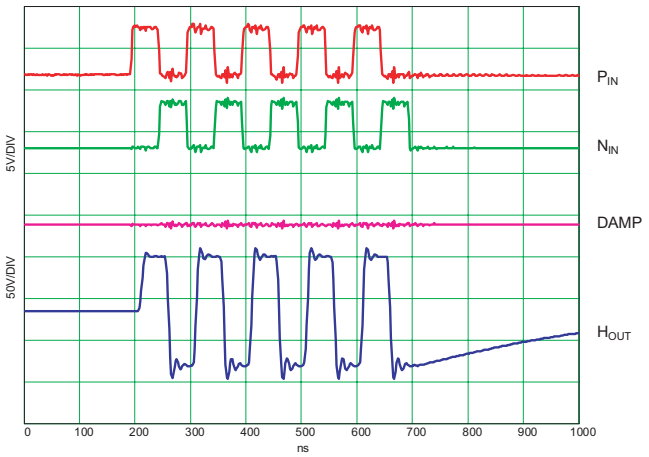
HV732-DB1 Waveform C with 220PF//1k Load



HV732-DB1 Waveform D with 220PF//1k Load

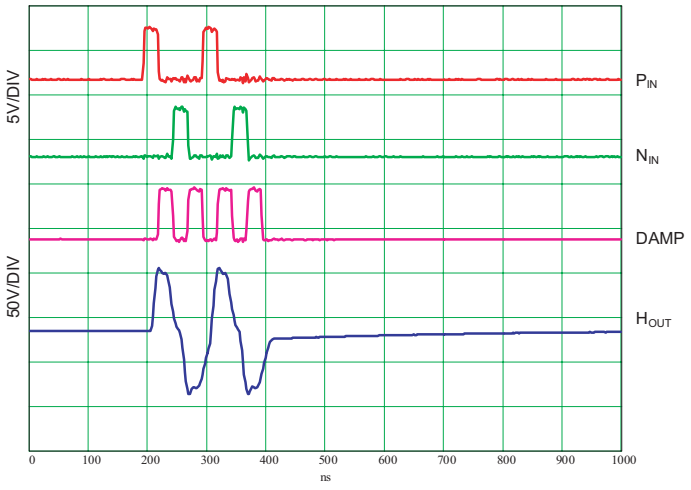


HV732-DB1 Waveform E with 220PF//1k Load

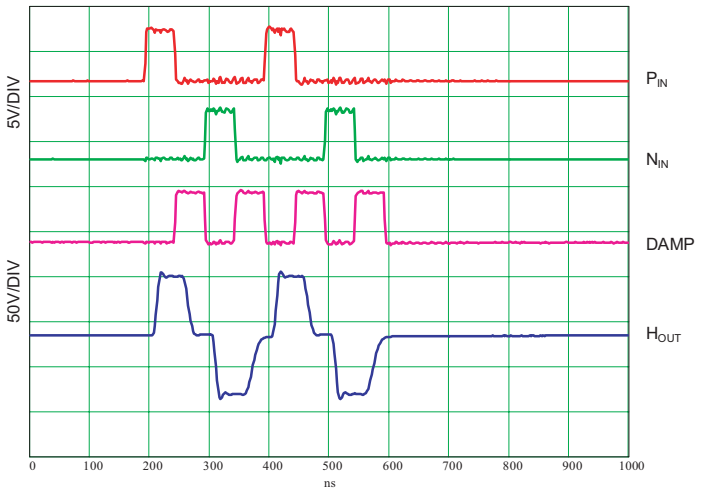


Pulser Oscilloscope Waveforms *(cont.)*

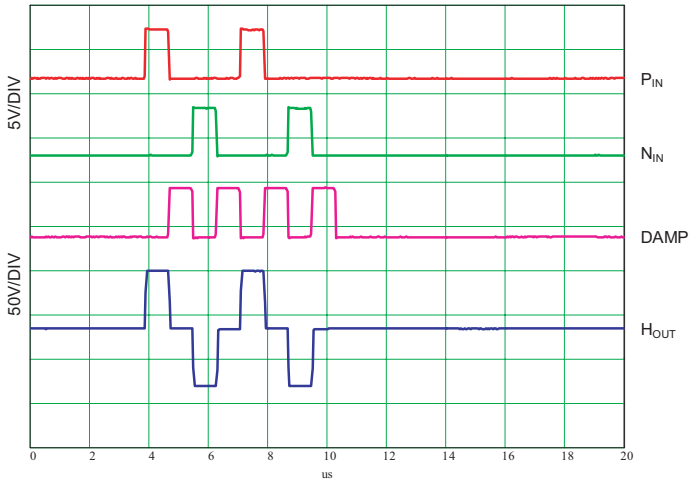
HV732-DB1 Waveform C at 20MHz,220PF//1k



HV732-DB1 Waveform C at 10MHz,220PF//1k



HV732-DB1 Waveform C 625KHz 220PF/1k



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