Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS MEMORY DRIVERS

ADVANCE INFORMATION
IDT54/74FBT2240
IDT54/74FBT2240A
IDT54/74FBT2240C

FEATURES:

- IDT54/74FBT2240 equivalent to the 54/74BCT2240
- **IDT54/74FBT2240A 25% faster than the 2240**
- **IDT54/74FBT2240C 10% faster than the 2240A**
- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

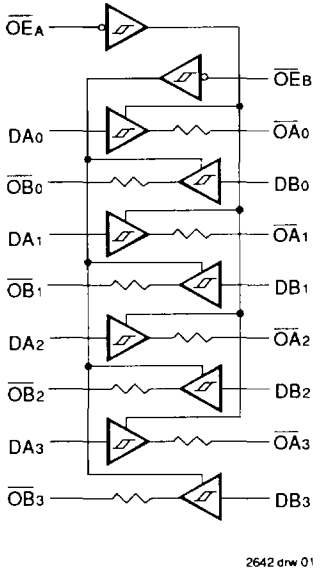
DESCRIPTION:

The FBT series of BiCMOS Memory Drivers is built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2240 series are octal buffers/line drivers where each output is terminated with a 25Ω series resistor.

The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection. This higher output level in the high state will result in a significant reduction in overall system power dissipation.

FUNCTIONAL BLOCK DIAGRAM



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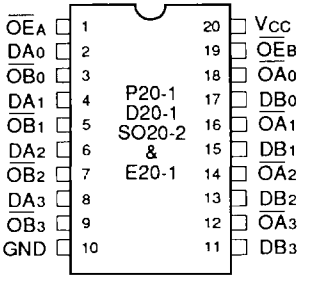
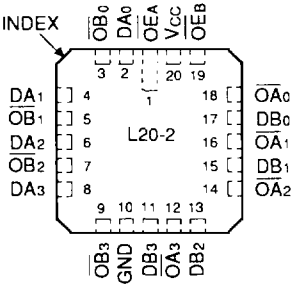
PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

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PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
D_0-D_7	Inputs
$\overline{O}_0$-$\overline{O}_7$	Outputs

2642 tbl 01

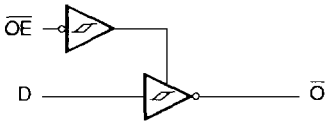
FUNCTION TABLE[1]

Inputs		Output
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	H
L	H	L
H	X	Z

NOTE: 2642 tbl 02

1 H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

LOGIC SYMBOL



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ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	•0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2642 tbl 03

1 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2642 tbl 04

1 This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = -18mA		—	-0.7	-1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2V		-35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2V		50	—	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-60	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = -1mA	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA	2.0	3.0	—	
V_{OL}	Output LOW Voltage		I_{OL} = 1mA	—	0.15	0.5	V
			I_{OL} = 12mA	—	0.35	0.8	
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2642 tbl 05

NOTES:
1 For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2 Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3 Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	6.5[5]	
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	14.5[5]	

NOTES:

2642 tbl 06

1. For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FBT2240				IDT54/74FBT2240A				IDT54/74FBT2240C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	C_L = 50pF R_L = 500Ω	1.5	5.7	—	—	—	—	—	—	—	—	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	9.3	—	—	—	—	—	—	—	—	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	8.7	—	—	—	—	—	—	—	—	—	—	ns

NOTES:

2642 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

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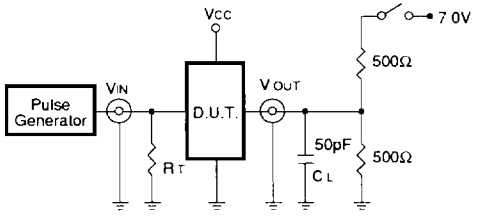
TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



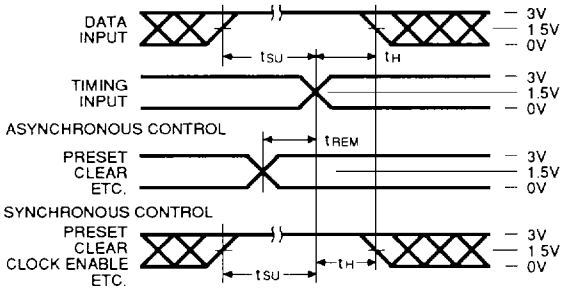
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

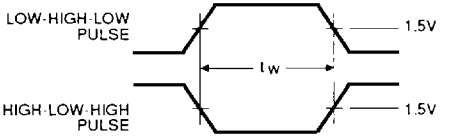
DEFINITIONS: 2642 tbl 05

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

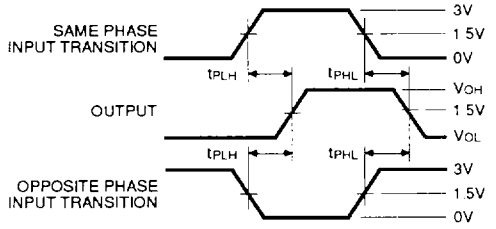
SET-UP, HOLD AND RELEASE TIMES



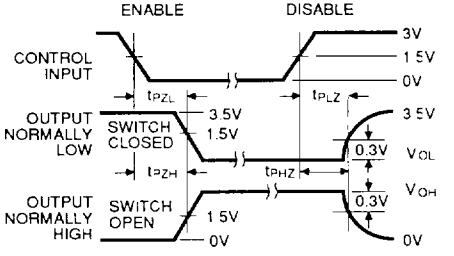
PULSE WIDTH



PROPAGATION DELAY



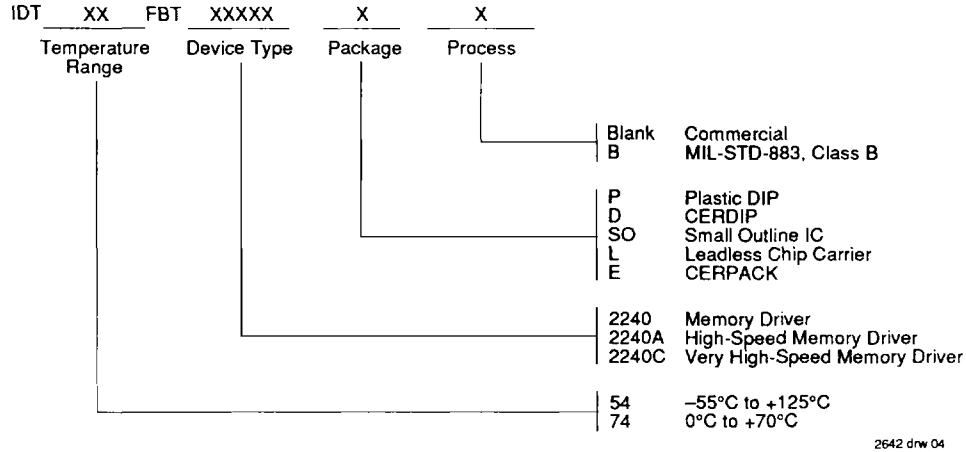
ENABLE AND DISABLE TIMES



NOTES 2642 drw 05

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz, Z_O ≤ 50Ω, t_F ≤ 2.5ns, t_R ≤ 2.5ns

ORDERING INFORMATION



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