SIEMENS

SAB 80512/80532
8-Bit Single-Chip Microcontroller

SAB 80512	Microcontroller with factory-mask programmable ROM
SAB 80532	Microcontroller for external ROM
SAB 80512-T40/85	Extended temperature range: −40°C to +85°C
SAB 80532-T40/85	Extended temperature range: −40°C to +85°C

- 4K × 8 ROM (SAB 80512 only)
- 128 × 8 RAM
- Backwardly Compatible with SAB 8051A/ 8031A
- Seven 8-Bit Ports
- Two 16-Bit Timers/Event Counters
- High-Performance Full Duplex Serial Channel with Own Baud Rate Generator
- 8-Bit A/D Converter with Eight Multiplexed Inputs, Reference Voltages Externally Adjustable
- Six Interrupt Sources (2 External, 4 Internal), Two Priority Levels Programmable
- Boolean Processor
- 1 µs Instruction Cycle Time (at 12 MHz Osc. Frequency)
- 4 µs Multiply and Divide (at 12 MHz Osc. Frequency)
- External Program and Data Memory Expandable up to 64 Kbyte Each
- PLCC 68 Package

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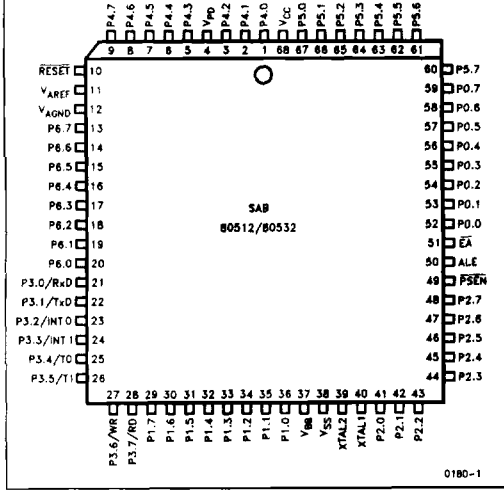
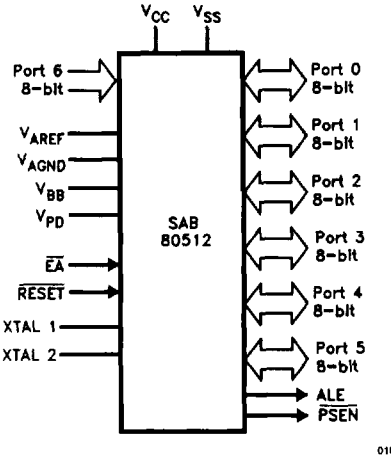
Pin Configuration



Logic Symbol



The SAB 80512/80532 is a new member of the Siemens SAB 8051 family of 8-bit microcontrollers. Maintaining all features of the SAB 8051A/8031A, it is fully backwardly compatible with the SAB 8051A/8031A. Furthermore the SAB 80512/80532 incorporates several enhancements that significantly increase design flexibility and cost effectiveness. In addition to the SAB 8051A/8031A the SAB 80512/80532 contains an 8-bit A/D converter with 8 multiplexed inputs (these inputs can also be used as digital inputs), an own baud rate generator for the serial interface and two more I/O ports. The SAB 80532 is identical with the SAB 80512, except that it lacks the on-chip ROM.

The SAB 80512/80532 is fabricated in +5V advanced N-channel, silicon gate MYMOS technology of Siemens and supplied in a PLCC 68 package. For the industrial temperature range −40°C to +85°C, the SAB 80512/80532-T40/85 is available.

Pin Definitions and Functions

Pin	Symbol	Input (I) Output (O)	Function
1-3, 5-9	P4.0-P4.7	I/O	Port 4 is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 4 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors.
4	V_{PD}		Power down supply voltage. If V_{PD} is held within its specifications while V_{CC} drops below the specification, V_{PD} will provide standby power to 40 byte of internal RAM (addr. 58H to 7FH). During normal operation of the SAB 80512, the RAM's current is supplied by V_{CC}, when V_{PD} is low.
10	$\overline{\text{RESET}}$	I	A low level on this pin for the duration of two machine cycles while the oscillator is running resets the SAB 80512. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
11	V_{AREF}		Reference voltage for the A/D converter.
12	V_{AGND}		Reference ground for the A/D converter.
13-20	P6.7-P6.0	I	Port 6, 8-bit unidirectional input port. Port pins can be used for digital input if voltage levels meet the specified input high/low voltages and for the eight multiplexed analog inputs of the A/D converter, simultaneously.
21-28	P3.0-P3.7	I/O	Port 3 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs port 3 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. It also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding

Pin Definitions and Functions (Continued)

Pin	Symbol	Input (I) Output (O)	Function
21–28	P3.0–P3.7	I/O	to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: —RxD (P3.0): serial port's receiver data input (asynchronous) or data input/output (synchronous) —TxD (P3.1): serial port's transmitter data output (asynchronous) or clock output (synchronous) —$\overline{INT0}$ (P3.2): interrupt 0 input/timer 0 gate control input —$\overline{INT1}$ (P3.3): interrupt 1 input/timer 1 gate control —T0 (P3.4): counter 0 input —T1 (P3.5): counter 1 input —$\overline{WR}$ (P3.6): the write control signal latches the data byte from port 0 into the external data memory —$\overline{RD}$ (P3.7): the read control signal enables the external data memory to port 0
29–36	P1.7–P1.0	I/O	Port 1 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs port 1 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. The port is also used for the low order address byte during program verification.
37	V_{BB}		Substrate pin. Must be connected to V_{SS} with a capacitor (47 nF to 100 nF) for proper operation of the A/D converter.
39 40	XTAL2 XTAL1		XTAL2 Output of the inverting oscillator amplifier. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is pulled low. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times specified in the AC characteristics must be observed: XTAL1 Input to the inverting oscillator amplifier. Required when a crystal or ceramic resonator is used.
41–48	P2.0–P2.7	I/O	Port 2 is an 8-bit bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs port 2 pins being externally pulled low will source current (I_{IL}, on the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), port 2 issues the contents of the P2 special function register.
49	$\overline{PSEN}$	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.
50	ALE	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.

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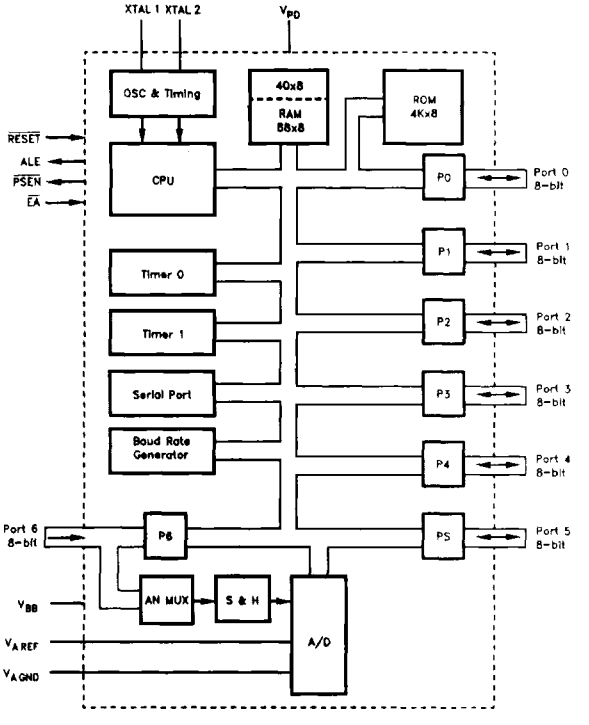
Pin Definitions and Functions (Continued)

Pin	Symbol	Input (I) Output (O)	Function
51	$\overline{EA}$	I	When held at a TTL high level, the SAB 80512 executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the SAB 80512 fetches all instructions from external program memory. For the SAB 80532 this pin must be tied low.
52–59	P0.0–P0.7	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1s. Port 0 also outputs the code bytes during program verification. External pullup resistors are required during program verification.
60–67	P5.7–P5.0	I/O	Port 5 is an 8-bit bidirectional I/O Port with internal pullup resistors. Port 5 pins that have 1s written to them are pulled high by the internal pullup registers, and in that state can be used as inputs. As inputs Port 5 pins being externally pulled low will source current (I_{IL}, on the DC Characteristics) because of the internal pullup resistors.
68	V_{CC}		Supply voltage during normal operation and program verification.
38	V_{SS}		Ground (0V)

Block Diagram



Functional Description

The SAB 80512/80532 is based on the architecture of the SAB 8051 microcontroller family. The SAB 80512 includes all features of the SAB 8051 and additionally offers peripheral extensions in three items:

— bit A/D converter with adjustable reference voltages

— two more ports

— dedicated baud rate generator

Different to the SAB 8051 is the inverted reset-input and the RAM power-down supply by a special pin (V_{PD}), which supplies 40 byte with a typical current of 2 mA. Beside the upward compatibilty to the SAB 8051 (all SAB 8051 software runs on the SAB 80512 without any changes) the SAB 80512 is also downward compatible to the SAB 80515. The SAB 80512 is packed into the PLCC 68 package and has the same pinning as the SAB 80515.

A/D Converter

The 8-bit A/D converter of the SAB 80512 has 8 multiplexed analog inputs and is using the successive approximation method. The sampling of an analog signal takes 5 machine cycles, the total conversion time is 15 machine cycles (15 μs at 12 MHz oscillator frequency). Conversion can be programmed to be single or continuous, at the end of a conversion an interrupt can be generated. The SAB 80512 provides variable external reference voltages V_{AGND} and V_{AREF} adjustable in a wide range. A compressed reference voltage range allows to increase the resolution of the converted analog input.

The lower reference voltage (V_{AGND}) can be varied within V_{SS} − 0.2V and 4V, the higher (V_{AREF}) within 1V and V_{CC} +5%. For proper operation of the A/D converter a minimum of 1V difference is required between the external voltages:

$$(V_{SS} - 0.2V) \leq V_{AGND} \leq (V_{AREF} - 1V)$$
$$(V_{AGND} + 1V) \leq V_{AREF} \leq (V_{CC} + 5\%)$$

Special Function Register

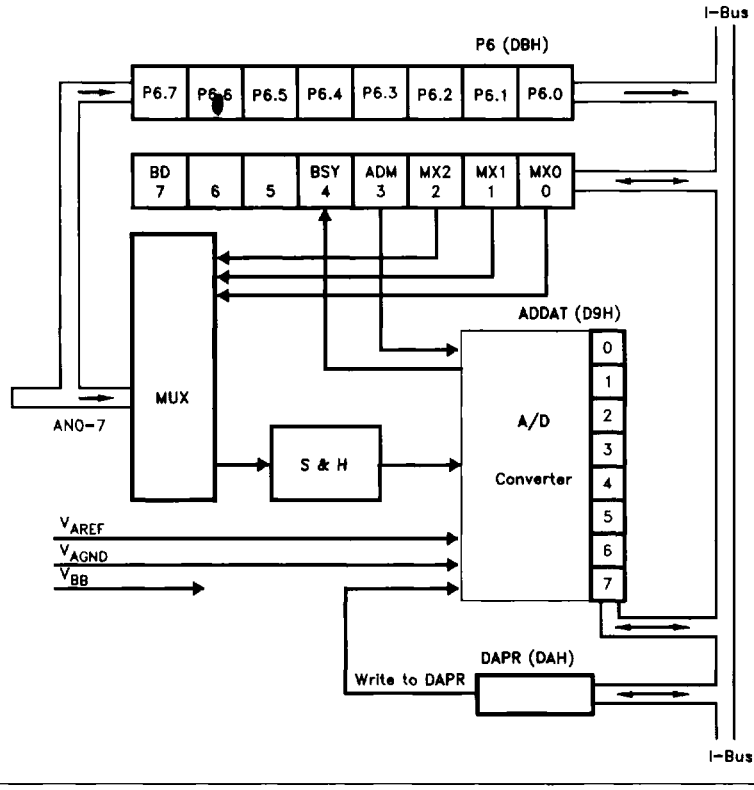
All registers, except the program counter and the four 8-register banks, reside in the special function register area. The 28 special function registers (SFRs) include arithmetic registers, pointers, and registers that provide an interface between the CPU and the on-chip peripheral functions. There are also 128 directly addressable bits within the SFR area.

I/O Ports

The SAB 80512 has six 8-bit I/O ports and one 8-bit input port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 5 are quasi-bidirectional I/O ports with internal pullups. That means, when configured as inputs, ports 1 to 5 will pull high and will source current when externally pulled low. Port 0 will float when configured as input. Port 6 is an input port only and can be used as digital input port, if the values meet the specified high/low voltages and as analog input for the A/D-converter.

Port 0 and port 2 can be used to expand the program and data memory externally. During an access to external memory, port 0 emits the low-order address byte. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.

Block Diagram of A/D Converter



Special Function Registers

Address	Symbol	Name	Bit-Addressable
80H	P0	Port 0 Register	Yes
81H	SP	Stack Pointer	
82H	DPL	Data Pointer, Low-Byte	
83H	DPH	Data Pointer, High-Byte	
87H	PCON	Power Control Register	
88H	TCON	Timer Control Register	Yes
89H	TMOD	Timer Mode Register	
8AH	TL0	Timer 0, Low-Byte	
8BH	TL1	Timer 1, Low-Byte	
8CH	TH0	Timer 0, High-Byte	
8DH	TH1	Timer 1, High-Byte	
90H	P1	Port 1 Register	Yes
98H	SCON	Serial Port Control Register	Yes
99H	SBUF	Serial Port Buffer Register	
0A0H	P2	Port 2 Register	Yes
0A8H	IE	Interrupt Enable Register	Yes
0B0H	P3	Port 3 Register	Yes
0B8H	IP	Interrupt Priority Register	Yes
0C0H	IRCON	Interrupt Request Control	Yes
0D0H	PSW	Program Status Word Register	Yes
0D8H	ADCON	A/D Converter Control Register	Yes
0D9H	ADDAT	A/D Converter Data Register	
0DAH	DAPR	D/A Converter Start Register	
0DBH	P6	Port 6 Register	
0E0H	ACC	Accumulator Register	Yes
0E8H	P4	Port 4 Register	Yes
0F0H	B	B-Register	Yes
0F8H	P5	Port 5 Register	Yes

Absolute Maximum Ratings*

Temperature under Bias
for the SAB 80512/80532 ..... 0°C to +70°C
for the SAB 80512/
80532-T40/85 ..... −40°C to +85°C

Storage Temperature ..... −65°C to +150°C

Voltage on any Pin with
Respect to Ground (v_{SS}) ..... −0.5V to +7V

Power Dissipation 2W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5V ±10%; V_{SS} = 0V; T_A = 0 to 70°C for SAB 80512/80532; T_A = −40°C to +85°C for SAB 80512/80532-T40/85

Parameter	Symbol	Test Conditions	Limit Values		Unit
			Min	Max	
Input Low Voltage	V_{IL}		0.5	0.8	V
Input High Voltage (Except $\overline{RESET}$ and XTAL2)	V_{IH}		2.0	V_{CC} + 0,5	V
Input High Voltage to XTAL2	V_{IH1}	XTAL1 to V_{SS}	2.5	V_{CC} + 0.5	V
Input High Voltage to $\overline{RESET}$	V_{IH2}		3.0		V
Power-Down Voltage	V_{PD}	V_{CC} = 0V	3	5.5	V
Output Low Voltage, Ports 1, 2, 3, 4, 5	V_{OL}	I_{OL} = 1.6 mA		0.45	V
Output Low Voltage, Port 0, ALE, $\overline{PSEN}$	V_{OL1}	I_{OL} = 3.2 mA		0.45	V
Output High Voltage, Ports 1, 2, 3, 4, 5	V_{OH}	I_{OH} = −80 µA	2.4		V
Output High Voltage, Port 0, ALE, $\overline{PSEN}$	V_{OH1}	I_{OH} = −400 µA	2.4		V
Logic 0 Input Current, Ports 1, 2, 3, 4, 5	I_{IL}	V_{IL} = 0.45V		-500	µA
Logic 0 Input Current, XTAL2	I_{IL2}	XTAL = V_{SS}, V_{IL} = 0.45V		-2.5	mA
Input Low Current to $\overline{RESET}$ for Reset	I_{IL3}	V_{IL} = 0.45V		-500	µA
Input Leakage Current to Port 0, $\overline{EA}$	I_{LI}	0V < V_{IN} < V_{CC}		±10	µA
Power Supply Current SAB 80512/80532 SAB 80512/80532-T40/85	I_{CC}	All Outputs Disconnected		175	mA
Power-Down Current	I_{PD}	V_{CC} = 0V		3	mA
Capacitance of I/O Buffer	C_{IO}	f_c = 1 MHz		10	pF

A/D Converter Characteristics

V_{CC} = 5V ±10%; V_{SS} = 0V; (V_{SS} − 0.2V) ≤ V_{AGND} ≤ (V_{AREF} − 1V); (V_{AGND} + 1V) ≤ V_{AREF} ≤ (V_{CC} +5%); T_A = 0°C to 70°C for SAB 80512/80532; T_A = −40°C to +85°C for SAB 80512/80532-T40/85

Parameter	Symbol	Test Conditions	Limit Values			Unit
			Min	Typ	Max	
Analog Input Voltage	V_{AINPUT}		V_{AGND} −0.2		V_{AREF} +0.2	V
Analog Input Capacitance(1)	C_I			25	70	pF
Load Time	t_L				2 t_{CY}	µs
Sample Time (Incl. Load Time)	t_S				5 t_{CY}	µs
Conversion Time (Incl. Sample Time)	t_C				15 t_{CY}	µs
Differential Non-Linearity	DNLE	V_{AREF} = V_{CC} V_{AGND} = V_{SS}		±¼	±½	LSB
Integral Non-Linearity	INLE			±¼	±½	
Offset Error				±¼	±½	
Gain Error				±¼	±½	
Total Unadjusted Error	TUE			±¼	±½	
V_{AREF} Supply Current(2)	I_{REF}				5	mA

NOTES:
1. The internal resistance of the analog source must be low enough to assure full loading of the sample capacitance (C_I) during load time (t_L). After charging of the internal capacitance (C_I) in the load time (t_L) the analog input must be held constant for the rest of the sample time (t_S).
2. The differential impedance r_D of the analog reference voltage source must be less than 1 kΩ at reference supply voltage.

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AC Characteristics

V_{CC} = 5V ±10%; V_{SS} = 0V; T_A = 0°C to 70°C for SAB 80512/80532; T_A = −40°C to +85°C for SAB 80512/80532-T40/85; (C_L for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; C_L for All Outputs = 80 pF)

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		Min	Max	Min	Max	
Program Memory Charactistics						
Cycle Time	t_{CY}	1000		12 t_{CLCL}		ns
ALE Pulse Width	t_{LHLL}	127		2 t_{CLCL} − 40		ns
Address Setup to ALE	t_{AVLL}	53		t_{CLCL} − 30		ns
Address Hold after ALE	t_{LLAX1}	48		t_{CLCL} − 35		ns
Address to Valid Instr In	t_{LLIV}		233		4 t_{CLCL} − 100	ns
ALE to $\overline{PSEN}$	t_{LLPL}	58		t_{CLCL} − 25		ns
$\overline{PSEN}$ Pulse Width	t_{PLPH}	215		3 t_{CLCL} − 35		ns
$\overline{PSEN}$ to Valid Instr In	t_{PLIV}		150		3 t_{CLCL} − 100	ns
Input Instruction Hold after $\overline{PSEN}$	t_{PXIX}	0		0		ns
Input Instruction Float after $\overline{PSEN}$	t_{PXIZ}*		63		t_{CLCL} − 20	ns
Address Valid after $\overline{PSEN}$	t_{PXAV}*	75		t_{CLCL} − 8		ns
Address to Valid Instr In	t_{AVIV}		302		5 t_{CLCL} − 115	ns
Address Float to $\overline{PSEN}$	t_{AZPL}	0		0		ns
External Data Memory Characteristics						
$\overline{RD}$ Pulse Width	t_{RLRH}	400		6 t_{CLCL} − 100		ns
$\overline{WR}$ Pulse Width	t_{WLWH}	400		6 t_{CLCL} − 100		ns
Address Hold after ALE	t_{LLAX2}	132		2 t_{CLCL} − 35		ns
$\overline{RD}$ to Valid Data In	t_{RLDV}		250		5 t_{CLCL} − 165	ns
Data Hold after $\overline{RD}$	t_{RHDX}	0		0		ns
Data Float after $\overline{RD}$	t_{RHDZ}		97		2 t_{CLCL} − 70	ns
ALE to Valid Data In	t_{LLDV}		517		8 t_{CLCL} − 150	ns
Address to Valid Data In	t_{AVDV}		585		9 t_{CLCL} − 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	3 t_{CLCL} − 50	3 t_{CLCL} + 50	ns
Address to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203		4 t_{CLCL} − 130		ns
$\overline{WR}$ or $\overline{RD}$ High to ALE High	t_{WHLH}	43	123	t_{CLCL} − 40	t_{CLCL} + 40	ns
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	33		t_{CLCL} − 50		ns
Data Setup before $\overline{WR}$	t_{QVWH}	433		7 t_{CLCL} − 150		ns
Data Hold after $\overline{WR}$	t_{WHQX}	33		t_{CLCL} − 50		ns
Address Float after $\overline{RD}$	t_{RLAZ}		0		0	ns

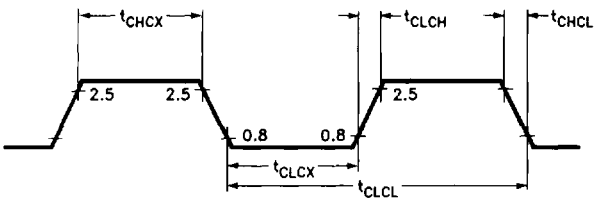
* Interfacing the SAB 80512 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (Continued)

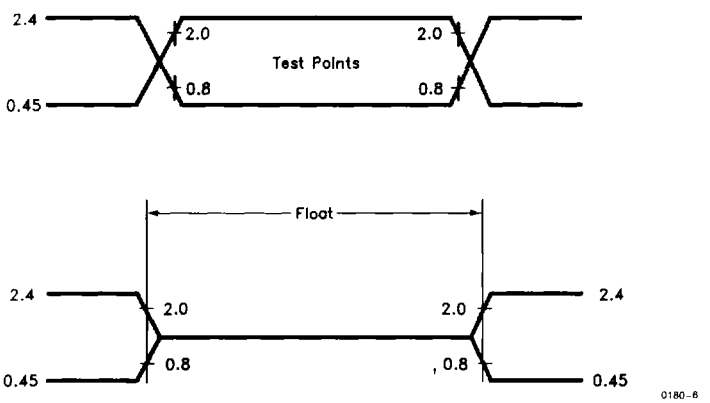
External Clock Drive XTAL2

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 1.2 MHz to 12 MHz		
		Min	Max	
Oscillator Period	t_{CLCL}	83.3	833.3	ns
High Time	t_{CHCX}	20	t_{CLCL}-t_{CLCX}	ns
Low Time	t_{CLCK}	20	t_{CLCL}-t_{CHCX}	ns
Rise Time	t_{CLCH}		20	ns
Fall Time	t_{CHCL}		20	ns

External Clock Cycle



AC Testing Input, Output, Float Waveforms



AC Testing inputs are driven at 2.4V for a logic "1" and at 0.45V for a logic "0".
Timing measurements are made at 2.0V for a logic "1" and at 0.8V for a logic "0".
For timing purposes, the float state is defined as the point where a P0 pin sinks 3.2 mA or sources 400 μA at voltage test levels.

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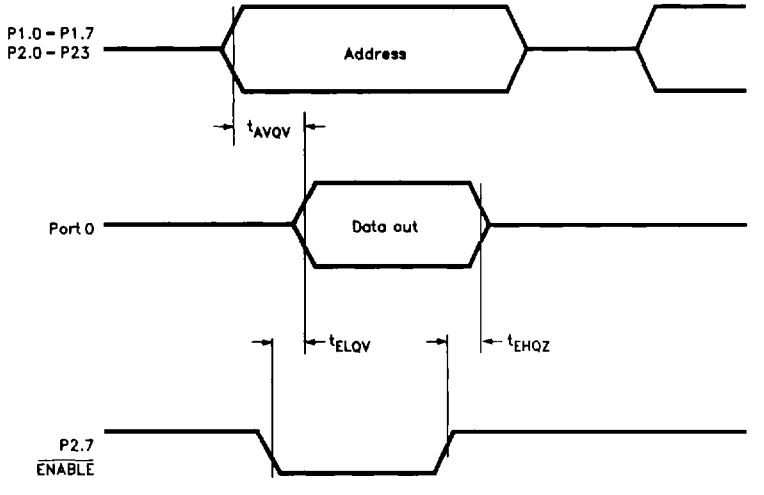
ROM Verification Characteristics $T_A = 25°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$

Parameter	Symbol	Limit Values		Unit
		Min	Max	
Address to Valid Data	t_{AVQV}		48 t_{CLCL}	ns
ENABLE to Valid Data	t_{ELQV}		48 t_{CLCL}	ns
Data Float after ENABLE	t_{EHQZ}	0	48 t_{CLCL}	ns
Oscillator Frequency	$1/t_{CLCL}$	4	6	MHz

ROM Verification

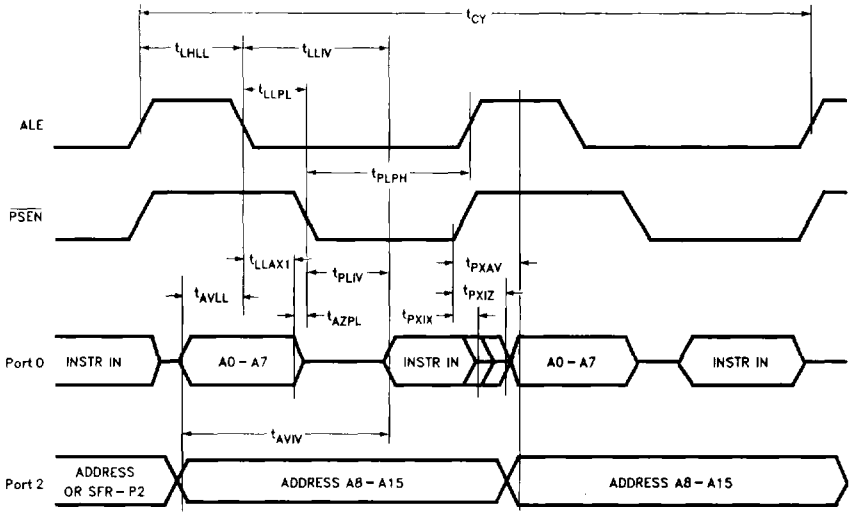


Address: P1.0–P1.7 = A0–A7
P2.0–P2.3 = A8–A11
Data: Port 0 = D0–D7

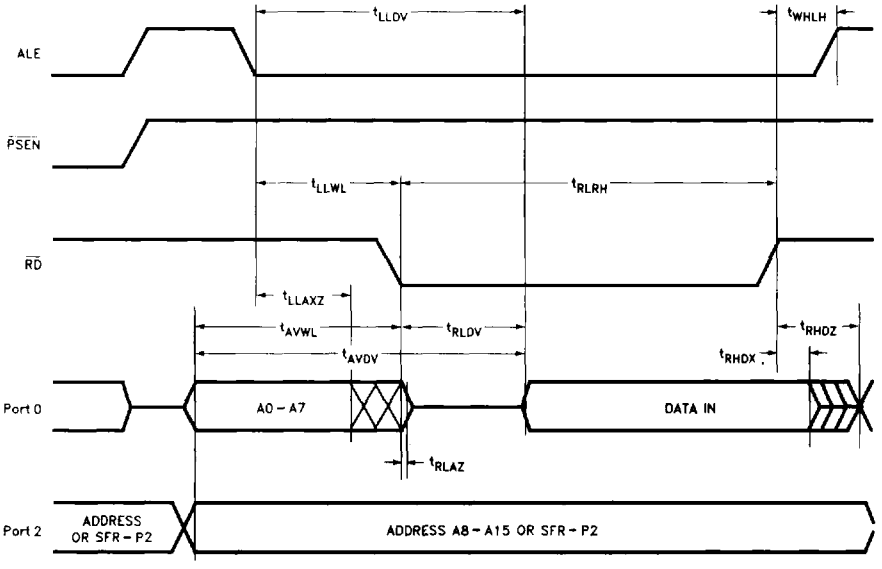
Inputs: P2.4–P2.6, $\overline{PSEN}$ = V_{SS}
ALE, $\overline{EA}$ = V_{IH}
$\overline{RESET}$ = V_{IL}

Waveforms

Program Memory Read Cycle



Data Memory Read Cycle



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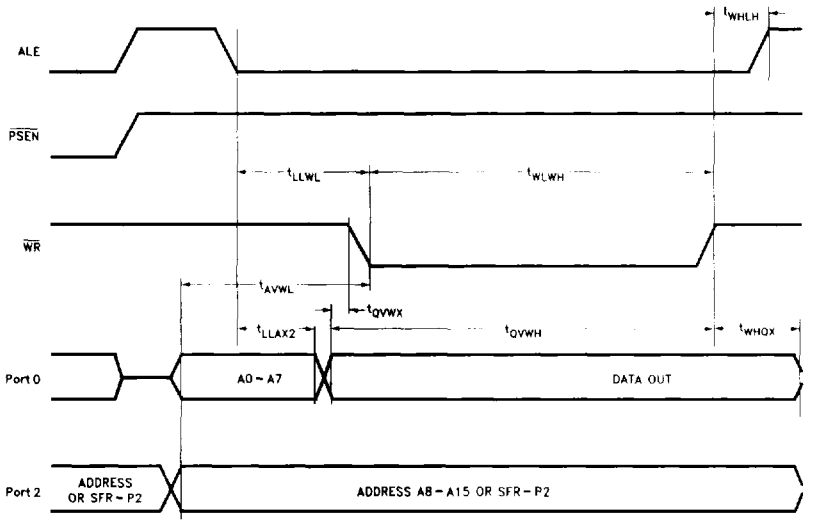
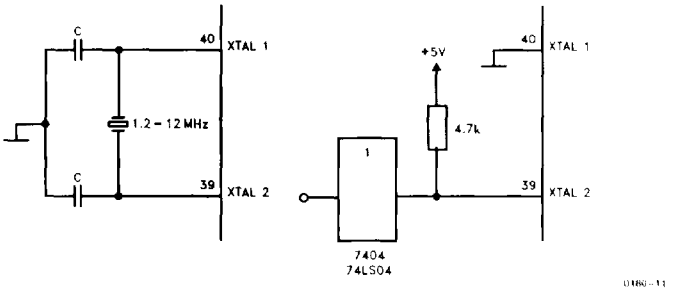
Data Memory Write Cycle



Recommended Oscillator Circuits



C = 30 pF ± 10 pF

Crystal Oscillator Mode

Driving from External Source

Ordering Information

Type	Function
SAB 80512	8-Bit Single-Chip Microcontroller with ROM
SAB 80532	8-Bit Single-Chip Microcontroller for External ROM
SAB 80512-T40/85	Like SAB 80512 but for – 40°C to + 85°C
SAB 80532-T40/85	Like SAB 80532 but for – 40°C to + 85°C