SPARC Technology Business

Preliminary

STP1012A

June 1995

microSPARC™-II

DATA SHEET Highly Integrated 32-Bit RISC Microprocessor

DESCRIPTION

The microSPARC-II 32-bit microprocessor is a highly integrated, high-performance microprocessor. Implementing the SPARC Architecture v8 specification, it is ideally suited for low-cost uniprocessor applications.

It is built with leading edge CMOS technology, featuring 0.5 micron geometries, 3-layer metal silicon process, with the core operating at low voltage for optimized power consumption.

The microSPARC-II includes on chip: Integer Unit (IU), Floating Point Unit (FPU), large separate Instruction and Data Caches, v8 Reference MMU, Programmable DRAM controller, SBus Controller, Graphics Interface support, Internal and Boundary Scan through JTAG Interface, Power Management and Clock Generation capabilities.

Taking advantage of optimized Compiler technology, impressive performance is achieved executing industry standard benchmarks. Running with the internal CPU-clock at 85 MHz, throughput has been measured above 64 SPECint92 and 54 SPECfp92.

Features

- SPARC High Performance RISC architecture
- Operating Frequency up to 85 MHz
- 8 window, 136-word register file
- 16 Kbyte Instruction cache, 8 Kbyte Data cache
- On-chip Memory Management Unit
- Optimized Integrated Floating-Point Unit
- Interface to S-Bus at 1/3, 1/4, 1/5 system clock
- Integrated DRAM controller
- On-chip Local Bus Controller (graphics)
- IEEE1149.1 (JTAG) boundary scan test bus
- 321-pin Ceramic PGA package

Benefits

- Compatible with 9400 SPARC applications and development tools
- 85 MIPs peak performance, 110 KDhrystone
- Fast interrupt response, procedure calls and program execution
- Decouples processor operation from slow external memory
- Support for sophisticated operating systems with memory protection and virtual addressing
- 18 MFlops peak performance
- Connection to industry standard expansion bus
- Simple, low part count system design
- High-performance graphics with minimum part count
- Ease of manufacturing test
- Small footprint package with high thermal efficiency

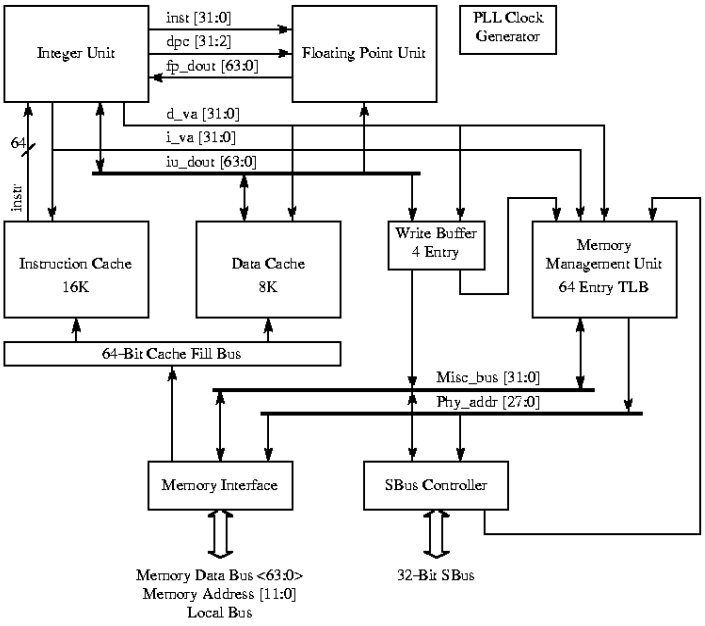


Figure 1. microSPARC–II Block Diagram

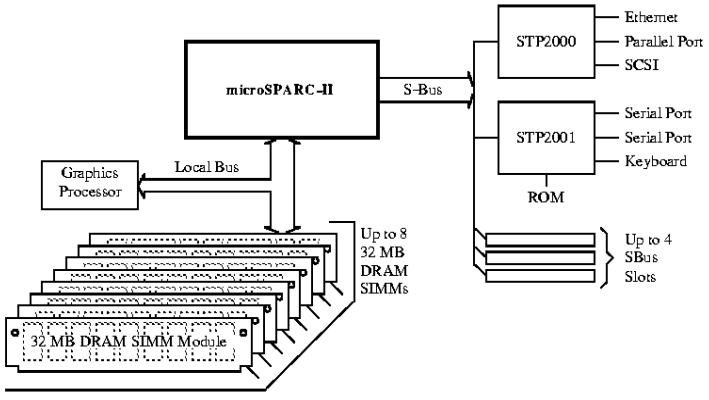


Figure 2. Typical microSPARC–II System Block Diagram

TECHNICAL OVERVIEW

Integer Unit (IU)

The STP1012A Integer Unit executes SPARC integer instructions defined in the SPARC Architecture Manual (Version 8). The IU contains 136 registers (8-window registers and 8-global registers) and operates on prefetched instructions using a five-stage pipeline.

The throughput is improved by using Branch folding and single cycle Load/Store instructions.

Floating Point Unit (FPU)

The FPU (based on Meiko design) fully executes all single and double precision FP instructions as defined in the SPARC Architecture Manual (Version 8). Quad-precision instructions trap and are implemented in software. The FPU contains 32x32 *f*registers, a general purpose execution unit and an FP multiplier allowing in most cases the parallel execution of an FPMUL and another FP instruction. A 3-instruction deep queue of FP instructions is provided to increase the efficiency of concurrent FP and integer execution.

Memory Management Unit (MMU)

The microSPARC-II MMU translates 32-bit virtual addresses of each running process to 31-bit physical addresses in memory. The 3 high-order bits of physical address are maintained to support memory mapping into 8 different address spaces.

It also serves as an I/O MMU and controls the arbitration between I/O, Data Cache, Instruction Cache, and TLB references to memory.

The MMU contains a 64-entry fully associative TLB and is compatible with the SPARC v8 Reference MMU. It supports 256 contexts and protects memory so that a process can be prohibited from reading or writing to the address space of another process.

Instruction Cache

The instruction Cache is a 16-KByte, direct mapped, virtually indexed, virtually tagged cache. The Instruction Cache data is organized as 512 lines of 32 bytes plus 32 tag bits. Cache refill is done two 32-bit words at a time and cache streaming and bypass are supported.

Data Cache

The Data Cache is an 8-KByte, direct mapped, virtually indexed, virtually tagged, write through cache with no write allocate. The data store is organized as 512 lines of 16 bytes plus 32 tag bits.

Single word Integer and double world FP read and write cache hits take only 1 clock cycle.

There is a 4-deep Store Buffer to hold data being stored from the IU or FPU to memory or other physical devices. The Store Buffers are 64-bit registers.

Cache refill is done 2 32-bit words at a time and cache streaming and bypass are supported.

Memory Interface

The STP1012A provides a complete DRAM controller which generates all the signals necessary to support up to 256 MBytes of system memory.

The DRAM bus is 64 bits wide with two parity bits, one covering each 32 bits of data.

The system DRAM is organized as eight banks, each of which may be 2 MBytes, 8 MBytes, or 32 MBytes depending upon the size of DRAM used.

The STP1012A RAM Refresh Control logic provides complete DRAM Refresh Control. This Refresh Controller performs $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh. Refresh interval is programmable and self-refreshed DRAMs are also supported.

SBus Interface

The SBus Interface performs all functions necessary to connect the STP1012A to the SBus, including dynamic bus sizing, cycle re-run control, burst cycle re-ordering, arbitration, and general SBus control.

It controls SBus devices sharing the bus, supporting:

- Programmed Input/Output (PIO) transactions between the CPU and SBus devices.
- Direct Virtual Memory Access (DVMA) transactions between SBus masters and local resources. (referred to as Local DVMA)
- Direct Virtual Memory Access (DVMA) transactions between SBus masters and other SBus slave devices. (referred to as SBus DVMA)

The SBus interface works with the MMU to arbitrate the system and memory resources and for I/O address translations.

JTAG Test Bus Interface

The STP1012A has a five-wire Test Access Port (TAP) interface to support internal scan, boundary scan and clock control. This interface is compatible with IEEE 1149.1 specification, "IEEE Standard Test Access Port and Boundary Scan Architecture". This allows efficient access to any single chip in the daisy-chain without board-level multiplexing.

TAP Controller

The TAP controller is a synchronous Finite State Machine (FSM) which controls the sequence of operations of the JTAG test circuitry, in response to changes at the JTAG bus. The TAP controller is asynchronous with respect to the system clock(s), and can therefore be used to control the clock control logic.

The TAP FSM implements the state (16 states) diagram as detailed in the 1149.1 protocol.

PIN DESCRIPTIONS

Signal	Type	Description
MEM–DATA[63:0]	I/O	64-bit bidirectional memory data bus for accessing main memory.
MEMPAR[1:0]	I/O	Bidirectional memory data parity pins. Parity is provided on a word basis (for DRAM only).
MEMADDR[11:0]	Out	DRAM address output pins. These memory address pins require external buffering to provide the necessary drive for the DRAMs.
RAS_L[7:0]	Out	DRAM Row Address Strobe. Eight separate RAS signals, buffered externally to provide sufficient drive to connect directly to the DRAMs. 8 DRAM banks are supported.
CAS_L[3:0]	Out	DRAM Column Address Strobes. Four separate CAS signals are provided for word access. They should be buffered externally to provide sufficient drive to connect directly to the DRAMs. Two separate banks are supported by the 4 CAS lines.
MWE_L	Out	DRAM Write Enable output pin. MWE should be buffered externally to provide sufficient drive to connect directly to the DRAMs.
SBADDR[27:0]	Out	SBus Address output pins, to provide the Physical Address to SBus slave devices.
SBDATA[31:0]	I/O	Bidirectional SBus data pins. The 32-bit SBus data pins provide SBus support for the CPU, and support DBMA cycle access via the CPU SBus controller.
SLVSEL_L[4:0]	Out	Output Slave Select pins. A separate slave select is driven to each SBus slot and the I/O chip. This is used in conjunction with the physical address for accessing each slot/device.
SB_SIZE[2:0]	I/O	Bidirectional SBus transfer Size description pins. These three pins describe (encoded) the size of the data transfer of the current SBus operation (See SBus controller section).
SB_READ	I/O	Bidirectional SBus Read/Write pin. This pin indicates whether the current transfer is a read or a write operation.
SBCLK[2:0]	Out	SBus clock (16.6 MHz to 25 MHz depends on the input frequency and the DIV_CTL_setting) output pin.
SB_AS_L	Out	SBus Address Strobe Output pin.
SB_ACK_L[2:0]	I/O	Transfer Acknowledgment bidirectional pins. The ACK[2:0] pins return the status (encoded) of the current SBus transfer, from the slave.
SB_LERR_L	In	SBus Late data Error input pin. This pin is driven by the current SBUs slave, and aborts the current SBus transfer.
SB_BR_L[5:0]	In	Bus Request input pins (1/Bus Master).
SB_BG_L[5:0]	Out	Bus Grant output pins 1/Bus Master).
IRL[3:0]	In	Interrupt Request Lines Input pins. These 4 pins represent the encoded highest priority, pending interrupt. These pins are driven by the I/O chip, directly to the CPU.
CP_STAT_L[1:0]	Out	Active low CP Status output pins. Used to indicate CP interrupt/trap status as follows: 11 –Normal 10 –Level 15 interrupt 01 –Trap occurred, when trap disabled 00 –Reserved

PIN DESCRIPTIONS (CONTINUED)

Signal	Type	Description
JTAG_CK	In	Test (JTAG) input clock for boundary scan registers.
JTAG_MS	In	Test Mode Select input pin.
JTAG_TDI	In	Test Data Input pin (JTAG standard).
JTAG_TRST	In	JTAG Reset pin (JTAG standard).
JTAG_TDO	Out	Test Data Output pin (JTAG standard).
EXT_CLK1 EXT_CLK2	In	CPU input clock pins. EXT_CLK1 is used as the clock to sync up with the phase lock loop. EXT_CLK2 is used to *EXclusiveOr* with EXT_CLK1 to produce the clock in bypass PLL mode.
INPUT_RESET_L	In	Power-up reset input pin.
SP_SEL[1:0]	In	These two input pins set the memory controller to operate with various DRAM speeds at different processor clock frequencies. Typically, for 60ns DRAMs: 00 = 70 MHz 01 = 85 MHz. *(See Table 1 "Memory Interface Timing")*
DIV_CNTL[1:0]	In	These two input pins set the division ratio for the SBus clock from the internal system clock as follows: 00 = Illegal condition 01 = ÷ 3 10 = ÷ 4 11 = ÷ 5
Reserved 0	In	Pull to V_{DD2}.
Reserved 1	Out	Leave open.
STANDBY	In	Input pin to put the CPU in Standby mode. Apply a "0" logic level in normal operation.
REF_CLOCK	Out	Clock output at 2x frequency of EXT_CLK1.
PLL_BYP_L	In	Input pin to select output of the Phase Lock Loop (when 1) or the clock inputs directly (when 0).
SB_CR_L	Out	SBus CPU request output. For Debug only.
SB_CG_L	Out	SBus CPU grant output. For Debug only.
Reserved 2	In	Leave open.
Reserved 3	Out	Leave open.
GCLK	Out	Graphic clock output for the local bus. This is generated by dividing the SS_CLOCK by 3.
AEN	Out	Address enable output. (local bus)
S_REPLY	Out	Output pins defining the graphic operations.
P_REPLY[1:0]	In	Input pins defining when to take data from the data bus or when the buffer is emptied from the frame buffer.
AB[14:12]	Out	Address bits for local bus.
VDD1, VSS1	In	Core power/ground.

PIN DESCRIPTIONS (CONTINUED)

Signal	Type	Description
VDD2, VSS2	In	Power/ground for non-memory I/O.
VDD3, VSS3	In	Power/ground for memory interface I/O.
VDD4, VSS4	In	First power/ground for PLL.
VDD5, VSS5	In	Second power/ground for PLL.

TABLE 1: Memory Interface Timing

Description	Number of cycles			
	sp_sel = 00	sp_sel =01	sp_sel = 10	sp_sel = 11
$\overline{RAS}$ precharge	3.5	3.5	4.5	5.5
$\overline{CAS}$ precharge	1	1	2	2
$\overline{RAS}$ active (read)	6.5	7.5	8.5	10.5
$\overline{RAS}$ active (write)	5.5	5.5	6.5	8.5
$\overline{CAS}$ active (read)	3	4	4	5
$\overline{CAS}$ active (write)	2	2	2	3
Data, $\overline{WE}$, parity sent before $\overline{CAS}$	1	2	2	2
Data, $\overline{WE}$, parity hold after $\overline{CAS}$ active	2	2	2	3
Column address sent before $\overline{CAS}$	1	1	2	2
$\overline{CAS}$-before-$\overline{RAS}$ (refresh)	1.5	1.5	2.5	3.5
$\overline{RAS}$ active (refresh)	6.5	6.5	6.5	8.5

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings [1]

Parameter	Symbol	Min	Max	Units
Supply voltage	V_{DD1}, V_{DD4}	-0.5	4	V
	V_{DD2}, V_{DD3}, V_{DD5}	-0.5	7	V
Input voltage (any pin)	V_{IN}	-0.5	7	V
Input clamp current (any pin)	I_I	-20	20	mA
Operating junction temperature	T_J	0	125	°C
Storage temperature	T_S	-65	150	°C
Static discharge voltage		–	2000	V

1. Operation of the device at values in excess of those listed above may result in degradation or destruction of the device. All voltages are defined with respect to ground.

Recommended Operating Conditions: -70A, -85 [1]

Parameter		Symbol	-70A			-85			Units
			Min	Typ	Max	Min	Typ	Max	
Core supply voltage		V_{DD1}	3.15	3.3	3.6	3.4	3.5	3.6	V
Peripheral I/O supply voltage		V_{DD2}	4.75	5.0	5.25	4.75	5.0	5.25	V
Memory I/O supply voltage	5.0V System	V_{DD3}	4.75	5.0	5.25	4.75	5.0	5.25	V
	3.3V System	V_{DD3}	3.15	3.3	3.6	3.4	3.5	3.6	V
PLL supply voltage		V_{DD4}	3.15	3.3	3.6	3.4	3.5	3.6	V
		V_{DD5}	4.75	5.0	5.25	4.75	5.0	5.25	V
Ground		V_{SS}	-0.2	0	0.2	-0.2	0	0.2	V
DC I/O voltage	Peripheral I/O		0	–	V_{DD2}	0	–	V_{DD2}	V
	Memory I/O		0	–	V_{DD3}	0	–	V_{DD3}	V
Operating case temperature		T_C	0	–	80	0	–	80	°C

1. The STP1012A is designed with TTL compatible 5.0V I/O except for the memory interface pins. The memory interface operates with either a 3.3V or 5.0V supply.

DC Characteristics (V_{CC} = V_{DD2} or V_{DD3})

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input high voltage		2.0	–	V_{CC} + 0.2	V
V_{IL}	Input low voltage		–0.5	–	0.8	V
V_{OH}	Output high voltage	I_{OH} = 4.0 mA, V_{CC} = Min [1]	2.4	–	–	V
		I_{OH} = 5.0 mA, V_{CC} = Min [2]	2.4	–	–	V
		I_{OH} = 8.0 mA, V_{CC} = Min [3]	2.4	–	–	V
V_{OL}	Output low voltage	I_{OL} = 4.0 mA, V_{CC} = Min [1]	–	–	0.4	V
		I_{OL} = 5.0 mA, V_{CC} = Min [2]	–	–	0.4	V
		I_{OL} = 8.0 mA, V_{CC} = Min [3]	–	–	0.4	V
I_{IN}	Input current	V_{IN} = V_{CC} or GND, except [4]	–10	–	10	µA
		V_{IN} = V_{CC} or GND, [4]	–500	–	10	µA
I_{OZ}	Output leakage current	V_{OUT} = V_{CC} or GND, Outputs disabled	–10	–	10	µA
W_D	Power dissipation	V_{DD1}, V_{DD2}, V_{DD3} = max, f = 70 MHz	–	–	6	W
		V_{DD1}, V_{DD2}, V_{DD3} = max, f = 85 MHz	–	–	7	W

1. SB_CR, SB_CG, ISSURE_REQ, REF_CLOCK, JTAG_TDO, SLVSEL, SB_BG, CP_STAT, MEMADDR, RAS, CAS, MWE outputs only.
2. For each line of SBCLK output only.
3. MEMPAR, MEMDATA, SBDATA, SB_ACK, SB_SIZE, SB_READ, SBADDR and SB_AS outputs only.
4. JTAG_MS, JTAG_TRST, JTAG_TDI, JTAG_CK, INPUT_RESET_L, PLL_BYP_L (Internal Pull-up).

Capacitance

Symbol	Parameter	Max	Units
C_{IN}	Input capacitance	15	pF
C_{OUT}	Output capacitance	10	pF
C_{BI}	Bidirectional capacitance	15	pF

AC Characteristics (Input Pins)

Pin Name	Symbol	Conditions	Reference Edge	-70A		-85		Unit
				Min	Max	Min	Max	
SB_LERR_L	t_{SI}		sbclk+	15	–	15	–	ns
	t_{HI}		sbclk+	0	–	0	–	ns
SB_BR_L[4:0]	t_{SI}		sbclk+	15	–	15	–	ns
	t_{HI}		sbclk+	0	–	0	–	ns
IRL[3:0]	t_{SI}	2 cycles	ref_clk+	10	–	7	–	ns
	t_{HI}		ref_clk+	1	–	1	–	ns
JTAG_CK	t_{HC}	1 MHz –10 MHz	asynch	25	–	25	–	ns
	t_{LC}		asynch	25	–	25	–	ns
	t_{RC}		asynch	–	10	–	10	
	t_{FC}		asynch	–	10	–	10	
JTAG_MS	t_{SI}		jtag_ck+	10	–	10	–	ns
	t_{HI}		jtag_ck+	0	–	0	–	ns
JTAG_TDI	t_{SI}		jtag_ck+	10	–	10	–	ns
	t_{HI}		jtag_ck+	0	–	0	–	ns
JTAG_TRST_L	t_{SI}	2 cycles	jtag_ck+	10	–	10	–	ns
	t_{HI}		jtag_ck+	0	–	0	–	ns
EXT_CLK1	t_{P}			28.5	–	23.5	–	ns
	t_{HC}			4	–	4	–	ns
	t_{LC}			4	–	4	–	ns
	t_{RC}			–	5	–	5	ns
	t_{FC}			–	5	–	5	ns
P_REPLY[1:0]	t_{SI}		gclk+	REF_CLK + 9	–	REF_CLK + 9	–	ns
	t_{HI}		gclk+	REF_CLK + 0	–	REF_CLK + 0	–	ns
INPUT_RESET_L	t_{SI}	32 cycles	ref_clk+	10	–	7	–	ns
	t_{HI}		ref_clk+	1	–	1	–	ns

AC Characteristics (Bidirectional Pins)

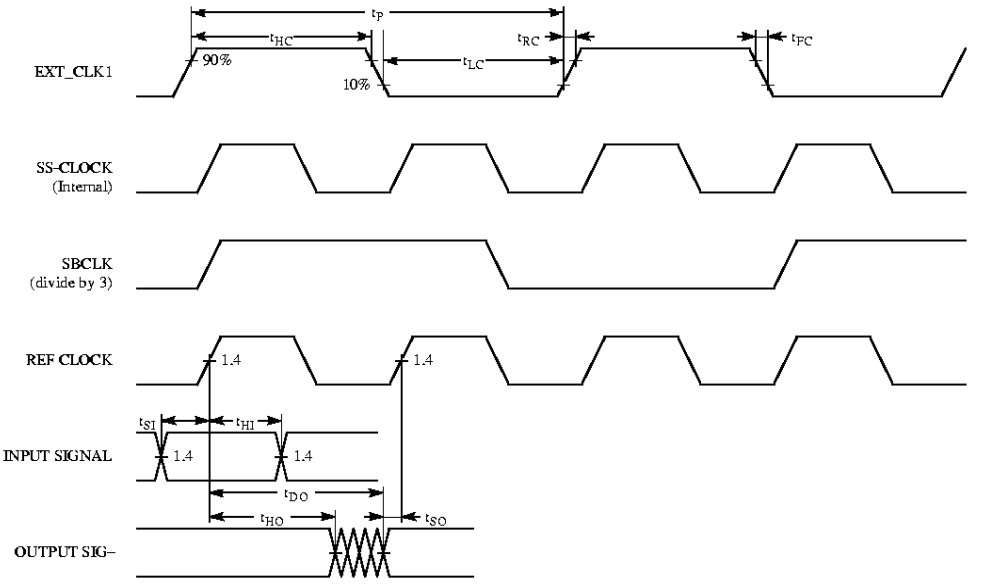
Pin Name	Symbol	Conditions	Reference Edge	-70A		-85		Unit
				Min	Max	Min	Max	
MEM-DATA[63:0][1]	t_{DO}	100 pF	ref_clk+	–	15	–	13	ns
	t_{HO}	100 pF	ref_clk+	0	–	0	–	ns
	t_{SI}		ref_clk+	7	–	7	–	ns
	t_{HI}		ref_clk+	0	–	0	–	ns
MEMPAR[1:0][1]	t_{DO}	85 pF	ref_clk+	–	15	–	13	ns
	t_{HO}	85 pF	ref_clk+	0	–	0	–	ns
	t_{SI}		ref_clk+	7	–	7	–	ns
	t_{HI}		ref_clk+	0	–	0	–	ns
SBDATA[31:0]	t_{SO}	100 pF, 10K¾ pull-up	sbclk+	15	–	15	–	ns
	t_{HO}		sbclk+	2.5	–	2.5	–	ns
	t_{SI}	100 pF, 10K¾ pull-up	sbclk+	15	–	15	–	ns
	t_{HI}		sbclk+	0	–	0	–	ns
SB_SIZE[2:0]	t_{SO}	100 pF, 10K¾ pull-up	sbclk+	15	–	15	–	ns
	t_{HO}		sbclk+	2.5	–	2.5	–	ns
	t_{SI}	100 pF, 10K¾ pull-up	sbclk+	15	–	15	–	ns
	t_{HI}		sbclk+	0	–	0	–	ns
SB_READ	t_{SO}	100 pF, 10K¾ pull-up	sbclk+	15	–	15	–	ns
	t_{HO}		sbclk+	2.5	–	2.5	–	ns
	t_{SI}	100 pF, 10K¾ pull-up	sbclk+	15	–	15	–	ns
	t_{HI}		sbclk+	0	–	0	–	ns
SB_ACK_L[2:0]	t_{SO}	100 pF, 10K¾ pull-up	sbclk+	15	–	15	–	ns
	t_{HO}		sbclk+	2.5	–	2.5	–	ns
	t_{SI}	100 pF, 10K¾ pull-up	sbclk+	16	–	16	–	ns
	t_{HI}		sbclk+	0	–	0	–	ns

1. DRAM interface pins tested with V_{DD3} 5.0V ±5%.

AC Characteristics (Output Pins)

Pin Name	Symbol	Conditions	Reference Edge	-70A		-85		Unit
				Min	Max	Min	Max	
MEMADDR[11:0][1]	t_{DO}	28 pF	ref_clk+	–	15	–	14	ns
	t_{HO}	28 pF	ref_clk+	0	–	0	–	ns
RAS_L[7:0]+ [1]	t_{DO}	35 pF	ref_clk+	–	10	–	10	ns
	t_{HO}	35 pF	ref_clk+	0	–	0	–	ns
RAS_L[7:0]–[1]	t_{DO}	35 pF	ref_clk–	–	10	–	10	ns
	t_{HO}	35 pF	ref_clk–	0	–	0	–	ns
CAS_L[3:0] [1]	t_{DO}	55 pF	ref_clk+	–	10	–	10	ns
	t_{HO}	55 pF	ref_clk+	2	–	2	–	ns
MWE_L [1]	t_{DO}	28 pF	ref_clk+	–	12	–	12	ns
	t_{HO}	28 pF	ref_clk+	0	–	0	–	ns
SLVSEL_L[4:0]	t_{SO}	20 pF	sbclk+	15	–	15	–	ns
	t_{HO}	20 pF	sbclk+	2.5	–	2.5	–	ns
SBADDR[27:0]	t_{SO}	100 pF	sbclk+	15	–	15	–	ns
	t_{HO}	100 pF	sbclk+	2.5	–	2.5	–	ns
SB_AS_L	t_{SO}	100 pF	sbclk+	15	–	15	–	ns
	t_{HO}	100 pF	sbclk+	2.5	–	2.5	–	ns
SB_BG_L[4:0]	t_{SO}	20 pF	sbclk+	15	–	15	–	ns
	t_{HO}	20 pF	sbclk+	2.5	–	2.5	–	ns
CP_STAT[1:0]	t_{DO}	10 pF	ref_clk+	–	15	–	15	ns
	t_{HO}	10 pF	5 cycles	0	–	0	–	ns
JTAG_TDO	t_{DO}	80 pF	jtag_ck+	–	30	–	30	ns
	t_{HO}	80 pF	jtag_ck+	0	–	0	–	ns
SBCLK+	t_{DO}	44 pF	ref_clk+	–1	1	–1	1	ns
AB[14:12]	t_{DO}	35 pF	ref_clk+	–	12	–	12	ns
	t_{HO}	35 pF	ref_clk+	0	–	0	–	ns
S_REPLY	t_{DO}	35 pF	ref_clk+	–	12	–	12	ns
	t_{HO}	35 pF	ref_clk+	0	–	0	–	ns
AEN	t_{DO}	35 pF	ref_clk+	–	12	–	12	ns
	t_{HO}	35 pF	ref_clk+	0	–	0	–	ns
GCLK+	t_{DO}	35 pF	ref_clk+	–1	1	–1	1	ns

1. DRAM interface pins tested with V_{DD3} 5.0V ±5%.



Parameter Definitions

t_{SI} : Required setup time of a chip input referenced to a given (clock) edge.
t_{HI} : Required hold time of a chip input referenced to a given (clock) edge.
t_{DO}: Guaranteed propagation time of an output referenced to a given (clock) edge.
t_{HO}: Guaranteed hold time of an output referenced to a given (clock) edge.
t_{SO} : Guaranteed setup time of an output referenced to a next given (clock) edge.
t_{HC}: Required clock high time.
t_{LC}: Required clock low time.
t_{rC} : Required clock rise time.
t_{fC} : Required clock fall time.

Figure 3. Timing Waveforms

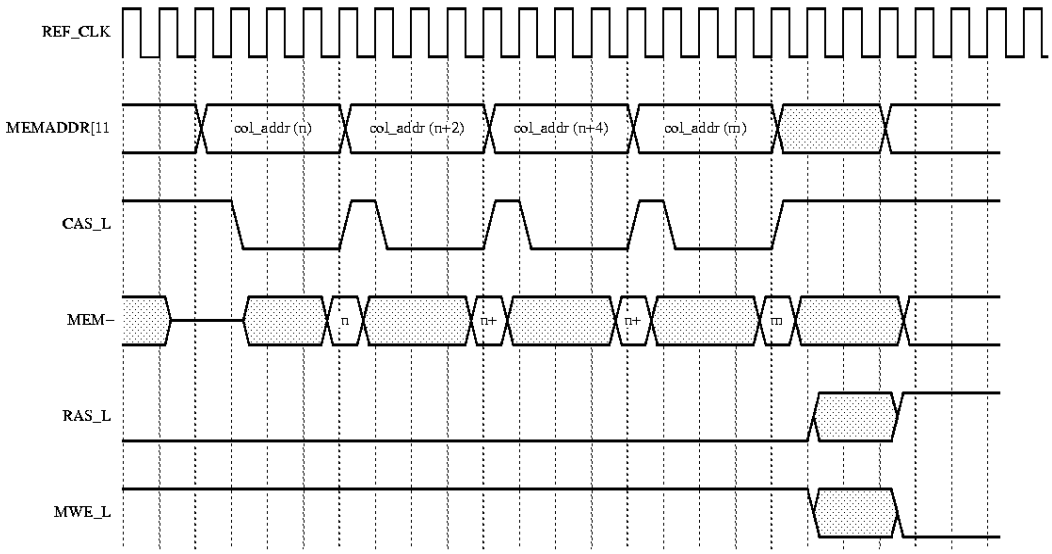


Figure 4. Page Mode Read Following a Read

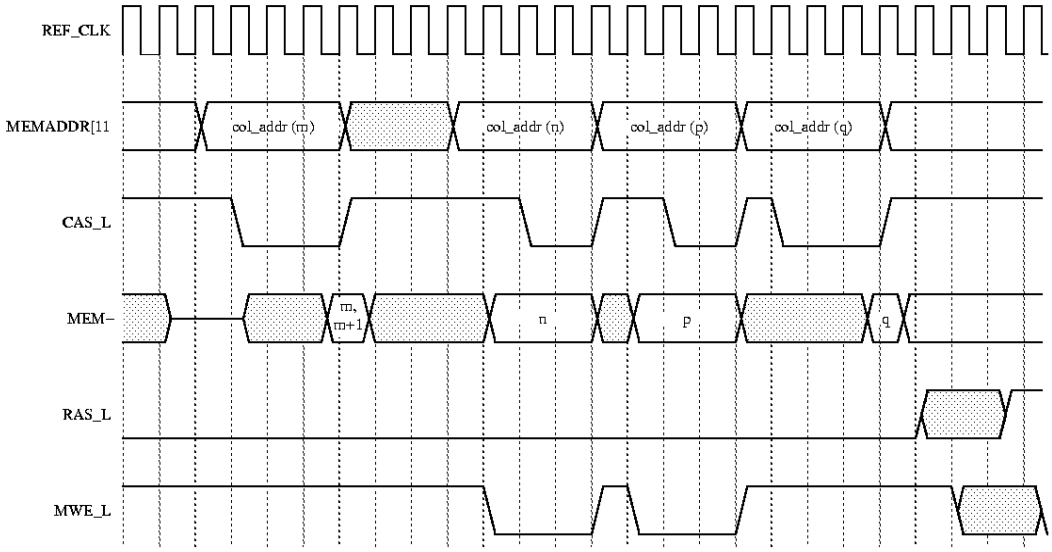


Figure 5. Page Mode Write Following a Read

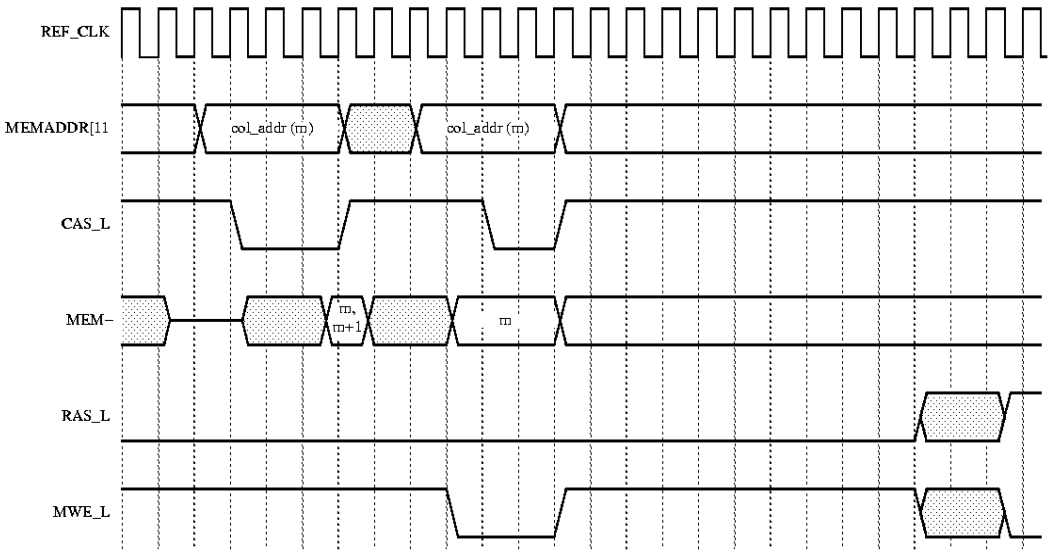


Figure 6. Page Mode Read–Modify–Write Sequence

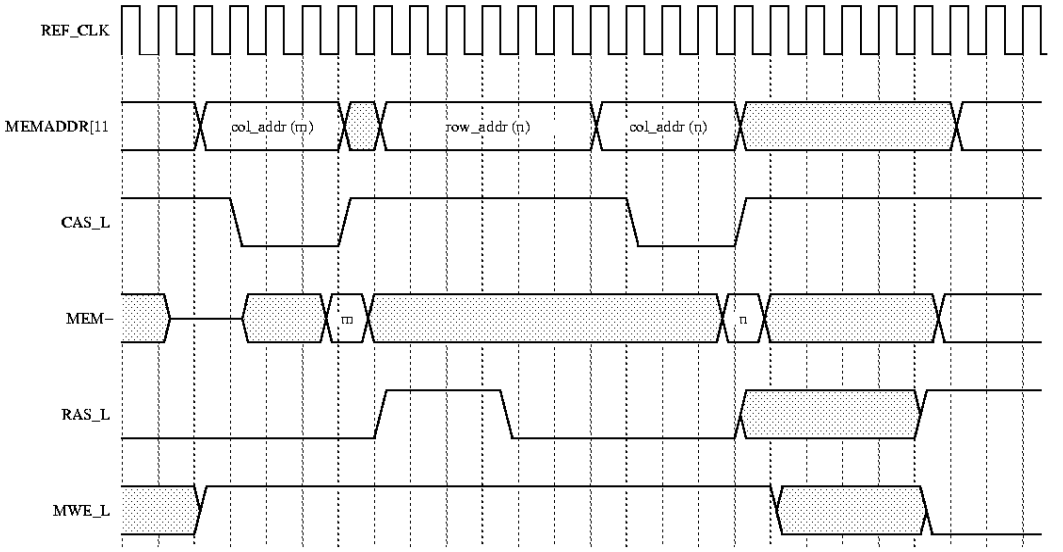


Figure 7. Non Page Read Following a Read

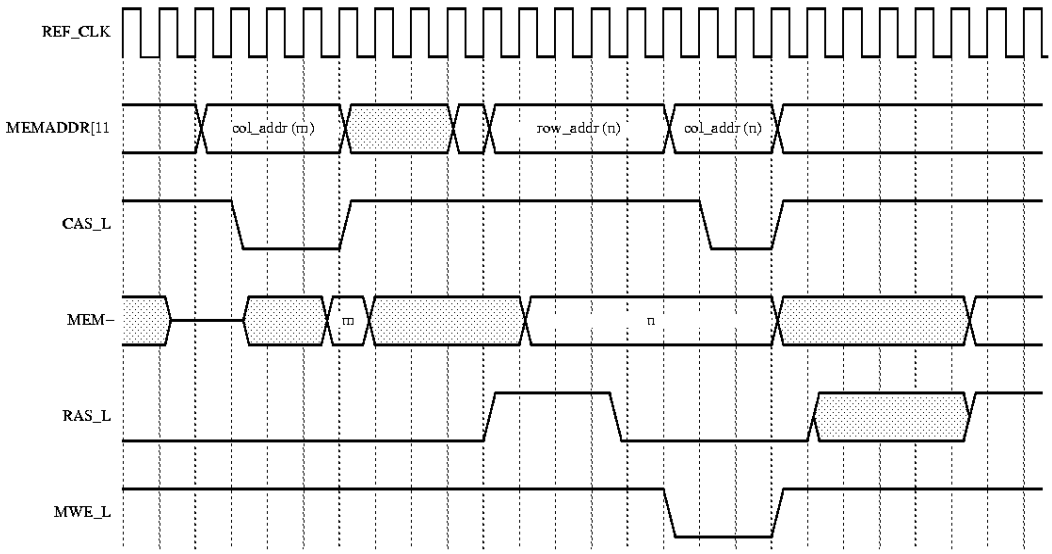


Figure 8. Non Page Write Following a Read

CPGA 321 PACKAGE PIN ASSIGNMENT

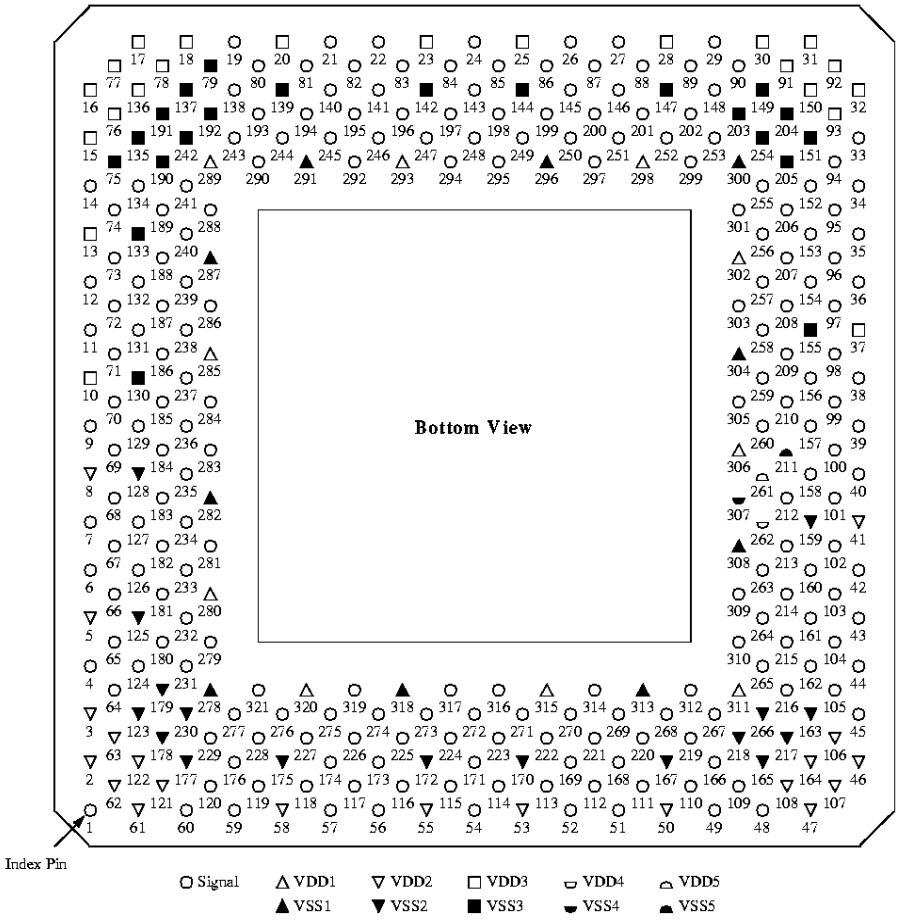
Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	N.C.	55	VDD2 (5V)	109	SBADDR [11]	163	VSS2	217	VSS2	271	SB_SIZE [2]
2	VDD2 (5V)	56	SB_BG_L [4]	110	SBADDR [6]	164	VDD2 (5V)	218	VSS2	272	SB_BR_L [5]
3	VDD2 (5V)	57	SB_BG_L [2]	111	SBADDR [2]	165	VSS2	219	SBADDR [8]	273	SB_BR_L [0]
4	SBDATA [10]	58	VDD2 (5V)	112	SB_ACK_L [2]	166	SBADDR [10]	220	SBADDR [5]	274	SLVSEL_L [4]
5	VDD2 (5V)	59	SLVSEL_L [0]	113	SB_SIZE [0]	167	VSS2	221	SBADDR [0]	275	SBDATA [29]
6	SBDATA [5]	60	SBDATA [27]	114	SBCLK [0]	168	SBADDR [1]	222	SB_ACK_L [0]	276	SBDATA [24]
7	SBDATA [0]	61	VDD2 (5V)	115	SB_BR_L [3]	169	SB_ACK_L [1]	223	SBCLK [2]	277	SBDATA [21]
8	VDD2 (5V)	62	VDD2 (5V)	116	SB_BG_L [5]	170	VSS2	224	SB_BR_L [1]	278	VSS1
9	SP_SEL [1]	63	VDD2 (5V)	117	SB_BG_L [0]	171	SB_LERR_L	225	SB_BG_L [3]	279	SBDATA [19]
10	VDD3 (3/5V)	64	SBDATA [17]	118	SLVSEL_L [1]	172	VSS2	226	SLVSEL_L [3]	280	VDD1
11	MEMDATA [58]	65	SBDATA [11]	119	SBDATA [31]	173	SB_BG_L [1]	227	SBDATA [28]	281	SBDATA [9]
12	MEMDATA [53]	66	SBDATA [8]	120	SBDATA [26]	174	SLVSEL_L [2]	228	SBDATA [23]	282	VSS1
13	VDD3 (3/5V)	67	SBDATA [3]	121	VDD2 (5V)	175	VSS2	229	SBDATA [22]	283	JTAG_TDO
14	MEMDATA [47]	68	SB_CG_L	122	VDD2 (5V)	176	SBDATA [25]	230	VSS2	284	MEMDATA [62]
15	VDD3 (3/5V)	69	JTAG_TDI	123	VSS2	177	VSS2	231	SBDATA [18]	285	VDD1
16	VDD3 (3/5V)	70	SP_SEL [0]	124	SBDATA [16]	178	VSS2	232	SBDATA [15]	286	MEMDATA [50]
17	VDD3 (3/5V)	71	MEMDATA [60]	125	VSS2	179	VSS2	233	SBDATA [12]	287	VSS1
18	VDD3 (3/5V)	72	MEMDATA [55]	126	SBDATA [6]	180	SBDATA [14]	234	SBDATA [4]	288	MEMDATA [41]
19	MEMDATA [35]	73	MEMDATA [49]	127	SBDATA [2]	181	SBDATA [13]	235	SB_CR_L	289	VDD1
20	VDD3 (3/5V)	74	MEMDATA [46]	128	VSS2	182	SBDATA [7]	236	JTAG_CK	290	MEMDATA [40]
21	RAS_L [3]	75	VSS3	129	JTAG_MS	183	SBDATA [1]	237	MEMDATA [61]	291	VSS1
22	CAS_L [2]	76	VDD3 (3/5V)	130	VSS3	184	JTAG_TRST_L	238	MEMDATA [56]	292	RAS_L [6]
23	VDD3 (3/5V)	77	VDD3 (3/5V)	131	MEMDATA [57]	185	MEMDATA [63]	239	MEMDATA [51]	293	VDD1
24	MEMADDR [9]	78	VDD3 (3/5V)	132	MEMDATA [52]	186	MEMDATA [59]	240	MEMDATA [44]	294	MEMPAR [1]
25	VDD3 (3/5V)	79	VSS3	133	VSS3	187	MEMDATA [54]	241	MEMDATA [42]	295	MEMADDR [7]
26	MEMADDR [2]	80	MEMDATA [34]	134	MEMDATA [45]	188	MEMDATA [48]	242	VSS3	296	VSS1
27	AB[12]	81	RAS_L [7]	135	VSS3	189	MEMDATA [43]	243	MEMDATA [39]	297	P_REPLY [0]
28	VDD3 (3/5V)	82	RAS_L [0]	136	VDD3 (3/5V)	190	VSS3	244	MEMDATA [37]	298	VDD1
29	MEMDATA [28]	83	CAS_L [1]	137	VSS3	191	VSS3	245	MEMDATA [32]	299	MEMDATA [22]
30	VDD3 (3/5V)	84	MWE_L	138	MEMDATA [36]	192	VSS3	246	RAS_L [2]	300	VSS1
31	VDD3 (3/5V)	85	MEMADDR [6]	139	VSS3	193	MEMDATA [38]	247	CAS_L [0]	301	MEMDATA [21]
32	VDD3 (3/5V)	86	MMEMADDR [4]	140	RAS_L [5]	194	MEMDATA [33]	248	MEMADDR [11]	302	VDD1
33	MEMDATA [19]	87	MEMADDR [0]	141	RAS_L [1]	195	RAS_L [4]	249	MEMADDR [5]	303	MEMDATA [12]
34	MEMDATA [13]	88	P_REPLY [1]	142	VSS3	196	CAS_L [3]	250	GCLK	304	VSS1
35	MEMDATA [8]	89	MEMDATA [29]	143	MEMADDR [10]	197	MEMPAR [0]	251	MEMDATA [30]	305	Reserved 2
36	MEMDATA [2]	90	MEMDATA 23]	144	VSS3	198	MEMADDR [8]	252	MEMDATA [25]	306	VDD1
37	VDD3 (3/5V)	91	VDD3 (3/5V)	145	MEMADDR [1]	199	MEMADDR [3]	253	MEMDATA [24]	307	VSS4 (PLL 3.3V)
38	AB [14]	92	VDD3 (3/5V)	146	S_REPLY	200	AEN	254	VSS3	308	VSS1
39	IRL [0]	93	VDD3 (3/5V)	147	VSS3	201	MEMDATA [31]	255	MEMDATA [20]	309	SBADDR [19]
40	Reserved 0	94	MEMDATA [17]	148	MEMDATA [27]	202	MEMDATA [26]	256	MEMDATA [15]	310	SBADDR [15]
41	VDD2 (5V)	95	MEMDATA [11]	149	VSS3	203	VSS3	257	MEMDATA [14]	311	VDD1
42	PLL_BYP_L	96	MEMDATA [7]	150	VDD3 (3/5V)	204	VSS3	258	MEMDATA [6]	312	SBADDR [13]
43	DIV_CNTL [0]	97	MEMDATA [3]	151	VSS3 (3/5V)	205	VSS3	259	MEMDATA [0]	313	VSS1
44	SBADDR [27]	98	AB [13]	152	MEMDATA [16]	206	MEMDATA [18]	260	IRL [2]	314	SBADDR [3]
45	SBADDR [24]	99	IRL [3]	153	MEMDATA [10]	207	MEMDATA [9]	261	VDD5 (PLL 5V)	315	VDD1
46	VDD2 (5V)	100	INPUT_RESET_L	154	MEMDATA [4]	208	MEMDATA [5]	262	VDD4 (PLL 3.3V)	316	SBCLK [1]
47	VDD2 (5V)	101	EXT_CLK2	155	VSS3	209	MEMDATA [1]	263	SBADDR [26]	317	SB_BR_L [2]
48	SBADDR [12]	102	DIV_CNTL [1]	156	Reserved 3	210	N.C. (Reserved)	264	SBADDR [20]	318	VSS1
49	SBADDR [7]	103	CP_STAT_L [1]	157	IRL[1]	211	VSS5 (PLL 5V)	265	SBADDR [16]	319	SBDATA [30]
50	VDD2 (5V)	104	Reserved 1	158	STANDBY	212	EXT_CLK1	266	VSS2	320	VDD1
51	SB_AS_L	105	SBADDR [21]	159	VSS2	213	REF_CLK	267	SBADDR [14]	321	SBDATA [20]
52	SB_SIZE [1]	106	VDD2 (5V)	160	CP_STAT_L [0]	214	SBADDR [23]	268	SBADDR [9]		
53	VDD2 (5V)	107	VDD2 (5V)	161	SBADDR [25]	215	SBADDR [18]	269	SBADDR [4]		
54	SB_BR_L [4]	108	VDD2 (5V)	162	SBADDR [22]	216	SBADDR [17]	270	SB_READ		

STP1012A CPGA321 THERMAL CHARACTERISTICS (TYPICAL)

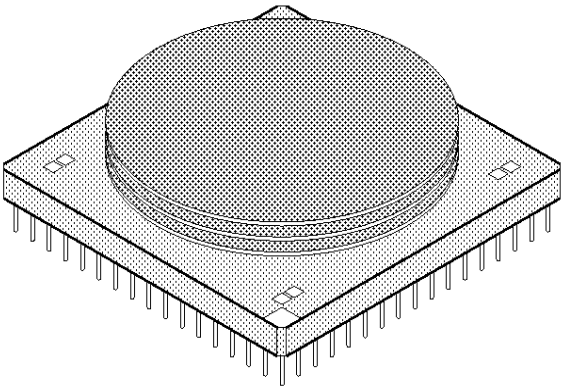
Package	Heat Sink	Theta j-a Airflow (LF/m)				Theta j-c	
		0	200	600	1000	1 [1]	2 [2]
CPGA-321	3-Fin Heatsink	13.5	8.5	4.5	3.5	0.8	1.6

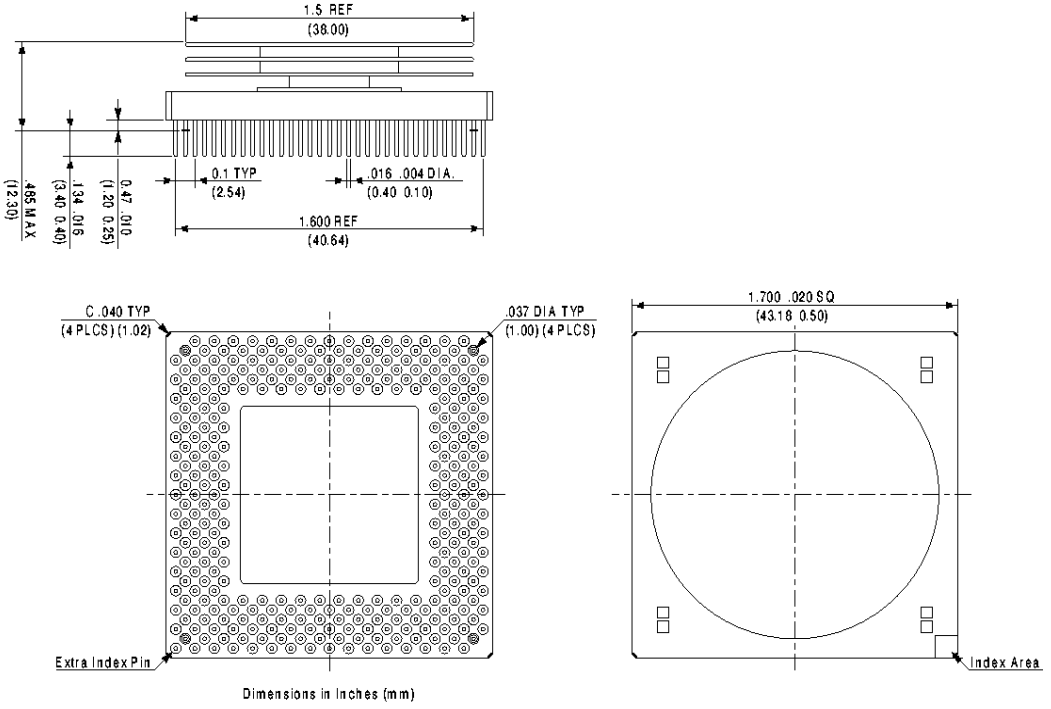
1. Measured at the package (Base of heatsink)
2. Measured at the top of the heat sink.

STP1012A CPGA321 PIN LAYOUT



CPGA321 PACKAGE DIMENSIONS





STP1012A ERRATA

This errata applies to the following products:

- STP1012APGA–70A microSPARC CPU
- STP1012APGA–85 microSPARC CPU

Errata Categories:

System Design

These errata are deviations from the product specification that a system design engineer needs to be aware of. These would include bus protocol, mechanical and thermal errata.

Performance

These errata result only in a loss in performance. These errata do not cause functional errors.

Operating System

These errata only occur with privileged–mode or supervisor–mode instructions. Workarounds should be implemented in the operating system or boot PROM. The target audience is the operating system or system firmware engineer.

Application Software

These errata can occur with nonprivileged–mode or user–mode instructions. The target audience is anyone writing software for a platform using this part, including the end–user, independent software vendors, and operating system engineers.

Each erratum will have the following rating scale at the top of each description:

System Design	Performance	Operating System	Application

Erratum: DRAM T_{PC} Timing Fix:

System Design	Performance	Operating System	Application

Description: (Ref. #319850)

The time between the falling edge of CAS in page mode operation, specified as T_{PC} in DRAM specifications, may not be met by some DRAM vendors. The change extends the duration of CAS active on writes by one cycle for 85 and 100 MHz case; i.e. speed_select of 1 and 2, respectively.

Workaround:

In practice, DRAMs that do not meet the Tpc requirement have proven to function normally, since the DRAMs run faster than specification.

This problem is fixed in STP1012B.

ORDERING INFORMATION

Part Number	Speed	Description
STP1012APGA-70A	70 MHz	Standard Supply Voltages
STP1012APGA-85	85 MHz	Special Supply Voltages

Notes:

Notes:

Preliminary
STP1012A

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