V320USC

HIGH INTEGRATION, LOW COST PCI SYSTEM CONTROLLER
For 32 Bit MIPS™ and SuperH™ Processors

- Glueless interface between the popular MIPS™ and SuperH™ processors and the industry standard PCI Bus
- Fully compliant with PCI 2.2 specification
- Configurable for primary master, bus master, and target PCI operation
- SDRAM Controller with support for Enhanced SDRAM
- Up to 1Kbyte burst access to (E)SDRAM from PCI, 32byte from the local processor
- 640 bytes of on chip FIFO storage with DYNAMIC BANDWIDTH ALLOCATION™
- On-the-fly byte order (endian) conversion
- I_2O-Ready™ ATU and messaging unit
- Programmable chip select/peripheral device strobe generation
- PICMG Hot Swap Ready including on-chip bias voltage
- 3.3v operation with 5v tolerant I/O
- 208-pin PQFP package
- Up to 75MHz local bus clock with separate asynchronous PCI clock up to 33MHz
- 2-32 bit timers, watchdog, heartbeat and bus watch timers
- Initialization through local processor, PCI, or serial EEPROM

The V320USC is a 3rd generation PCI product that also integrates many of the functions that are needed in typical embedded systems. Its high level of integration results in a very high performance, low cost system solution for some of the most popular 32/64 bit processors available.

3 WAY ARCHITECTURE

A 3-bus architecture is employed by the V320USC so that the processor, PCI bus and memory system can all operate independently when a MIPS processor is used. As a result, the USC is really 3 bridges in one package. With 3 concurrent buses, system performance is increased and deadlock conditions eliminated.

PCI CONTROLLER AND MORE

The PCI bus is an important standard used in today's embedded systems. While the V320USC addresses this important requirement, it is also far more than a PCI interface. It also controls the most essential components of an embedded system such as SDRAM memory, FLASH memory and peripherals using a very flexible Memory Controller and Peripheral Control Unit.

DIRECT PROCESSOR INTERFACE

Some of the most popular and cost effective processors in the industry, such as MIPS and SuperH, will connect directly to the V320USC. The interfaces are designed to provide low latency of access by employing large on-chip buffers that utilize the Dynamic Bandwidth Allocation™ feature. This feature allows the on-chip buffers to be more fully utilized.

INDUSTRIAL STRENGTH PCI

CompactPCI applications will benefit from the Hot Swap features implemented by the V320USC according to the PICMG™ specification. The V320USC is a "Hot Swap Ready" silicon device as defined by the specification. For this, the V320USC employs custom designed PCI buffers that provide the necessary bias voltage. This eliminates the need for more than 40 external components that would be required by other solutions. When the bias voltage is enabled, the input buffers are automatically disabled to prevent excessive current flow through the P and N devices of the input buffers.

Other PICMG requirements for Hot Swap such as the ejector input, extended Configuration Registers (HS_CSR, and ECP), blue LED and ENUM# output are provided. V3 has long established itself as a leader in industrial applications with all components in the product line, including the V320USC, available as industrial temperature devices.

V3 SEMICONDUCTOR
THE EMBEDDED INTELLIGENCE COMPANY

COST EFFECTIVE SOLUTIONS THAT SIMPLIFY EMBEDDED SYSTEM DESIGN!

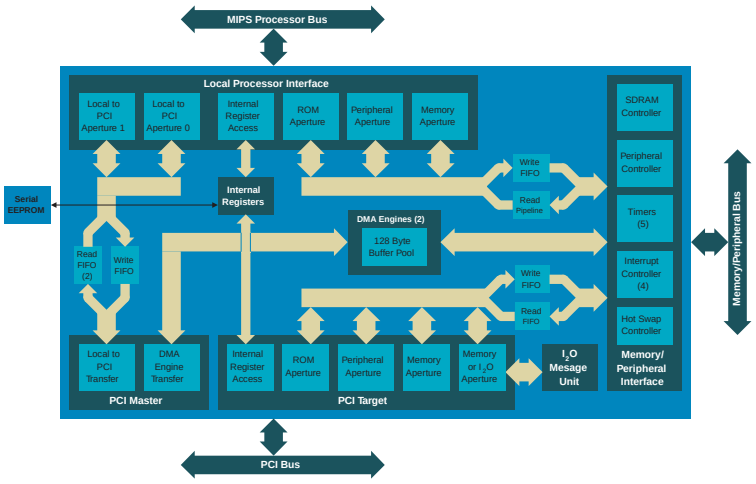


Figure 1.
V320USC Block Diagram (MIPS mode)

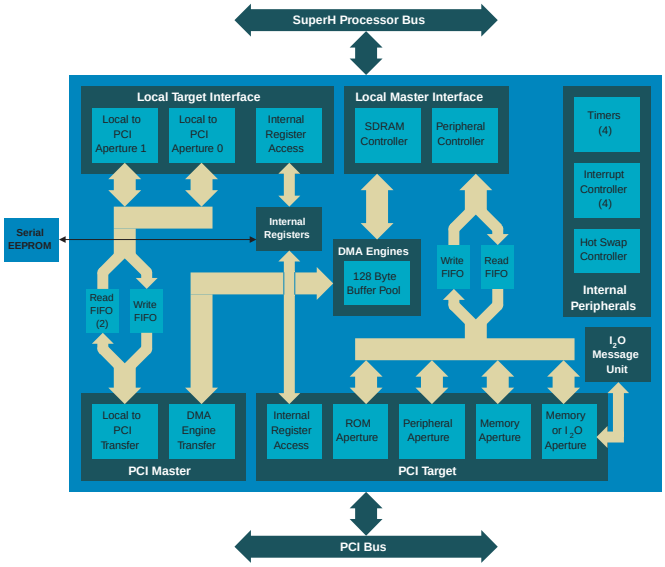


Figure 2.
V320USC Block Diagram (SuperH mode)

MASTERING THE PCI BUS

It would be pointless to emphasize the 132MB/s peak PCI transfer rate of the V320USC (which is at the theoretical maximum). Throughput in real world applications is what counts and that is exactly what the V320USC was designed to do. To achieve this, long sustained bursting is the key. The PCI bus master interface on the V320USC guarantees the highest possible overall bus utilization by employing large on chip buffers and never inserting wait states. The large on chip memory (640 bytes total) ensures long bursts so that the overhead of starting a cycle are amortized over more data. When the USC can no longer handle more data then it will end the transfer, rather than insert IRDY wait states, so that other masters can utilize the bus.

PCI TARGET APPLICATIONS

The V320USC provides 5 independent slave interfaces: 1-internal register access, 2-SDRAM memory apertures (one of which also acts as an I_2O ATU), a Peripheral aperture and a ROM aperture. Except for the internal register aperture, all other slave apertures are directed through FIFO buffers that are designed to maximize bus utilization. When the V320USC, as a target, is accessed by a PCI master, it will either return a target ready one cycle after FRAME or it will issue a retry. A retry will be issued if the write FIFO is full (writes) or there is no prefetched read data (reads). This allows other PCI transactions to proceed and keep the bus occupied. When the V320USC is ready to deliver data then it will assert TRDY and keep it asserted as long as data can move. When data cannot move, the USC will terminate the transfer with the last data rather than insert target wait states.

DUAL DMA ENGINE WITH DESCRIPTOR PROCESSING

Two fully independent DMA engines provide one of the fastest methods of moving data in the system. Each engine is capable of processing descriptors in either PCI space or local memory. The unique Pooled Buffer™ architecture of the V320USC guarantees high bus utilization and long sustained bursts. Two FIFO buffers (128 bytes total) are dedicated to the DMA engines. The buffers can be dynamically allocated to the DMA engines on a priority basis. When a single or high priority DMA engine is activated, then both buffers can be allocated to it to allow longer bursts. Burst length, however, is not limited to total buffer size since simultaneous fill and drain can easily be achieved. When both DMA engines are activated together, then they can be prioritized to allow fair and equal access to the buffers, first-come first-serve or fixed priority.

Other DMA features

- Anywhere-to-anywhere DMA: PCI, SDRAM or peripheral to PCI, SDRAM or peripheral
- Descriptor based scatter/gather capability
- Descriptor write-back to indicate completion of an individual descriptor link and to allow looped descriptors
- Block Fill
- Interrupt on End of Transfer (EOT) or End of Link (EOL)
- Programmable byte lane swapping
- Burst loading of descriptors

TUNING FOR PERFORMANCE

The Dynamic Bandwidth Allocation architecture allows the application developer to fine tune the 640 bytes of on-chip buffers to achieve the best overall system performance for a specific application. It also allows data to be packed into the on-chip buffers so that higher utilization is achieved. For example, when the local processor writes data to the PCI, multiple sequential or non-sequential bursts or single cycles can be queued into the posting FIFO. Furthermore, sequential bursts or single cycles from the processor can be automatically combined into larger bursts on the PCI bus. These are some of the examples of tunable features within the V320USC:

- The write posting drain strategy can be programmed to determine how aggressively the Local Processor to PCI writes will be drained. Simultaneous filling and draining allows long bursts to be sustained - even longer than the write-posting buffer size.
- Prefetched read data can be stored in either a single buffer or two buffers (64 bytes total) managed as a least recently used cache. With dual buffers, two sequential streams of data can be prefetched continuously without scrapping data.
- Thresholds for the prefetch buffers are programmable to determine how aggressively they will be filled.

MESSAGING UNIT

- 32 Byte bi-directional mailbox with interrupts
- Queue based I_2O messaging unit (can also be used as a general purpose messaging unit)

DUAL PORTED SDRAM INTERFACE

Memory is at the heart of most embedded systems and is a key factor in determining overall system performance. V3 Semiconductor was the first company to provide single chip DRAM control solutions fine-tuned to the appetites of embedded RISC processors. The V320USC builds on that experience by tightly integrating SDRAM control functions into the PCI and processor interfaces. The result is a very low latency memory system that actually behaves like two memory controllers: one optimized for PCI access and another optimized for the local processor.

When a MIPS processor is used, the SDRAM controller uses a toggle burst order the same as the processor. However, for PCI access, linear bursts are used to provide the greatest PCI compatibility. When a SuperH processor is used, it can access SDRAM directly and bypass the V320USC.

Other SDRAM features:

- Up to 1GB of SDRAM in 4 blocks
- Very flexible address multiplexing modes (more than 100 modes)
- Fine grained control over SDRAM timing parameters
- I^2C interface for reading configuration data from DIMMs
- Supports Enhanced SDRAM for higher performance
- SDRAM can be accessed by an alternate bus master

PERIPHERAL CONTROL UNIT

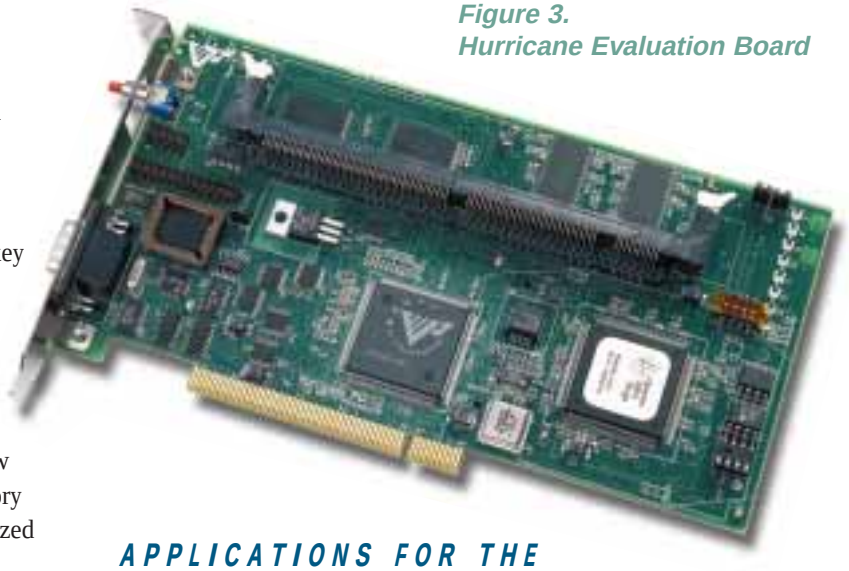
A Peripheral Control Unit (PCU) provides a simple way to interface 8/16 or 32 bit peripherals to either PCI bus or the local processor. A total of 5 chip select strobes can be generated, each with separately controlled read/write timing characteristics and data width.

INTEGRATED PERIPHERALS

As a system controller, the V320USC provides additional peripheral functions that are required in a typical embedded system.

- 2 - 32 bit general purpose timers can be individually configured as a pulse width modulator, rate generator, pulse counter or hardware/software triggered pulse generator.
- Watchdog timer for graceful recovery from catastrophic program failures
- Heartbeat interrupt timer for RTOS interrupt generation
- Bus watch timer to prevent system hangs during accesses to un-decoded regions
- 4 channel interrupt controller to generate either PCI or local CPU interrupts and interrupt cross-routing

Figure 3.
Hurricane Evaluation Board



APPLICATIONS FOR THE V320USC

The V320USC is well suited to the most demanding embedded applications in networking, telecom, servers, digital video and industrial control. Windows CE developers will benefit from the rich feature set of the V320USC for use in CompactPCI or set-top box applications.

ADD-IN CARD APPLICATIONS

Either CompactPCI, PMC or standard PCI plug-in adapters are easily and quickly designed using the V320USC. Typical applications include xDSL/ISDN modems, RAID controllers and ATM adapters. The USC employs the latest standards in power management and intelligent I/O so that the need for proprietary solutions is avoided. The Hurricane evaluation board (Figure 3) and accompanying software provides an ideal starting point to launch your design.

COST EFFECTIVE SOLUTIONS THAT SIMPLIFY EMBEDDED SYSTEM DESIGN!

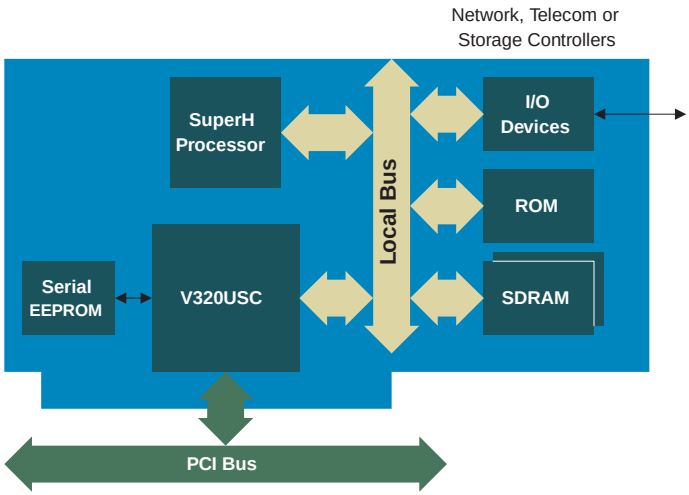


Figure 4.
Plug-in Card Application

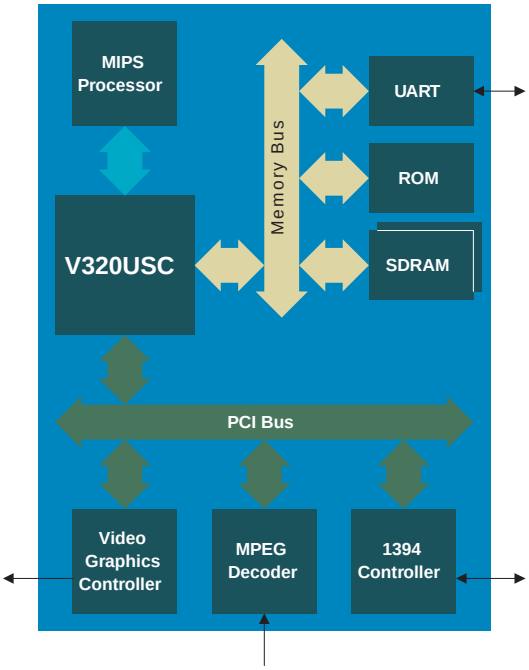


Figure 5.
Embedded Host Application

HOST CONTROLLER APPLICATION

In embedded applications the V320USC makes an ideal host bridge. In this type of application, the USC performs as the main system master. In this capacity, the local processor is responsible for enumerating devices on the PCI bus via the USC using either type 0 or type 1 configuration cycles. An example of this application is a set-top box (Figure 5). In this application, the operating system and user interface is run on the local processor. Peripherals such as graphics controllers and MPEG decoders typically use PCI bus as their main interface. The dual ported SDRAM interface can be used to provide a unified memory for the operating system and the video/graphics sub-systems. With the V320USC acting as the main "hub" of the system, very low component count and system cost is achieved without sacrificing performance.

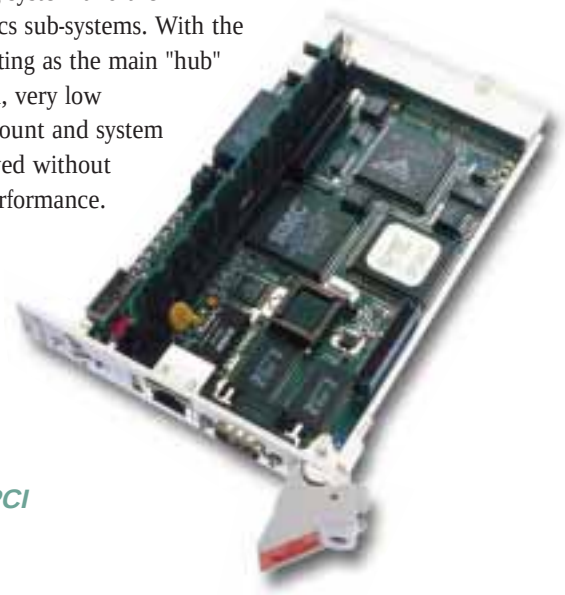


Figure 6.
Monsoon CompactPCI Board

SOFTWARE AND DESIGN SUPPORT

Our goal is to help developers to get their product to market quickly. Software tools, reference designs and evaluation boards are available to accelerate development so that the application developer can concentrate on other areas of the design task that help differentiate their product.

Multiple reference designs are available for the USC and include Orcad schematics, printed circuit artwork, Windows based configuration tools with source code, local processor initialization source code and user documentation. Technical support is available via Email, Fax and phone.

For more information on the V320USC or other V3 products, please contact:

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