Description

The VP464641641B and VP864641641B are 4Mx64-bit and 8Mx64-bit small-outline dual-in-line synchronous dynamic RAM module (SODIMM). It is mounted with 4/8 pieces of 4Mx16 synchronous DRAM (VG36641641BT), and each in a standard 54 pin TSOP package. Decoupling capacitors are mounted on power supply line for noise reduction. The module use serial presence detects implemented via a 2k-bit EEPROM component.

Features

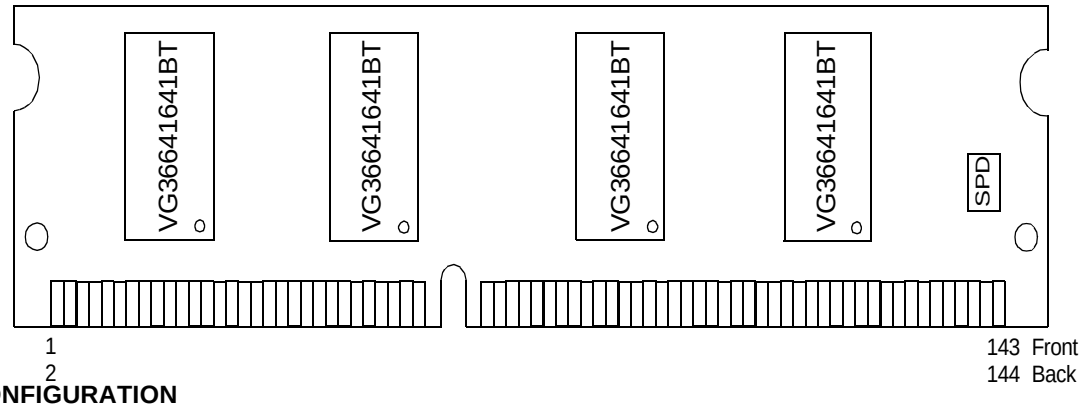
VP464641641B, VP864641641B :

- Comply to Intel pc 100 spuitication
- Single 3.3V (±0.3V) power supply
- Utilizes -8H, -8L, -10 SDRAM components
- 32MB (VP464641641B) and 64MB (VP864641641B)
- Fully synchronous with all signals referenced to a positive clock edge
- Nonbuffered
- Programmable burst length (1,2,4,8 & Full page)
- Programmable wrap sequence (Sequential/Interleave)
- Automatic precharge and controlled precharge
- Auto refresh and self refresh modes
- I/O level : LVTTL interface
- Random column access in every cycle
- 4096 refresh cycles/64ms
- Serial Presence Detect (SPD)
- JEDEC Standard pinout
- Performance Options (at 100MHz)

Marking	SDRAMs	CL	T_{RCD}	T_{RP}	T_{RC}
-8H	-8H	2	2	2	7
-8L	-8L	3	2	2	7
-10	-10	3	3	3	8

unit: clock

PIN ASSIGNMENT (Front View)



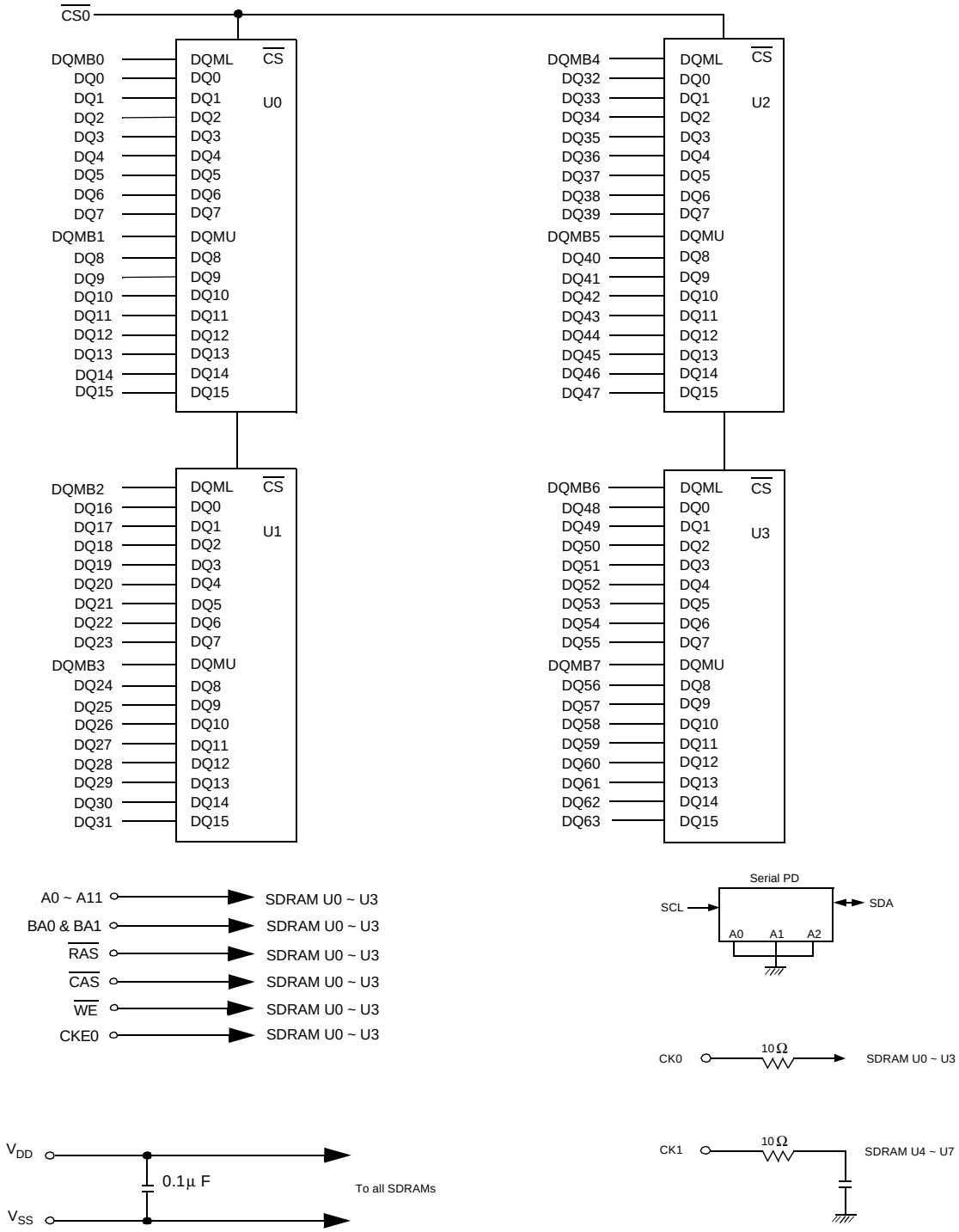
PIN CONFIGURATION

PIN Number	Front side Pin Name	PIN Number	Back side Pin Name	PIN Number	Front side Pin Name	PIN Number	Back side Pin Name
1	V_{SS}	2	V_{SS}	73	NC	74	CK1
3	DQ0	4	DQ32	75	V_{SS}	76	V_{SS}
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	V_{DD}	82	V_{DD}
11	V_{DD}	12	V_{DD}	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	V_{SS}	92	V_{SS}
21	V_{SS}	22	V_{SS}	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	V_{DD}	28	V_{DD}	99	DQ23	100	DQ55
29	A0	30	A3	101	V_{DD}	102	V_{DD}
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	V_{SS}	36	V_{SS}	107	V_{SS}	108	V_{SS}
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10	112	A11
41	DQ10	42	DQ42	113	V_{DD}	114	V_{DD}
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	V_{DD}	46	V_{DD}	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	V_{SS}	120	V_{SS}
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	54	DQ46	123	DQ25	124	DQ57
53	DQ15	56	DQ47	125	DQ26	126	DQ58
55	V_{SS}	58	V_{SS}	127	DQ27	128	DQ59
57	NC	60	NC	129	V_{DD}	130	V_{DD}
59	NC	64	NC	131	DQ28	132	DQ60
61	CK0	66	CKE0	133	DQ29	134	DQ61
63	V_{DD}	68	V_{DD}	135	DQ30	136	DQ62
65	$\overline{RAS}$	70	$\overline{CAS}$	137	DQ31	138	DQ63
67	$\overline{WE}$	74	CKE1	139	V_{SS}	140	V_{SS}
69	$\overline{CS0}$	76	NC	141	SDA	142	SCL
71	$\overline{CS1}$	78	NC	143	V_{DD}	144	V_{DD}

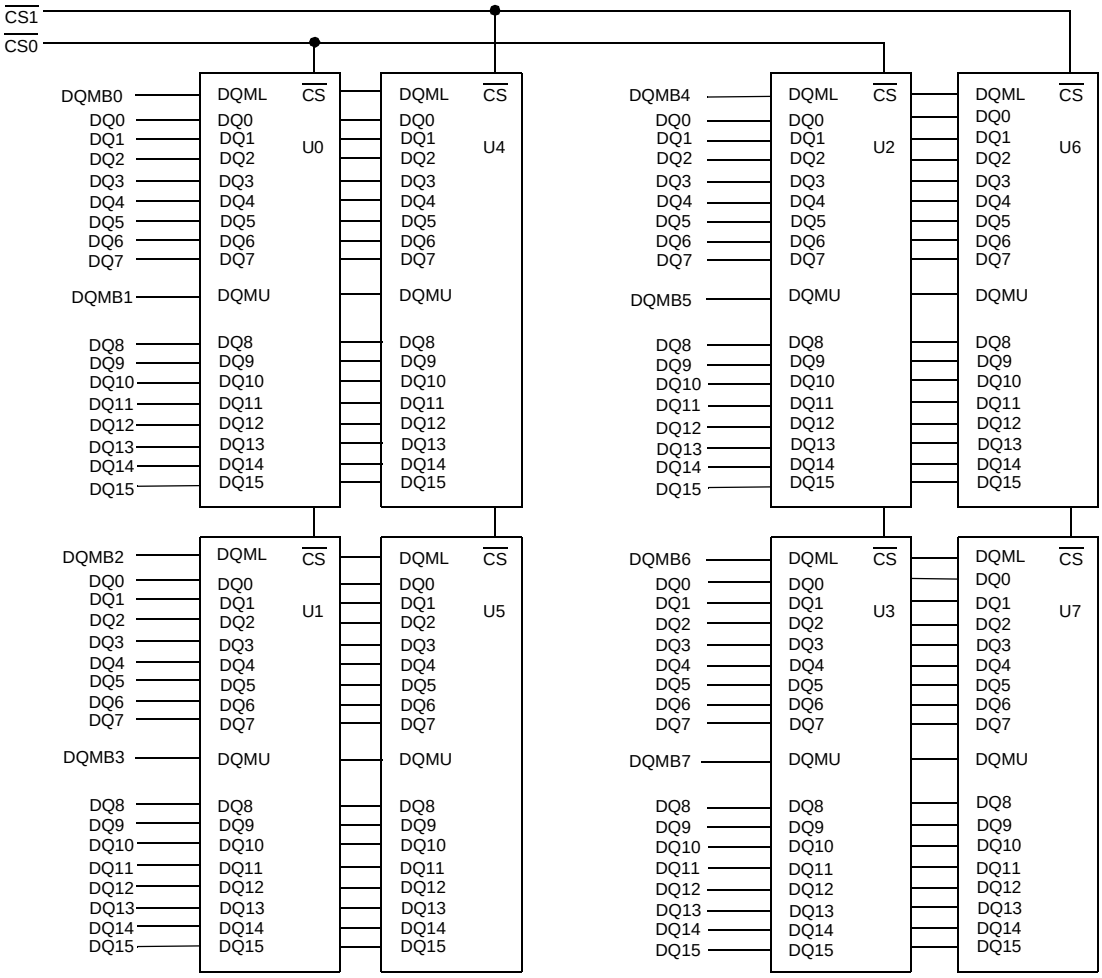
PIN DESCRIPTION

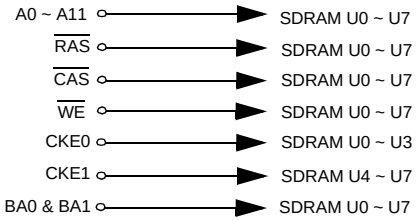
Pin Name	Function	Pin Name	Function
A0 ~ A11	Address input	DQMB0 ~ DQMB7	DQ mask enable
DQ0 ~ DQ63	Data-in/Data - out	CK0, CK1	Clock input
$\overline{RAS}$	Row address strobe	V_{DD}	power
$\overline{CAS}$	Column address strobe	V_{SS}	Ground
$\overline{WE}$	Write enable		
BA0, BA1	Bank address	SCL	Serial clock
CKE	Clock enable	SDA	Serial data I/O
$\overline{CS0}$, $\overline{CS1}$	Chip select	NC	No connect

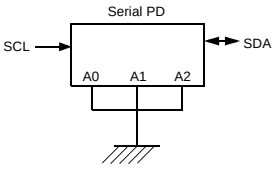
Block Diagram (4M x 64)

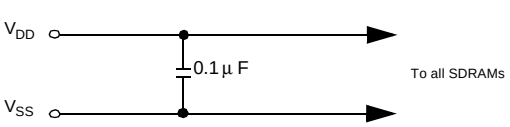


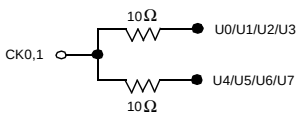
Block Diagram (8M x 64)











Command Truth Table

FUNCTION	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10	A0 - A9 A11
		n - 1	n							
Device deselect	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	X	X	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V
Read	READ	H	X	L	H	L	H	V	L	V
Read with auto precharge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	X	L	H	L	L	V	H	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Burst stop	BST	H	X	L	H	H	L	X	X	X

H : High Level, L : Low Level, V : Valid, X : Don't Care, n : CK cycle number

Absolute Maximum Ratings

Parameter	Symbol	Value		Unit
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-1.0 to +4.6		V
Supply voltage relative to Vss	V_{DD},V_{DDQ}	-1.0 to +4.6		V
Short circuit out put current	I_{OUT}	50		mA
Power dissipation	P_D	4Mx64	4	W
		8Mx64	8	
Operating temperature	T_{OPT}	0 to +70		°C
Storage temperature	T_{STG}	-55 to +125		°C

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Input High Voltage, all inputs	V_{IH}	2.0	-	V_{DD} + 0.3	V	1
Input Low Voltage, all inputs	V_{IL}	-0.3	-	0.8	V	2

Note 1. Overshoot limit: $V_{IH(max.)}$= V_{DDQ} + 2.0V with a pulse width < 3ns

2. Undershoot limit: V_{IL}=V_{SSQ} - 2.0V with a pulse < 3ns and -1.5V with a pulse < 5ns

Capacitance

Ta = 25°C,f = 1MHz

Parameter	Symbol	Size	Typ	Max	Unit
Input capacitance (Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ BA0, BA1)	C11	4M x 64 8M x 64	-	50 85	pF
Input capacitance (CS0, CS1)	C12	4M x 64 8M x 64	-	25 25	pF
Input capacitance (CKE0, CKE1)	C13	4M x 64 8M x 64	-	50 50	pF
Input capacitance (CK0~CK1)	C14	4M x 64 8M x 64	-	25 25	pF
Input capacitance(DQMB0 ~ DQMB7)	C15	4M x 64 8M x 64	-	15 22	pF
Data input/output capacitance(DQ0 ~ DQ63)	C16	4M x 64 8M x 64	-	14 20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test Conditions		VP464641641B						Unit	Notes
				-8H		-8L		-10			
				Min	Max	Min	Max	Min	Max		
Operating current	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC\ (MIN.)}$, Io = 0mA One bank active	CL = 3		420		420		380	mA	1,2
			CL = 2		400		400		350		
Precharge standby current in power down mode	$I_{CC2}P$	CKE ≤ $V_{IL(MAX.)}$ t_{CK} = 10ns			12		12		12	mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL(MAX)}$ t_{CK} = ∞			8		8		8		
Precharge standby current in Nonpower down mode	$I_{CC2}N$	CKE ≥ $V_{IH(MIN.)}$ t_{CK} = 10ns CS ≥ $V_{IH(MIN.)}$ Input signals are changed. one time during 30ns.			100		100		100	mA	
	$I_{CC2}NS$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = ∞ CLK ≤ $V_{IL(MAX.)}$ Input signals are stable.			30		30		30		
Active standby current in power down mode	$I_{CC3}P$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 10ns			25		25		25	mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞			20		20		20		
Active standby current in nonpower down mode	$I_{CC3}N$	CKE ≥ $V_{IH(MAX.)}$, t_{CK} = 10ns CS ≥ $V_{IH(MIN.)}$ Input signals are changed one time during 30ns			100		100		100	mA	
	$I_{CC3}NS$	CKE ≥ $V_{IH(MIN.)}$ t_{CK} = ∞ CLE ≤ $V_{IL(MAX.)}$ Input signals are stable.			50		50		50		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\ (MIN.)}$,Io = 0mA Burst length = 4	CL = 3		500		500		400	mA	1,2
			CL = 2		330		330		260		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC(MIN.)}$	CL = 3		550		550		480	mA	2
			CL = 2		525		525		525		
Self refresh current	I_{CC6}	CKE ≤ 0.2V			8		8		8	mA	
Input leakage current	I_{LI}	$V_{IN} \geq 0$, $V_{IN} \leq V_{DD}$ + 0.3V Pins not under test = 0V		-40	40	-40	40	-40	40	uA	
Output leakage current	I_{LO}	$V_{OUT} \geq 0$, $V_{OUT} \leq V_{DD}$ + 0.3V DQ# in H - Z., Dout disabled		-5	5	-5	5	-5	5	uA	
Output Low Voltage	V_{OL}	I_{OL} = 2mA			0.4		0.4		0.4	V	
Output High Voltage	V_{OH}	I_{OH} = -2mA		2.4		2.4		2.4		V	

Notes 1. I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.

2. I_{CC} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test Conditions		VP864641641B						Unit	Notes
				-8H		-8L		10			
				Min	Max	Min	Max	Min	Max		
Operating current	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC\ (MIN.)}$, Io = 0mA One bank active	CL = 3		450		450		420	mA	1,2
			CL = 2		430		430		380		
Precharge standby current in power down mode	$I_{CC2}P$	CKE $\leq V_{IL(MAX.)}$ t_{CK} = 15ns			24		24		24	mA	
	$I_{CC2}PS$	CKE $\leq V_{IL(MAX)}$ $t_{CK} = \infty$			16		16		16		
Precharge standby current in Nonpower down mode	$I_{CC2}N$	CKE $\geq V_{IH(MIN.)}$ t_{CK} = 15ns CS $\geq V_{IH(MIN.)}$ Input signals are changed. one time during 30ns.			200		200		200	mA	
	$I_{CC2}NS$	CKE $\geq V_{IH(MIN.)}$, $t_{CK} = \infty$ CLK $\leq V_{IL(MAX.)}$ Input signals are stable.			60		60		60		
Active standby current in power down mode	$I_{CC3}P$	CKE $\leq V_{IL(MAX.)}$, t_{CK} = 15ns			45		45		45	mA	
	$I_{CC3}PS$	CKE $\leq V_{IL(MAX.)}$, $t_{CK} = \infty$			40		40		40		
Active standby current in nonpower down mode	$I_{CC3}N$	CKE $\geq V_{IL(MAX.)}$, t_{CK} = 15ns CS $\geq V_{IL(MIN.)}$ Input signals are changed one time during 30ns			200		200		200	mA	
	$I_{CC3}NS$	CKE $\geq V_{IH(MIN.)}$ $t_{CK} = \infty$ CLE $\leq V_{IL(MAX.)}$ Input signals are stable.			100		100		100		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\ (MIN.)}$, Io = 0mA Burst length=4	CL = 3		510		510		470	mA	1,2
			CL = 2		420		350		280		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC\ (MIN.)}$	CL = 3		550		550		520	mA	2
			CL = 2		520		520		500		
Self refresh current	I_{CC6}	CKE $\leq$ 0.2V			16		16		16	mA	
Input leakage current	I_{LI}	$V_{IN} \geq 0$, $V_{IN} \leq V_{DD}$ + 0.3V Pins not under test = 0V		-80	80	-80	80	-80	80	uA	
Output leakage current	I_{LO}	$V_{OUT} \geq 0$, $V_{OUT} \leq V_{DD}$ + 0.3V DQ# in H - Z., Dout disabled		-10	10	-10	10	-10	10	uA	
Output Low Voltage	V_{OL}	I_{OL} = 2mA			0.4		0.4		0.4	V	
Output High Voltage	V_{OH}	I_{OH} = -2mA		2.4		2.4		2.4		V	

Notes 1. I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.

2. I_{CC} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

A.C Characteristics

Test Conditions : (Ta = 0 to 70°C V_{DD} = 3.3V±0.3V , V_{SS} = 0V)

AC input Levels(V_{IH}/V_{IL})	2.0/0.8V	Input timing reference level/ Output timing reference level	1.4v
Input and fall time	1ns	Output load condition	50pF

Parameter	CAS Latency	symbol	VP464641641B/VP864641641B						Unit
			-8H		-8L		-10		
			Min	Max	Min	Max	Min	Max	
CLK cycle time	3	t_{CK3}	8		8		10		ns
	2	t_{CK2}	10		12		15		ns
CLK to valid output delay	3	t_{AC3}		6		6		7	ns
	2	t_{AC2}		6		8		8	ns
CLK high pulse width		t_{CH}	3		3		3		ns
CLK low pulse width		t_{CL}	3		3		3		ns
CKE setup time		t_{CKS}	2		2		2		ns
CKE hold time		t_{CKH}	1		1		1		ns
Address setup time		t_{AS}	2		2		2		ns
Address hold time		t_{AH}	1		1		1		ns
Command setup time		t_{CMS}	2		2		2		ns
Command hold time		t_{CMH}	1		1		1		ns
Data - in setup time		t_{DS}	2		2		2		ns
Data - in hold time		t_{DH}	1		1		1		ns
Output data hold time		t_{OH}	3		3		3		ns
CLK to output on low - Z		t_{LZ}	0		0		0		ns
CLK to output in Hi - Z	3	t_{HZ}		6		6		7	ns
	2			6		8		8	
CLK to output in Hi - Z without load		t_{OHN}	1		2		2		ns
Row active to active delay		t_{RRD}	16		20		24		ns
RAS to CAS delay		t_{RCD}	20		20		20		ns
Row precharge time		t_{RP}	20		24		30		ns
Row active time		t_{RAS}	46	120K	46	120K	50	120K	ns
Row cycle time		t_{RC}	70		70		80		ns
Last data in to burst stop		t_{BDL}	1CLK		1CLK		1CLK		ns
Data - in to ACT (REF) command (Auto Precharge)		t_{DAL}	1CLK + t_{RP}		1CLK + t_{RP}		1CLK + t_{RP}		ns
Data - in to precharge		t_{DPL}	1 CLK		1 CLK		1 CLK		ns
Transition time		t_{T}	1	10	1	10	1	10	ns
Mode reg. set cycle		t_{RSC}	2 CLK		2 CLK		2 CLK		ns
Power down exit setup time		t_{PDE}	2		3		3		ns
Self refresh exit time		t_{SRX}	1		1		1		ns
Refresh time		t_{REF}		64		64		64	ms

Serial presence detect information

32 MB

Byte	Function described	Function Supported			HEX		
		-8H	-8L	10	-8H	-8L	10
0	Number of bytes used by Vanguard	128 bytes			80		
1	Total SPD memory size	256 bytes			08		
2	Memory Type	SDRAM			04		
3	Number of Row addresses	12			0C		
4	Number of Column addresses	8			08		
5	Number of Banks on module	1 row			01		
6	Module data width	64 bits			40		
7	Module data width (continued)	0			00		
8	Module voltage interface levels	LVTTL			01		
9	SDRAM cycle time. CAS latency = 3	8ns	8ns	10ns	80	80	A0
10	SDRAM access from clock. CAS latency = 3	6ns	6ns	7ns	60	60	70
11	Module configuration type	Non-Parity			00		
12	Refresh Rate/Type	15.6us/self			80		
13	SDRAM width, Primary SDRAM	x16			10		
14	Error checking SDRAM data width	N/A			00		
15	Min. clock delay, Back to back random column address	1			01		
16	Burst length supported	1,2,4,8,Page			8F		
17	Number of banks on each SDRAM device	4			04		
18	CAS latencies supported	2 & 3			06		
19	CS latency	0 CLK			01		
20	Write latency	0 CLK			01		
21	SDRAM module attributes	Non-buffered			00		
22	SDRAM device attributes : general	0E			0E		
23	SDRAM cycle time. CAS latency = 2	10ns	12ns	15ns	A0	18	1E
24	SDRAM access from clock. CAS latency = 2	6ns	8ns	8ns	60	14	18
27	Min. row precharge time	20ns	24ns	30ns	14	14	14
28	Min. row active to row active	16ns	20ns	24ns	10	2E	32
29	Min. RAS to CAS delay	20ns	20ns	20ns	14	08	08
30	Min. RAS pulse width	46ns	46ns	50ns	2E	12	12
31	Module bank density	32MB			08		
62	SPD data revision code	Rev.1, 2			12		
63	Checksum for bytes 0-62	Checksum data			7C	9E	DC
64	Manufacturer ' s JEDEC ID code	Continuation code			7F		
65	Manufacturer ' s JEDEC ID code	Vanguard			29		
66-71	Manufacturer ' s JEDEC ID code	None			FF		

Byte	Function described	Function Supported			HEX		
		-8H	-8L	10	-8H	-8L	10
72	Manufacturering location	-			-		
73	Manufacture's part number	V			56		
74	Manufacture's part number	P			50		
75	Manufacture's part number	4			34		
76	Manufacture's part number	6			36		
77	Manufacture's part number	4			34		
78	Manufacture's part number	6			36		
79	Manufacture's part number	4			34		
80	Manufacture's part number	1			31		
81	Manufacture's part number	6			36		
82	Manufacture's part number	4			34		
83	Manufacture's part number	1			31		
84	Manufacture's part number	B			42		
85	Manufacture's part number	T			54		
86	Manufacture's part number	G(Gold lead) S(Tin lead)			47 53		
87	Manufacture's part number	A			41		
88	Manufacture's part number	"-"			2D		
89	Manufacture's part number	8	8	10	38	38	40
90	Manufacture's part number	H	L	Blank	48	4C	20
91	Revision code for PCB	A			41		
92	Revision code	Blank			20		
93~94	Manufacturing data	Year/Week code			-		
95~98	Module serial number	Serial number			-		
99~125	Manufacturer specific data	-			-		
126	Module supports clock frequency	100Mhz			64		
127	Intel specification details	Detail 100MHz information			AF	AD	AD
128~255	For customer usc	None			FF		

Serial presence detect information

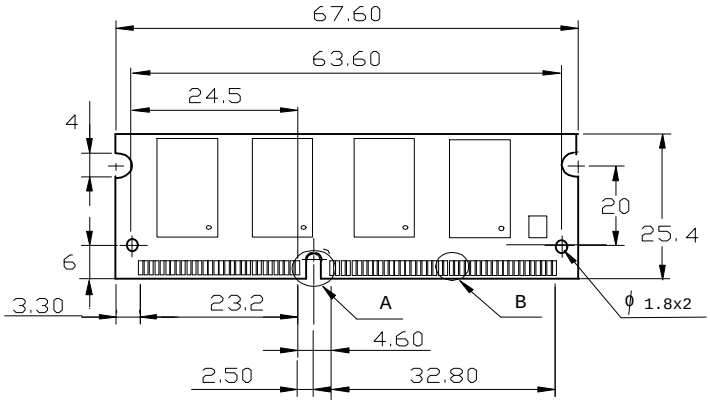
64 MB

Byte	Function described	Function Supported			HEX		
		-8H	-8L	10	-8H	-8L	10
0	Number of bytes used by Vanguard	128 bytes			80		
1	Total SPD memory size	256 bytes			08		
2	Memory Type	SDRAM			04		
3	Number of Row addresses	12			0C		
4	Number of Column addresses	8			08		
5	Number of Banks on module	2 row			02		
6	Module data width	64 bits			40		
7	Module data width (continued)	0			00		
8	Module voltage interface levels	LVTTL			01		
9	SDRAM cycle time. CAS latency = 3	8ns	8ns	10ns	80	80	A0
10	SDRAM access from clock. CAS latency = 3	6ns	6ns	7ns	60	60	70
11	Module configuration type	Non-Parity			00		
12	Refresh Rate/Type	15.6us/self			80		
13	SDRAM width, Primary SDRAM	x16			10		
14	Error checking SDRAM data width	N/A			00		
15	Min. clock delay, Back to back random column address	1			01		
16	Burst length supported	1,2,4,8,Page			8F		
17	Number of banks on each SDRAM device	4			04		
18	CAS latencies supported	2 & 3			06		
19	CS latency	0 CLK			01		
20	Write latency	0 CLK			01		
21	SDRAM module attributes	Non-buffered			00		
22	SDRAM device attributes : general	0E			0E		
23	SDRAM cycle time. CAS latency = 2	10ns	12ns	15ns	A0	18	1E
24	SDRAM access from clock. CAS latency = 2	6ns	8ns	8ns	60	14	18
27	Min. row precharge time	20ns	24ns	30ns	14	14	14
28	Min. row active to row active	16ns	20ns	24ns	10	2E	32
29	Min. RAS to CAS delay	20ns	20ns	20ns	14	08	08
30	Min. RAS pulse width	46ns	46ns	50ns	2E	12	12
31	Module bank density	32MB			08		
62	SPD data revision code	Rev.1, 2			12		
63	Checksum for bytes 0-62	Checksum data			7D	9F	DD
64	Manufacturer ’s JEDEC ID code	Continuation code			7F		
65	Manufacturer ’ s JEDEC ID code	Vanguard			29		
66-71	Manufacturer ’ s JEDEC ID code	None			FF		

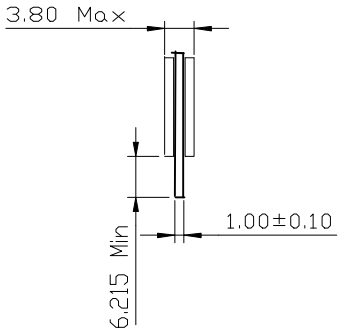
Byte	Function described	Function Supported			HEX		
		-8H	-8L	10	-8H	-8L	10
72	Manufacturering location	-			-		
73	Manufacture's part number	V			56		
74	Manufacture's part number	P			50		
75	Manufacture's part number	8			38		
76	Manufacture's part number	6			36		
77	Manufacture's part number	4			34		
78	Manufacture's part number	6			36		
79	Manufacture's part number	4			34		
80	Manufacture's part number	1			31		
81	Manufacture's part number	6			36		
82	Manufacture's part number	4			34		
83	Manufacture's part number	1			31		
84	Manufacture's part number	B			42		
85	Manufacture's part number	T			54		
86	Manufacture's part number	G(Gold lead) S(Tin lead)			47 53		
87	Manufacture's part number	A			41		
88	Manufacture's part number	"-"			2D		
89	Manufacture's part number	8	8	10	38	38	40
90	Manufacture's part number	H	L	Blank	48	4C	20
91	Revision code for PCB	A			41		
92	Revision code	Blank			20		
93~94	Manufacturing data	Year/Week code			-		
95~98	Module serial number	Serial number			-		
99~125	Manufacturer specific data	-			-		
126	Module supports clock frequency	100Mhz			64		
127	Intel specification details	Detail 100MHz information			FF	FD	FD
128~255	For customer usc	None			FF		

144 Pin SODIMM Mechanical Dimension(Front Side)

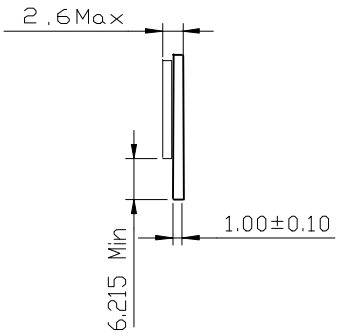
Front



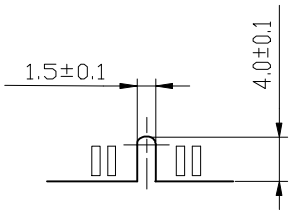
8Mx64 Side



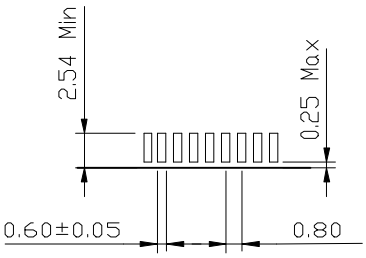
4Mx64 Side



Detail A



Detail B



NOTE : The use device is TSOP SDRAM

All dimensions are typical unless otherwise stated. (MILLIMETERS)

Ordering Information

	1	2	3	4	5	6	7	8	9	10
V	X	XX	XX	XXXXXX	X	X	X	X	X	-X

V : VIS Product
1 : RAM Family
P: SDRAM SODIMM(144pin)

2 : Memory density (work)
4 : 4M
8 : 8M

3 : I/O width
64 : X 64

4 : Operation mode and refresh with different density
641641 : 4K ref., 4M X16 SDRAM

5 : Component revision
Blank : None
A : A revision
B : B revision
C : C revision

6 : Component Package
T : TSOP

7 : PC board finger plating
G : Gold
S : Tin/lead

8 : PC board revision
Blank : none
A : A revision
B : B revision
C : C revision

9 : Customer specific
Blank : none

10 : Module speed
-8H : 100Mhz, CL = 2, t_{RP} = 2, t_{RCD} = 2
-8L : 100Mhz, CL = 3, t_{RP} = 2, t_{RCD} = 2
-10 : 100Mhz, CL = 3, t_{RP} = 3, t_{RCD} = 3

Description

The VP464641641B and VP864641641B are 4Mx64-bit and 8Mx64-bit small-outline dual-in-line synchronous dynamic RAM module (SODIMM). It is mounted with 4/8 pieces of 4Mx16 synchronous DRAM (VG36641641BT), and each in a standard 54 pin TSOP package. Decoupling capacitors are mounted on power supply line for noise reduction. The module use serial presence detects implemented via a 2k-bit EEPROM component.

Features

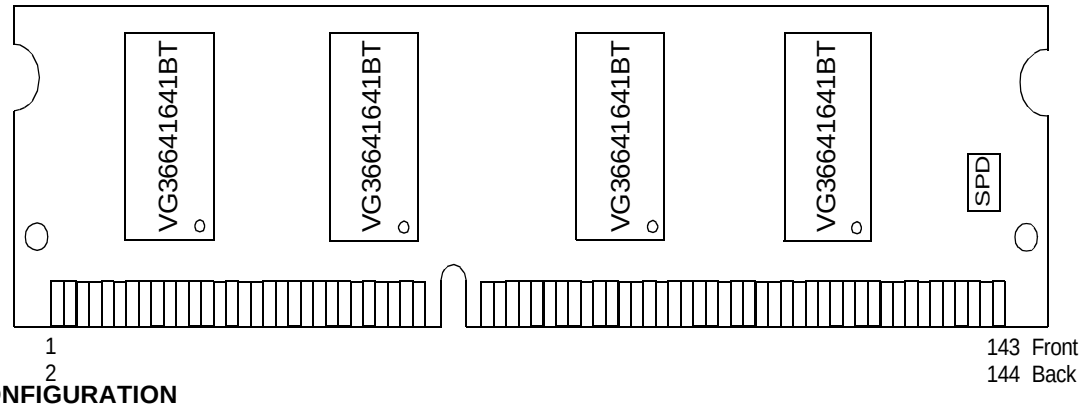
VP464641641B, VP864641641B :

- Comply to Intel pc 100 spuitication
- Single 3.3V (±0.3V) power supply
- Utilizes -8H, -8L, -10 SDRAM components
- 32MB (VP464641641B) and 64MB (VP864641641B)
- Fully synchronous with all signals referenced to a positive clock edge
- Nonbuffered
- Programmable burst length (1,2,4,8 & Full page)
- Programmable wrap sequence (Sequential/Interleave)
- Automatic precharge and controlled precharge
- Auto refresh and self refresh modes
- I/O level : LVTTL interface
- Random column access in every cycle
- 4096 refresh cycles/64ms
- Serial Presence Detect (SPD)
- JEDEC Standard pinout
- Performance Options (at 100MHz)

Marking	SDRAMs	CL	T_{RCD}	T_{RP}	T_{RC}
-8H	-8H	2	2	2	7
-8L	-8L	3	2	2	7
-10	-10	3	3	3	8

unit: clock

PIN ASSIGNMENT (Front View)



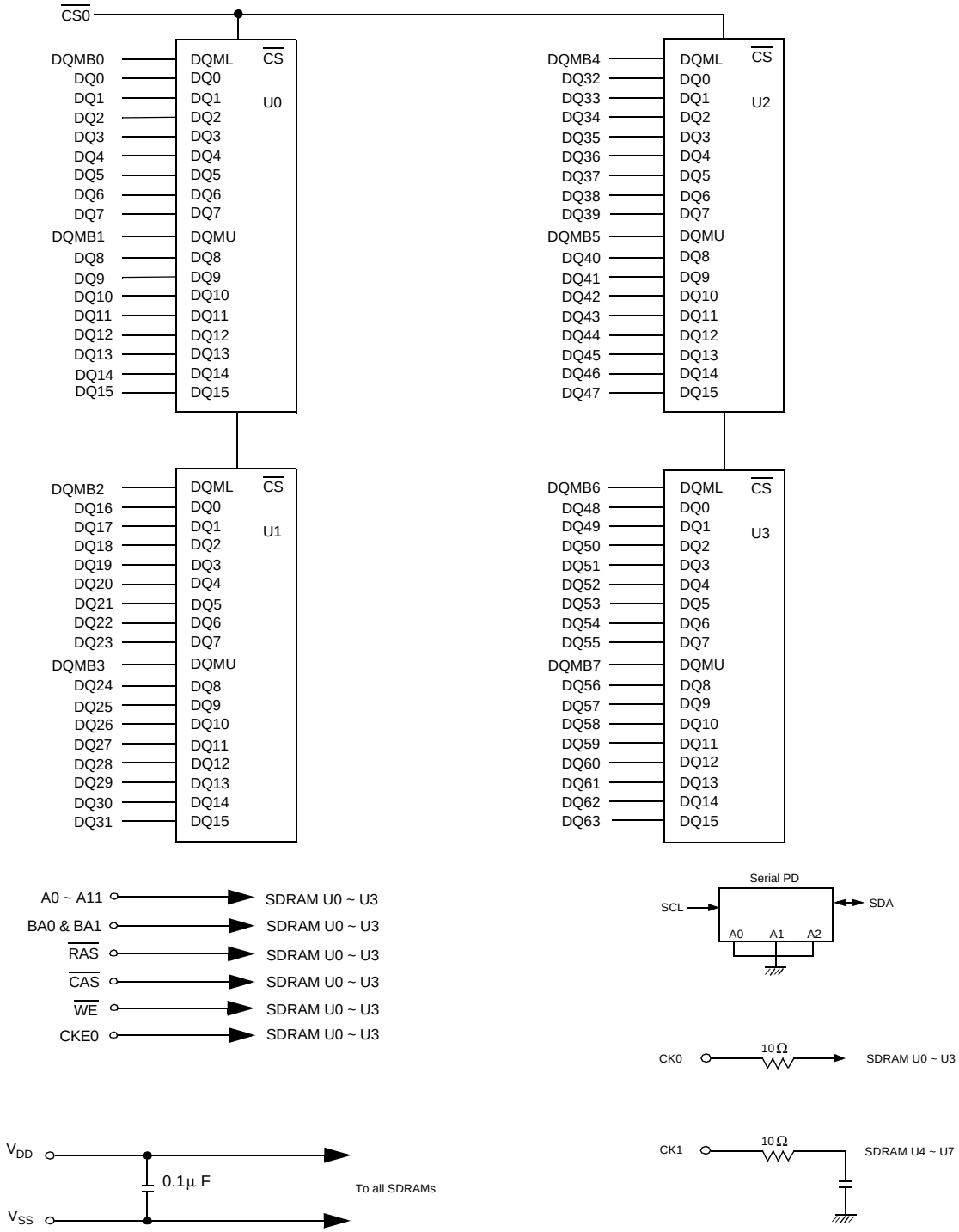
PIN CONFIGURATION

PIN Number	Front side Pin Name	PIN Number	Back side Pin Name	PIN Number	Front side Pin Name	PIN Number	Back side Pin Name
1	V_{SS}	2	V_{SS}	73	NC	74	CK1
3	DQ0	4	DQ32	75	V_{SS}	76	V_{SS}
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	V_{DD}	82	V_{DD}
11	V_{DD}	12	V_{DD}	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	V_{SS}	92	V_{SS}
21	V_{SS}	22	V_{SS}	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	V_{DD}	28	V_{DD}	99	DQ23	100	DQ55
29	A0	30	A3	101	V_{DD}	102	V_{DD}
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	V_{SS}	36	V_{SS}	107	V_{SS}	108	V_{SS}
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10	112	A11
41	DQ10	42	DQ42	113	V_{DD}	114	V_{DD}
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	V_{DD}	46	V_{DD}	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	V_{SS}	120	V_{SS}
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	54	DQ46	123	DQ25	124	DQ57
53	DQ15	56	DQ47	125	DQ26	126	DQ58
55	V_{SS}	58	V_{SS}	127	DQ27	128	DQ59
57	NC	60	NC	129	V_{DD}	130	V_{DD}
59	NC	64	NC	131	DQ28	132	DQ60
61	CK0	66	CKE0	133	DQ29	134	DQ61
63	V_{DD}	68	V_{DD}	135	DQ30	136	DQ62
65	$\overline{RAS}$	70	$\overline{CAS}$	137	DQ31	138	DQ63
67	$\overline{WE}$	74	CKE1	139	V_{SS}	140	V_{SS}
69	$\overline{CS0}$	76	NC	141	SDA	142	SCL
71	$\overline{CS1}$	78	NC	143	V_{DD}	144	V_{DD}

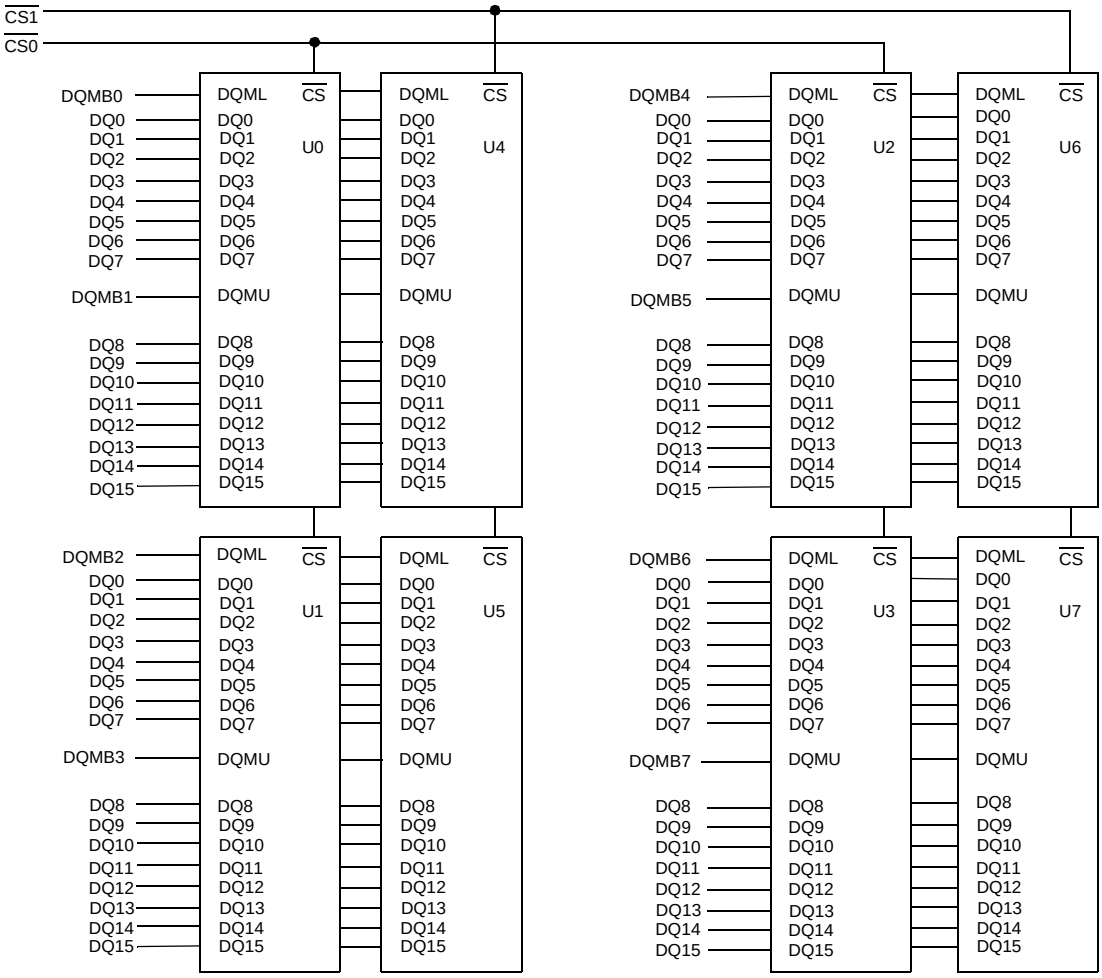
PIN DESCRIPTION

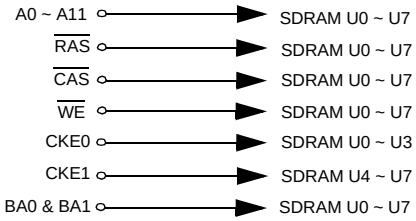
Pin Name	Function	Pin Name	Function
A0 ~ A11	Address input	DQMB0 ~ DQMB7	DQ mask enable
DQ0 ~ DQ63	Data-in/Data - out	CK0, CK1	Clock input
$\overline{RAS}$	Row address strobe	V_{DD}	power
$\overline{CAS}$	Column address strobe	V_{SS}	Ground
$\overline{WE}$	Write enable		
BA0, BA1	Bank address	SCL	Serial clock
CKE	Clock enable	SDA	Serial data I/O
$\overline{CS0}$, $\overline{CS1}$	Chip select	NC	No connect

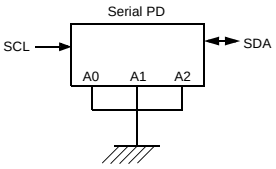
Block Diagram (4M x 64)

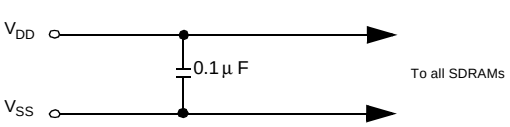


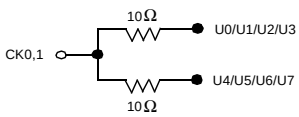
Block Diagram (8M x 64)











Command Truth Table

FUNCTION	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10	A0 - A9 A11
		n - 1	n							
Device deselect	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	X	X	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V
Read	READ	H	X	L	H	L	H	V	L	V
Read with auto precharge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	X	L	H	L	L	V	H	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Burst stop	BST	H	X	L	H	H	L	X	X	X

H : High Level, L : Low Level, V : Valid, X : Don't Care, n : CK cycle number

Absolute Maximum Ratings

Parameter	Symbol	Value		Unit
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-1.0 to +4.6		V
Supply voltage relative to Vss	V_{DD},V_{DDQ}	-1.0 to +4.6		V
Short circuit out put current	I_{OUT}	50		mA
Power dissipation	P_D	4Mx64	4	W
		8Mx64	8	
Operating temperature	T_{OPT}	0 to +70		°C
Storage temperature	T_{STG}	-55 to +125		°C

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Input High Voltage, all inputs	V_{IH}	2.0	-	V_{DD} + 0.3	V	1
Input Low Voltage, all inputs	V_{IL}	-0.3	-	0.8	V	2

Note 1. Overshoot limit: $V_{IH(max.)}$= V_{DDQ} + 2.0V with a pulse width < 3ns

2. Undershoot limit: V_{IL}=V_{SSQ} - 2.0V with a pulse < 3ns and -1.5V with a pulse < 5ns

Capacitance

Ta = 25°C,f = 1MHz

Parameter	Symbol	Size	Typ	Max	Unit
Input capacitance (Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ BA0, BA1)	C11	4M x 64 8M x 64	-	50 85	pF
Input capacitance (CS0, CS1)	C12	4M x 64 8M x 64	-	25 25	pF
Input capacitance (CKE0, CKE1)	C13	4M x 64 8M x 64	-	50 50	pF
Input capacitance (CK0~CK1)	C14	4M x 64 8M x 64	-	25 25	pF
Input capacitance(DQMB0 ~ DQMB7)	C15	4M x 64 8M x 64	-	15 22	pF
Data input/output capacitance(DQ0 ~ DQ63)	C16	4M x 64 8M x 64	-	14 20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test Conditions		VP464641641B						Unit	Notes
				-8H		-8L		-10			
				Min	Max	Min	Max	Min	Max		
Operating current	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC\ (MIN.)}$, Io = 0mA One bank active	CL = 3		420		420		380	mA	1,2
			CL = 2		400		400		350		
Precharge standby current in power down mode	$I_{CC2}P$	CKE ≤ $V_{IL(MAX.)}$ t_{CK} = 10ns			12		12		12	mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL(MAX)}$ t_{CK} = ∞			8		8		8		
Precharge standby current in Nonpower down mode	$I_{CC2}N$	CKE ≥ $V_{IH(MIN.)}$ t_{CK} = 10ns CS ≥ $V_{IH(MIN.)}$ Input signals are changed. one time during 30ns.			100		100		100	mA	
	$I_{CC2}NS$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = ∞ CLK ≤ $V_{IL(MAX.)}$ Input signals are stable.			30		30		30		
Active standby current in power down mode	$I_{CC3}P$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 10ns			25		25		25	mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞			20		20		20		
Active standby current in nonpower down mode	$I_{CC3}N$	CKE ≥ $V_{IH(MAX.)}$, t_{CK} = 10ns CS ≥ $V_{IH(MIN.)}$ Input signals are changed one time during 30ns			100		100		100	mA	
	$I_{CC3}NS$	CKE ≥ $V_{IH(MIN.)}$ t_{CK} = ∞ CLE ≤ $V_{IL(MAX.)}$ Input signals are stable.			50		50		50		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\ (MIN.)}$,Io = 0mA Burst length = 4	CL = 3		500		500		400	mA	1,2
			CL = 2		330		330		260		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC(MIN.)}$	CL = 3		550		550		480	mA	2
			CL = 2		525		525		525		
Self refresh current	I_{CC6}	CKE ≤ 0.2V			8		8		8	mA	
Input leakage current	I_{LI}	$V_{IN} \geq 0$, $V_{IN} \leq V_{DD}$ + 0.3V Pins not under test = 0V		-40	40	-40	40	-40	40	uA	
Output leakage current	I_{LO}	$V_{OUT} \geq 0$, $V_{OUT} \leq V_{DD}$ + 0.3V DQ# in H - Z., Dout disabled		-5	5	-5	5	-5	5	uA	
Output Low Voltage	V_{OL}	I_{OL} = 2mA			0.4		0.4		0.4	V	
Output High Voltage	V_{OH}	I_{OH} = -2mA		2.4		2.4		2.4		V	

Notes 1. I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.

2. I_{CC} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test Conditions		VP864641641B						Unit	Notes
				-8H		-8L		10			
				Min	Max	Min	Max	Min	Max		
Operating current	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC\ (MIN.)}$, Io = 0mA One bank active	CL = 3		450		450		420	mA	1,2
			CL = 2		430		430		380		
Precharge standby current in power down mode	$I_{CC2}P$	CKE $\leq V_{IL(MAX.)}$ t_{CK} = 15ns			24		24		24	mA	
	$I_{CC2}PS$	CKE $\leq V_{IL(MAX)}$ $t_{CK} = \infty$			16		16		16		
Precharge standby current in Nonpower down mode	$I_{CC2}N$	CKE $\geq V_{IH(MIN.)}$ t_{CK} = 15ns CS $\geq V_{IH(MIN.)}$ Input signals are changed. one time during 30ns.			200		200		200	mA	
	$I_{CC2}NS$	CKE $\geq V_{IH(MIN.)}$, $t_{CK} = \infty$ CLK $\leq V_{IL(MAX.)}$ Input signals are stable.			60		60		60		
Active standby current in power down mode	$I_{CC3}P$	CKE $\leq V_{IL(MAX.)}$, t_{CK} = 15ns			45		45		45	mA	
	$I_{CC3}PS$	CKE $\leq V_{IL(MAX.)}$, $t_{CK} = \infty$			40		40		40		
Active standby current in nonpower down mode	$I_{CC3}N$	CKE $\geq V_{IL(MAX.)}$, t_{CK} = 15ns CS $\geq V_{IL(MIN.)}$ Input signals are changed one time during 30ns			200		200		200	mA	
	$I_{CC3}NS$	CKE $\geq V_{IH(MIN.)}$ $t_{CK} = \infty$ CLE $\leq V_{IL(MAX.)}$ Input signals are stable.			100		100		100		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\ (MIN.)}$, Io = 0mA Burst length=4	CL = 3		510		510		470	mA	1,2
			CL = 2		420		350		280		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC\ (MIN.)}$	CL = 3		550		550		520	mA	2
			CL = 2		520		520		500		
Self refresh current	I_{CC6}	CKE $\leq$ 0.2V			16		16		16	mA	
Input leakage current	I_{LI}	$V_{IN} \geq 0$, $V_{IN} \leq V_{DD}$ + 0.3V Pins not under test = 0V		-80	80	-80	80	-80	80	uA	
Output leakage current	I_{LO}	$V_{OUT} \geq 0$, $V_{OUT} \leq V_{DD}$ + 0.3V DQ# in H - Z., Dout disabled		-10	10	-10	10	-10	10	uA	
Output Low Voltage	V_{OL}	I_{OL} = 2mA			0.4		0.4		0.4	V	
Output High Voltage	V_{OH}	I_{OH} = -2mA		2.4		2.4		2.4		V	

Notes 1. I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.

2. I_{CC} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

A.C Characteristics

Test Conditions : (Ta = 0 to 70°C V_{DD} = 3.3V±0.3V , V_{SS} = 0V)

AC input Levels(V_{IH}/V_{IL})	2.0/0.8V	Input timing reference level/ Output timing reference level	1.4v
Input and fall time	1ns	Output load condition	50pF

Parameter	CAS Latency	symbol	VP464641641B/VP864641641B						Unit
			-8H		-8L		-10		
			Min	Max	Min	Max	Min	Max	
CLK cycle time	3	t_{CK3}	8		8		10		ns
	2	t_{CK2}	10		12		15		ns
CLK to valid output delay	3	t_{AC3}		6		6		7	ns
	2	t_{AC2}		6		8		8	ns
CLK high pulse width		t_{CH}	3		3		3		ns
CLK low pulse width		t_{CL}	3		3		3		ns
CKE setup time		t_{CKS}	2		2		2		ns
CKE hold time		t_{CKH}	1		1		1		ns
Address setup time		t_{AS}	2		2		2		ns
Address hold time		t_{AH}	1		1		1		ns
Command setup time		t_{CMS}	2		2		2		ns
Command hold time		t_{CMH}	1		1		1		ns
Data - in setup time		t_{DS}	2		2		2		ns
Data - in hold time		t_{DH}	1		1		1		ns
Output data hold time		t_{OH}	3		3		3		ns
CLK to output on low - Z		t_{LZ}	0		0		0		ns
CLK to output in Hi - Z	3	t_{HZ}		6		6		7	ns
	2			6		8		8	
CLK to output in Hi - Z without load		t_{OHN}	1		2		2		ns
Row active to active delay		t_{RRD}	16		20		24		ns
RAS to CAS delay		t_{RCD}	20		20		20		ns
Row precharge time		t_{RP}	20		24		30		ns
Row active time		t_{RAS}	46	120K	46	120K	50	120K	ns
Row cycle time		t_{RC}	70		70		80		ns
Last data in to burst stop		t_{BDL}	1CLK		1CLK		1CLK		ns
Data - in to ACT (REF) command (Auto Precharge)		t_{DAL}	1CLK + t_{RP}		1CLK + t_{RP}		1CLK + t_{RP}		ns
Data - in to precharge		t_{DPL}	1 CLK		1 CLK		1 CLK		ns
Transition time		t_{T}	1	10	1	10	1	10	ns
Mode reg. set cycle		t_{RSC}	2 CLK		2 CLK		2 CLK		ns
Power down exit setup time		t_{PDE}	2		3		3		ns
Self refresh exit time		t_{SRX}	1		1		1		ns
Refresh time		t_{REF}		64		64		64	ms

Serial presence detect information

32 MB

Byte	Function described	Function Supported			HEX		
		-8H	-8L	10	-8H	-8L	10
0	Number of bytes used by Vanguard	128 bytes			80		
1	Total SPD memory size	256 bytes			08		
2	Memory Type	SDRAM			04		
3	Number of Row addresses	12			0C		
4	Number of Column addresses	8			08		
5	Number of Banks on module	1 row			01		
6	Module data width	64 bits			40		
7	Module data width (continued)	0			00		
8	Module voltage interface levels	LVTTL			01		
9	SDRAM cycle time. CAS latency = 3	8ns	8ns	10ns	80	80	A0
10	SDRAM access from clock. CAS latency = 3	6ns	6ns	7ns	60	60	70
11	Module configuration type	Non-Parity			00		
12	Refresh Rate/Type	15.6us/self			80		
13	SDRAM width, Primary SDRAM	x16			10		
14	Error checking SDRAM data width	N/A			00		
15	Min. clock delay, Back to back random column address	1			01		
16	Burst length supported	1,2,4,8,Page			8F		
17	Number of banks on each SDRAM device	4			04		
18	CAS latencies supported	2 & 3			06		
19	CS latency	0 CLK			01		
20	Write latency	0 CLK			01		
21	SDRAM module attributes	Non-buffered			00		
22	SDRAM device attributes : general	0E			0E		
23	SDRAM cycle time. CAS latency = 2	10ns	12ns	15ns	A0	18	1E
24	SDRAM access from clock. CAS latency = 2	6ns	8ns	8ns	60	14	18
27	Min. row precharge time	20ns	24ns	30ns	14	14	14
28	Min. row active to row active	16ns	20ns	24ns	10	2E	32
29	Min. RAS to CAS delay	20ns	20ns	20ns	14	08	08
30	Min. RAS pulse width	46ns	46ns	50ns	2E	12	12
31	Module bank density	32MB			08		
62	SPD data revision code	Rev.1, 2			12		
63	Checksum for bytes 0-62	Checksum data			7C	9E	DC
64	Manufacturer ' s JEDEC ID code	Continuation code			7F		
65	Manufacturer ' s JEDEC ID code	Vanguard			29		
66-71	Manufacturer ' s JEDEC ID code	None			FF		

Byte	Function described	Function Supported			HEX		
		-8H	-8L	10	-8H	-8L	10
72	Manufacturering location	-			-		
73	Manufacture's part number	V			56		
74	Manufacture's part number	P			50		
75	Manufacture's part number	4			34		
76	Manufacture's part number	6			36		
77	Manufacture's part number	4			34		
78	Manufacture's part number	6			36		
79	Manufacture's part number	4			34		
80	Manufacture's part number	1			31		
81	Manufacture's part number	6			36		
82	Manufacture's part number	4			34		
83	Manufacture's part number	1			31		
84	Manufacture's part number	B			42		
85	Manufacture's part number	T			54		
86	Manufacture's part number	G(Gold lead) S(Tin lead)			47 53		
87	Manufacture's part number	A			41		
88	Manufacture's part number	"-"			2D		
89	Manufacture's part number	8	8	10	38	38	40
90	Manufacture's part number	H	L	Blank	48	4C	20
91	Revision code for PCB	A			41		
92	Revision code	Blank			20		
93~94	Manufacturing data	Year/Week code			-		
95~98	Module serial number	Serial number			-		
99~125	Manufacturer specific data	-			-		
126	Module supports clock frequency	100Mhz			64		
127	Intel specification details	Detail 100MHz information			AF	AD	AD
128~255	For customer usc	None			FF		

Serial presence detect information

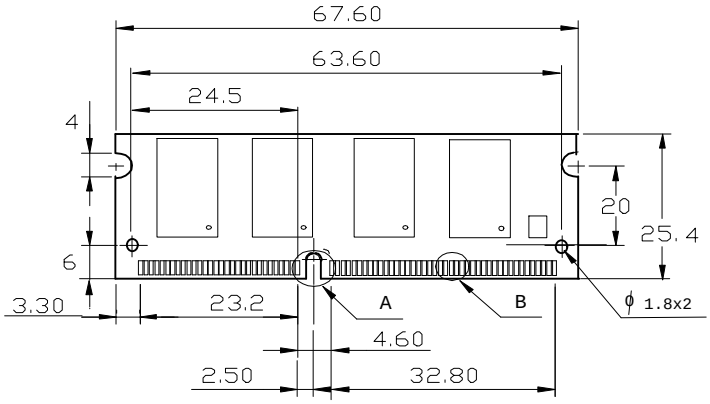
64 MB

Byte	Function described	Function Supported			HEX		
		-8H	-8L	10	-8H	-8L	10
0	Number of bytes used by Vanguard	128 bytes			80		
1	Total SPD memory size	256 bytes			08		
2	Memory Type	SDRAM			04		
3	Number of Row addresses	12			0C		
4	Number of Column addresses	8			08		
5	Number of Banks on module	2 row			02		
6	Module data width	64 bits			40		
7	Module data width (continued)	0			00		
8	Module voltage interface levels	LVTTL			01		
9	SDRAM cycle time. CAS latency = 3	8ns	8ns	10ns	80	80	A0
10	SDRAM access from clock. CAS latency = 3	6ns	6ns	7ns	60	60	70
11	Module configuration type	Non-Parity			00		
12	Refresh Rate/Type	15.6us/self			80		
13	SDRAM width, Primary SDRAM	x16			10		
14	Error checking SDRAM data width	N/A			00		
15	Min. clock delay, Back to back random column address	1			01		
16	Burst length supported	1,2,4,8,Page			8F		
17	Number of banks on each SDRAM device	4			04		
18	CAS latencies supported	2 & 3			06		
19	CS latency	0 CLK			01		
20	Write latency	0 CLK			01		
21	SDRAM module attributes	Non-buffered			00		
22	SDRAM device attributes : general	0E			0E		
23	SDRAM cycle time. CAS latency = 2	10ns	12ns	15ns	A0	18	1E
24	SDRAM access from clock. CAS latency = 2	6ns	8ns	8ns	60	14	18
27	Min. row precharge time	20ns	24ns	30ns	14	14	14
28	Min. row active to row active	16ns	20ns	24ns	10	2E	32
29	Min. RAS to CAS delay	20ns	20ns	20ns	14	08	08
30	Min. RAS pulse width	46ns	46ns	50ns	2E	12	12
31	Module bank density	32MB			08		
62	SPD data revision code	Rev.1, 2			12		
63	Checksum for bytes 0-62	Checksum data			7D	9F	DD
64	Manufacturer ’s JEDEC ID code	Continuation code			7F		
65	Manufacturer ’ s JEDEC ID code	Vanguard			29		
66-71	Manufacturer ’ s JEDEC ID code	None			FF		

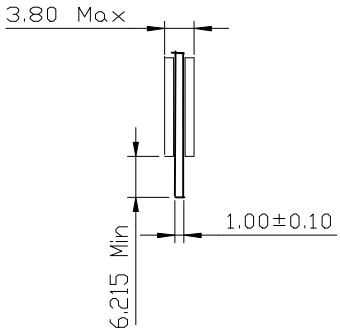
Byte	Function described	Function Supported			HEX		
		-8H	-8L	10	-8H	-8L	10
72	Manufacturering location	-			-		
73	Manufacture's part number	V			56		
74	Manufacture's part number	P			50		
75	Manufacture's part number	8			38		
76	Manufacture's part number	6			36		
77	Manufacture's part number	4			34		
78	Manufacture's part number	6			36		
79	Manufacture's part number	4			34		
80	Manufacture's part number	1			31		
81	Manufacture's part number	6			36		
82	Manufacture's part number	4			34		
83	Manufacture's part number	1			31		
84	Manufacture's part number	B			42		
85	Manufacture's part number	T			54		
86	Manufacture's part number	G(Gold lead) S(Tin lead)			47 53		
87	Manufacture's part number	A			41		
88	Manufacture's part number	"-"			2D		
89	Manufacture's part number	8	8	10	38	38	40
90	Manufacture's part number	H	L	Blank	48	4C	20
91	Revision code for PCB	A			41		
92	Revision code	Blank			20		
93~94	Manufacturing data	Year/Week code			-		
95~98	Module serial number	Serial number			-		
99~125	Manufacturer specific data	-			-		
126	Module supports clock frequency	100Mhz			64		
127	Intel specification details	Detail 100MHz information			FF	FD	FD
128~255	For customer usc	None			FF		

144 Pin SODIMM Mechanical Dimension(Front Side)

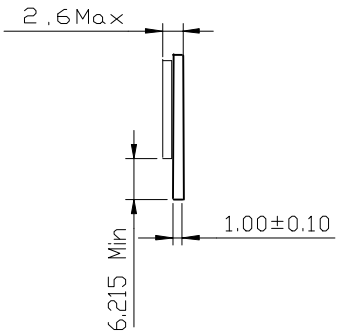
Front



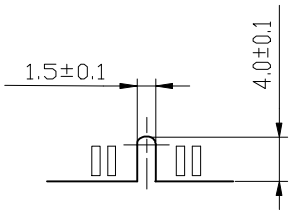
8Mx64 Side



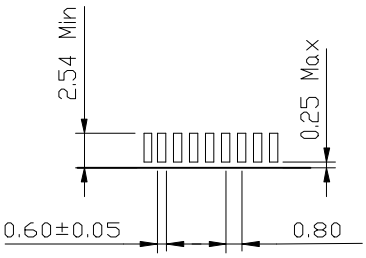
4Mx64 Side



Detail A



Detail B



NOTE : The use device is TSOP SDRAM

All dimensions are typical unless otherwise stated. (MILLIMETERS)

Ordering Information

	1	2	3	4	5	6	7	8	9	10
V	X	XX	XX	XXXXXX	X	X	X	X	X	-X

V : VIS Product
1 : RAM Family
P: SDRAM SODIMM(144pin)

2 : Memory density (work)
4 : 4M
8 : 8M

3 : I/O width
64 : X 64

4 : Operation mode and refresh with different density
641641 : 4K ref., 4M X16 SDRAM

5 : Component revision
Blank : None
A : A revision
B : B revision
C : C revision

6 : Component Package
T : TSOP

7 : PC board finger plating
G : Gold
S : Tin/lead

8 : PC board revision
Blank : none
A : A revision
B : B revision
C : C revision

9 : Customer specific
Blank : none

10 : Module speed
-8H : 100Mhz, CL = 2, t_{RP} = 2, t_{RCD} = 2
-8L : 100Mhz, CL = 3, t_{RP} = 2, t_{RCD} = 2
-10 : 100Mhz, CL = 3, t_{RP} = 3, t_{RCD} = 3