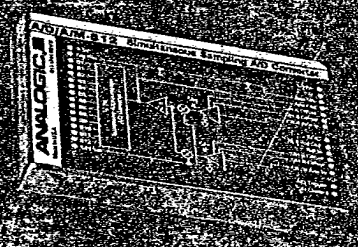

ANALOGIC®

A/D/A/M-812

DUAL CHANNEL SIMULTANEOUSLY SAMPLING 51 kHz 12-BIT A/D CONVERTER

INTRODUCTION

The A/D/A/M-812 is a two-channel data acquisition system consisting of two simultaneously operating Sample-and-Hold Amplifiers (S/H) and a 12-bit Analog-to-Digital Converter (ADC). The dual S/H's allow near simultaneous (within 5 ns) sampling of time- or phase-related signals, thereby reducing the complexity of expensive hardware and/or software time-skew correction in systems such as quadrature demodulated signal processing front-ends, component transfer function testers, and colorimeters.

In systems using time-shared S/H's or dedicated S/H's controlled with insufficient simultaneity, the information contained within the time or phase interrelationship can be lost. Sequential sampling of these signals may require costly correcting of errors induced by the sampling process; these correction methods are of use only if the delay between the samples is known precisely. By sampling the input pair within 5 ns of one another, the A/D/A/M-812 significantly reduces these sources of error.

The A/D/A/M-812 provides a two-channel throughput rate of 51 kHz (single channel throughput of 91 kHz). A/D/A/M-812 specifications are based on an end-to-end error budget that accounts for all internal error sources, including S/H droop at a 51 kHz sampling rate, errors due to aperture uncertainty for bandlimited signals up to 25 kHz, S/H pedestal non-linearities, and A/D non-linearities. The design of the A/D/A/M-812 takes maximum advantage of the temperature and time stability of discrete components, and offers an end-to-end accuracy of ±1 LSB maximum; this is in direct contrast to monolithic S/H's which commonly exhibit more than 1 LSB equivalent error at the 12-bit level by themselves.

The fully integrated A/D/A/M-812 is tested as a subsystem by ANALOGIC, which frees the system designer from performing a myriad of time-consuming design and testing tasks, and minimizes system production and test efforts. A fully tested and shielded subsystem, the A/D/A/M-812 offers superior performance, ease of use and integration, at a lower cost than the parts alone for a custom design.

FEATURES

- **Guaranteed Overall Transfer Accuracy**
  ±0.025% FSR, maximum
- **High Throughput Rate**
  51,000 two-channel samples per second
  91,000 single-channel samples per second
- **Low Aperture Uncertainty Time**
  5 ns—minimizes phase error between simultaneously sampled channels
- **Universal Data Systems Compatibility**
  Standard TTL digital inputs/outputs
- **Low Noise**
  165 μV rms
- **Separate Reference Input and Output**
  Allows ratiometric operation
- **Small Size**
  2" x 3" x 0.375"
- **RFI and EMI Shielded**

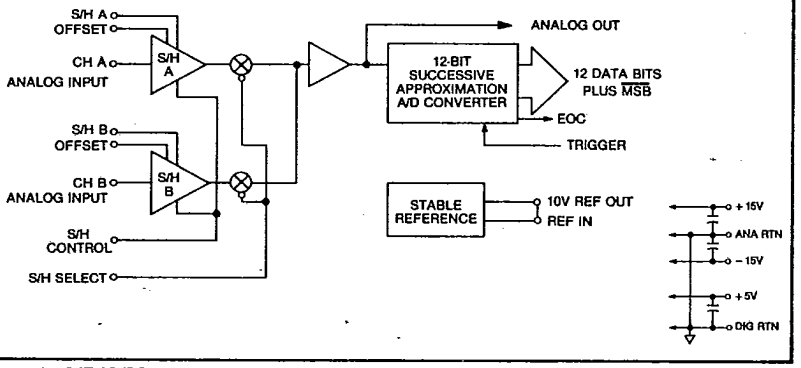

Figure 1. A/D/A/M-812 Functional Block Diagram

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A/D/A/M-812 SPECIFICATIONS

(All Specifications guaranteed at 25°C unless otherwise noted.)

ANALOG INPUTS

Number of Channels:	2
Configuration:	Voltage Follower Input
Full Scale Range (FSR):	0 to +10V, ±5V, or ±10V; Factory configured
Maximum Input Without Damage:	±15V
Input Impedance:	>100 Megohms
Input Bias Current[1]:	<1 nA (at 25°C)

ACCURACY (at 51 kHz Sampling Rate, at 25°C, nominal)

Relative Accuracy[2]:	±0.025% FSR, maximum
Differential Non-linearity:	±1/2 LSB, maximum
Noise:	165 μV rms maximum for 10V FSR; 320 μV rms maximum for 20V FSR; referred to input; measured over dc to 1 MHz bandwidth
Monotonicity:	Guaranteed; No missing codes
S/H Hold Mode Feedthrough Rejection Ratio[3]:	−82 dB minimim; measured with 1 kHz squarewave, full scale
Channel-to-Channel Crosstalk[4]:	−110 dB at 10 kHz
Total Offset Error (Untrimmed, Including pedestal Error)[5]:	25 mV maximum; adjustable to zero
Gain Error[5,6]:	±0.025% FSR, maximum
Gain Accuracy Between Channels:	±7.5 mV, maximum

DYNAMIC PERFORMANCE

Maximum Dual Channel Sampling Rate[7]:	2 samples/19.5 μs (51 kHz)
Maximum Single Channel Sampling Rate[7]:	1 sample/11.0 μs (91 kHz)
S/H Acquisition Time to 1/2 LSB:	4.5 μs maximum
S/H Droop Rate (at 25°C)[1]:	0.02 μV/μs, typical, 0.2μV/μs, maximum
S/H Multiplexer Settling Time to ±1/2 LSB:	Refer to Timing Diagram
S/H Aperture Delay Time:	50 ns typical
S/H Aperture Uncertainty Time:	5 ns typical

STABILITY

Differential Non-linearity Temperature Coefficient:	±3 ppm/°C FSR maximum
Offset Temperature Coefficient Unipolar:	±10 ppm/°C FSR Maximum
Bipolar:	±15 ppm/°C FSR maximum
Gain Temperature Coefficient:	±20 ppm/°C FSR maximum
Power Supply Sensitivity:	0.003% FSR per percent change in Supply Voltage
Warm-up Time to Specified Accuracy:	5 Minutes

DIGITAL INPUT/OUTPUT

General:	Inputs: 1 TTL LS Load, each; Outputs: 2 TTL Load Fanout, each TTL positive true is Logic "1" Logic "0" = 0.4V maximum for output; 0.8V maximum for input Logic "1" = 2.4V minimum for output; 2.0V minimum for input
S/H Select:	Logic "0" selects S/H A, logic "1" selects S/H B
S/H Mode Control:	Logic "0" selects HOLD mode, logic "1" selects SAMPLE mode for both channels
A/D Trigger:	Positive pulse, trailing edge triggered; 100 ns minimum pulse width
Data:	12 data bits plus $\overline{\text{MSB}}$; binary, offset binary, or two's complement coding
EOC:	Logic "1" during conversion; "1" to "0" transition indicates data available

POWER REQUIREMENT[8]

+15V, ±3%	60mA maximum
−15V, +3%	70mA maximum
+5V, ±3%	65mA maximum

ENVIRONMENTAL AND MECHANICAL

Operating Temperature:	0°C to +70°C
Storage Temperature:	−25°C to +85°C
Relative Humidity:	Up to 95%, non-condensing
Dimensions:	2.00" x 3.00" x 0.375" (50.8 x 76.2 x 9.53 mm)
Shielding:	Electromagnetic 5 sides Electrostatic 6 sides

NOTES:

1. Doubles every 10°C
2. Includes effects of input switching, buffer amplifier, S/H amplifier and ADC
3. Measured on S/H output, in HOLD mode with input signal as stated
4. Measured on Channel A S/H output with input grounded. Input signal applied to Channel B input. Both channels in SAMPLE mode
5. Offset and gain errors are externally adjustable to zero
6. With 50 ohm, 1% fixed resistor installed in series with Reference input
7. On ±10V FSR
8. Digital ground, analog ground and case are tied internally

TYPICAL TIMING

Figure 2 depicts a typical timing relationship among the various control signals required by the A/D/A/M-812. Channel A and B are simultaneously sampled, then sequentially converted to digital data.

The S/H amplifiers require 4.5 μs to simultaneously acquire the signals on both input channels (to within 1/2 LSB for a worst case full-scale input step). Once the signal pair is acquired, the S/H Control can be switched into the HOLD mode. If the application warrants, the S/H Control input can also be used as the A/D Trigger input.

The diagram indicates that the output data from the A/D converter is valid after a 10 ns delay from the logic "1" to "0" transition of EOC. The output data can be read at this time or at any time up to the next A/D trigger, since the last bit (LSB) decision is made, and the result settled prior to the EOC transition. The S/H Control can be switched to SAMPLE while the second data word is being read, with no effect on the data.

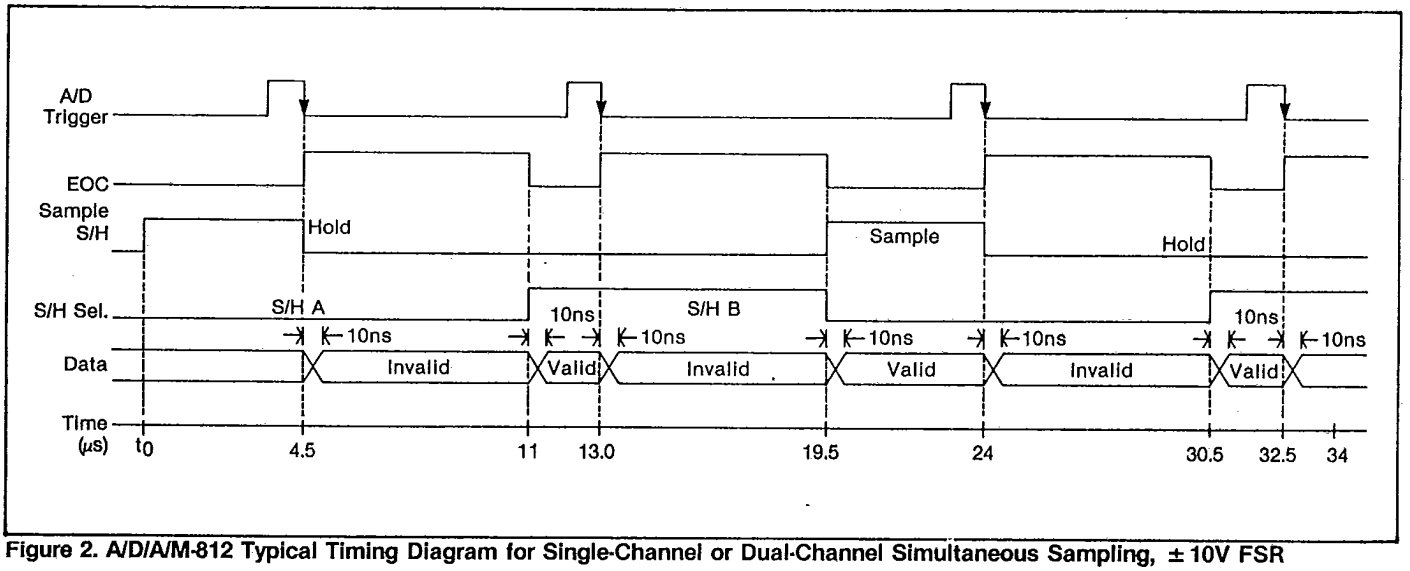


Figure 2. A/D/A/M-812 Typical Timing Diagram for Single-Channel or Dual-Channel Simultaneous Sampling, ±10V FSR

OUTPUT CODING

Unipolar Binary

Input	B1,	B2,	B3,	B4,	B5,	B6,	B7,	B8,	B9,	B10,	B11,	B12
+9.9976V	1	1	1	1	1	1	1	1	1	1	1	1
0.0000V	0	0	0	0	0	0	0	0	0	0	0	0

Offset Binary*

Input	B1,	B2,	B3,	B4,	B5,	B6,	B7,	B8,	B9,	B10,	B11,	B12
+9.9951V	1	1	1	1	1	1	1	1	1	1	1	1
0.0000V	1	0	0	0	0	0	0	0	0	0	0	0
−10.0000V	0	0	0	0	0	0	0	0	0	0	0	0

Two's Complement*

Input	B1,	B2,	B3,	B4,	B5,	B6,	B7,	B8,	B9,	B10,	B11,	B12
+9.9951V	0	1	1	1	1	1	1	1	1	1	1	1
0.0000V	0	0	0	0	0	0	0	0	0	0	0	0
−10.0000V	1	0	0	0	0	0	0	0	0	0	0	0

*For ±5V Full Scale Range, divide voltages by 2

CALIBRATION

OFFSET

A separate, external 20 kohm multi-turn potentiometer for each S/H amplifier is recommended, per Figure 3. The +15V source used to power the A/D/A/M-812 should be used for the offset circuit as well.

With S/H A selected and the S/H Control line at logic "1" (SAMPLE), suply the input indicated in the Calibration Voltages table to input A. Adjust the S/H A offset pot until the LSB of the output data word varies equally between 0 and 1. Repeat the above procedure for S/H B.

GAIN

If gain trimming is required by the application, a 100 ohm, multi-turn potentiometer connected between the 10V REF OUT and REF IN pins per Figure 3 will provide an approximate ±0.25% FSR adjustment in gain. For many applications, a fixed 50 ohm, 1% resistor may be used in place of the trimpot.

Gain will rarely require recalibration in most applications. If gain is to be adjusted, follow the procedure below, after performing the offset procedure for both S/H's.

Select either the A or B S/H, and supply a logic "1" to the S/H Control line (SAMPLE). Supply the input indicated in the Calibration Voltages table to the selected input. Adjust the optional 100 ohm trimpot until the LSB of the data word varies equally between 0 and 1.

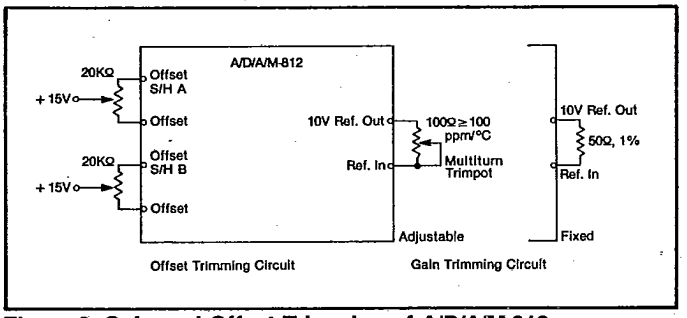
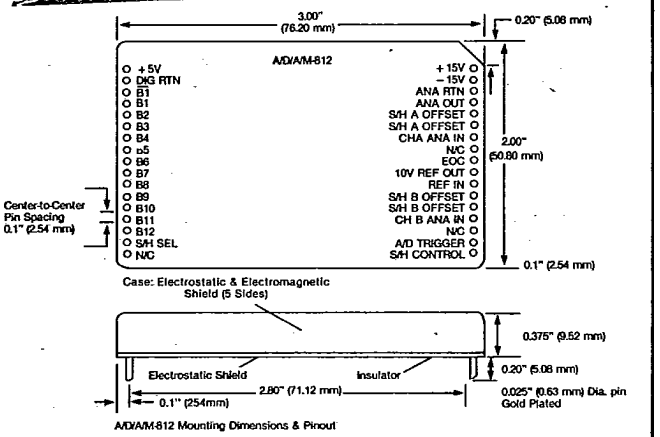


Figure 3. Gain and Offset Trimming of A/D/A/M-812

Calibration Voltages

Adjustment Procedure	Input Full Scale Range		
	0 to +10V	±10V	±5V
Offset	+0.0012V	+0.0024V	+0.0012V
Gain	+9.9976V	+9.9951V	+4.9975

MOUNTING DIMENSIONS & PINOUTS



A/D/A/M-812 Mounting Dimensions & Pinout

ORDERING GUIDE

For an input voltage range of:	Specify:
0V to +10V FSR	☐ A/D/A/M-812-1
±10V FSR	☐ A/D/A/M-812-2
±5V FSR	☐ A/D/A/M-812-3

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