HD63085

Document Image Compression and Expansion Processor (DICEP)

The DICEP is an LSI that performs compression (encoding) and expansion (decoding) of the digital (two-value) data representing a document image.
The DICEP is used in G3 and G4 facsimile apparatus, intelligent copiers, word processors, telex, terminals, laser beam printers, file servers and other office automation systems.
The DICEP uses Modified Huffman (MH) coding scheme, Modified READ (MR) coding scheme and Modified MR (M^2R) coding scheme which are compatible with the CCITT (Comité Consultatif International Télégraphique et Téléphonique) recommendations for Group 3 and Group 4 facsimile apparatus.

Features

- Compatible with the CCITT Recommendations for Group 3 and Group 4 facsimile apparatus
- Simple MPU Command
  As the DICEP stores coding and decoding algorithms in the microprogram ROM as firmware, a single MPU command allows this LSI to encode (i.e. compress) or decode (i.e. expand) a scan line of digital data.
- High Speed Coding and Decoding
  The DICEP realizes high speed coding and decoding by:
  - including a changing pels* detector which can detect a changing pel contained in a word (8 bits/16 bits) of document image data within an instruction cycle time (at least 125nsec), and
  - including a decoded pels generator which can generate a word (8 bits/16 bits) of document image data within an instruction cycle time.

  *: The term 'picture element' is abbreviated to 'pel' in this document.
- Flexible System Configuration
  - Either 68 type MPU or 80 type MPU can be interfaced.
    The system bus has the size of 8 bits.
  - The DICEP has two bus interfaces; the system bus interface and the document image bus interface.
  - The DICEP may be interfaced with two independent buses (i.e. the system bus and the document image bus), while it may be interfaced with a common bus.
  - The size of the document image bus is selectable (8 bits/16 bits) depending on the word size of document image memory.
- High Speed DMA Transfer
  - The DICEP can perform direct memory access (DMA) transfer between an I/O device (scanner or printer) and the document image memory. The maximum transfer rate is 4M byte/sec.
  - With a DMA controller (DMAC) on the system bus, DMA transfers can be performed between a memory on the system bus and the DICEP.
- A Variety of Programmable Parameters
  Internal programmable registers present the DICEP flexibility to allow application to many kinds of systems.
  - The parameters can be changed before initiation of every command.
  - The length of a scan line is programmable from the word size of the document image memory (8 bits/16 bits) to 64K bits.
  - One of coding operation, decoding operation and transfer operation can be selected.
  - One of MH coding scheme, MR coding scheme, M^2R coding scheme and run length coding scheme can be selected.
  - The minimum length of a coded scan line is programmable from 0 to $2^{16}-1$ bits.
  - The number of End of Line (EOL) code words is programmable from 0 to $2^{16}-1$.
  - The number of Return to Control (RTC) code words is programmable from 0 to $2^{16}-1$.
  - The DICEP can code and decode a desired part of a document on a word (8 bits/16 bits) basis.
- Data Transfer between Buses
  The DICEP can perform data transfer between the system bus and the document image bus without coding or decoding.
- Octet Mode
  The DICEP provides Octet Mode. In this mode, a coded scan line or a coded page is 8-bit boundary conditioned.
- Run Length Coding Scheme
  The DICEP provides run length coding scheme in addition to MH coding, MR

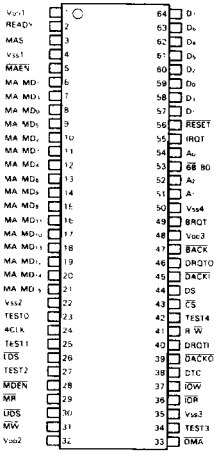
coding and M²R coding.
- High Operating Speed
  - −Instruction cycle time is 125 nsec min. (at system clock of 8 MHz max.)
  - −Input clock frequency is 32 MHz max.
- Package
  - −64 pin plastic shrink DIP (DP-64S)
  - −72 pin ceramic PGA (PC-72)

Ordering Information

Type No.	Input Clock	Package
HD63085P	2MHz to 32MHz	64 pin plastic shrink DIP (DP-64S)
HD63085YR		72 pin ceramic PGA (PC-72)

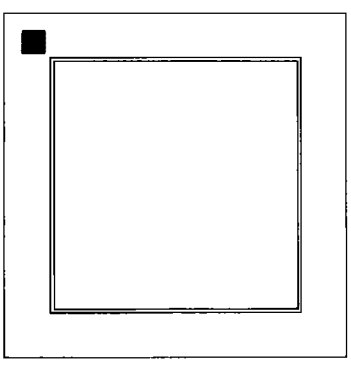
Pin Arrangement

●DP-64S

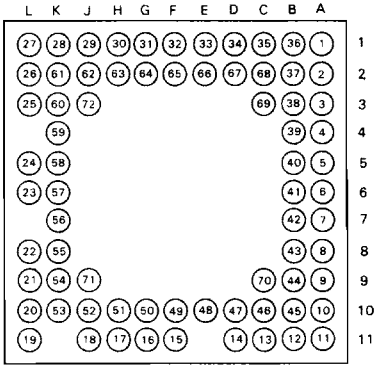


(Top View)

●PC-72



(Top View)



(Bottom View)

Pin Code	Pin No.	Mnemonic	Pin Code	Pin No.	Mnemonic	Pin Code	Pin No.	Mnemonic
A1	1	MA/MD_0	C3	69	NC	J2	62	D_1
A2	2	MA/MD_2	C9	70	NC	J3	72	NC
A3	3	MA/MD_4	C10	46	$\overline{LDS}$	J9	71	NC
A4	4	MA/MD_6	C11	13	$\overline{UDS}$	J10	52	$\overline{DACKO}$
A5	5	MA/MD_8	D1	34	READY	J11	18	DTC
A6	6	MA/MD_{10}	D2	67	NC	K1	28	V_{DD}
A7	7	MA/MD_{12}	D10	47	$\overline{MDEN}$	K2	61	V_{DD}
A8	8	MA/MD_{14}	D11	14	$\overline{MW}$	K3	60	IRQT
A9	9	V_{SS}	E1	33	V_{DD}	K4	59	A_0
A10	10	$TEST_0$	E2	66	V_{DD}	K5	58	A_2
A11	11	4CLK	E10	48	$\overline{MR}$	K6	57	BRQT
B1	36	MA/MD_1	F1	32	D_6	K7	56	DRQTO
B2	37	MA/MD_3	F2	65	D_7	K8	55	$\overline{CS}$
B3	38	MA/MD_5	F10	49	$\overline{DMA}$	K9	54	NC
B4	39	MA/MD_7	F11	15	SET	K10	53	DRQTI
B5	40	MA/MD_9	G1	31	D_4	L1	27	$\overline{RESET}$
B6	41	MA/MD_{11}	G2	64	D_5	L2	26	NC
B7	42	MA/MD_{13}	G10	50	V_{SS}	L3	25	$\overline{68/80}$
B8	43	MA/MD_{15}	G11	16	V_{SS}	L5	24	A_1
B9	44	V_{SS}	H1	30	D_2	L6	23	$\overline{BACK}$
B10	45	$TEST_1$	H2	63	D_3	L8	22	DACKI
B11	12	TDATA	H10	51	$\overline{IOW}$	L9	21	DS
C1	35	MAS	H11	17	$\overline{IOR}$	L10	20	AGE
C2	68	$\overline{MAEN}$	J1	29	D_0	L11	19	R/$\overline{W}$

Pin Descriptions (1 of 4)

<System Bus Interface Pins>

Signal	Pin No. PC-72	Pin No. DP-64S	I/O	Descriptions
$\overline{68}$/80	25	53	I	68/80 Mode select If $\overline{68}$/80 is low, it indicates that a 68 type MPU is interfaced with the DICEP. If high, it indicates that an 80 type MPU is interfaced.
A0 A1 A2	59 24 58	54 51 52	I	Addresses 0 to 2. These pins are connected to the 3 low-order bits of the system address bus to address the DICEP internal registers.
D0 D1 D2 D3 D4 D5 D6 D7	29 62 30 63 31 64 32 65	59 57 60 58 62 61 63 64	I/O, 3-state output	Data 0 to 7. These pins are interfaced with the system data bus to provide bidirectional communication between the MPU and the DICEP. The MPU can read/write the DICEP internal registers via D0 to D7 pins.
$\overline{CS}$	55	43	I	Chip select. A low level on this pin indicates that the MPU accesses a DICEP internal register.
DS	21	44	I	Data strobe. This pin must be connected to ϕ 2 clock pin of 68 type MPU or $\overline{RD}$ pin of 80 type MPU.
R/$\overline{W}$	19	41	I	Read/Write. This pin is connected to R/$\overline{W}$ pin of 68 type MPU or $\overline{WR}$ pin of 80 type MPU.
$\overline{RESET}$	27	56	I	A low level on$\overline{RESET}$ initializes the DICEP.
4CLK	11	24	I	4 Clock. The clock frequency is four times as high as the DICEP system clock frequency.
IRQT	60	55	O	Interrupt Request. The DICEP sends an interrupt request to the MPU by diving IRQT high upon completion of a command, end of a DMA transfer, occurrence of decoding error or reception of Return to Control (RTC) code words. MPU can know the cause of an interrupt by reading the Interrupt Request Register (IRR). When the MPU reads the IRR, IRQT returns to the low state.
DRQT0	56	46	O	DMA Request Output. The DICEP can drive DRQTO high to provide DMA request to the DMA Controller (DMAC) when: (1) coded data of more than 1 byte are stored in the FIFO during coding operation, (2) the FIFO has empty space of more than 1 byte during decoding operation or (3) Data Buffer Register (DBR) is ready for a read or write operation during data transfer between the system bus and the document image bus.
$\overline{DACKI}$	22	45	I	DMA Acknowlege Input. This input is a response to DRQTO. When $\overline{DACKI}$ goes low during coding operation or decoding operation, the FIFO is accessed. If $\overline{DACKI}$ goes low during data transfer between the system bus and the document image bus, the DBR is accessed. $\overline{CS}$ and $\overline{DACKI}$ must not be pulled low together.

3

DICEP Pin Descriptions (2 of 4)
〈Document Image Bus Interface Pins〉

Signal	Pin No. PC-72	Pin No. DP-64S	I/O	Descriptions
BRQT	57	49	O	Bus Request. When BRQT is driven high by DICEP, it indicates to all other potential bus master devies on the document image bus that the DICEP desires to become the bus master. When the document image bus has no other potential master device, BRQT does not have to be connected to any line.
$\overline{\text{BACK}}$	23	47	I	Bus Acknowledge. This input is a response to the BRQT. A low level on $\overline{\text{BACK}}$ indicates that the DICEP is granted to be the master of the document image bus. This pin must be fixed low when the document image bus has no potential bus master devices other than the DICEP.
$\overline{\text{MAEN}}$	68	5	O	Memory Address Enable. When $\overline{\text{MAEN}}$ is driven low by DICEP, it indicates that the DICEP has become the master of the document image bus. If $\overline{\text{MAEN}}$ is high, all of three-state outputs interfaced with the document image bus are in high impedance state.
MAS	35	3	O	Memory address Strobe. When the DICEP drives MAS high, it indicates that the DICEP outputs an address onto MA/MD0 through MA/MD15.
$\overline{\text{UDS}}$	13	30	3-state output	When $\overline{\text{UDS}}$ is driven low by DICEP, it indicates that the DICEP uses the high-order byte of the document image bus.
$\overline{\text{LDS}}$	46	26	3-state output	When $\overline{\text{LDS}}$ is driven low by DICEP, it indicates that the DICEP uses the low-order byte of the document image bus.
$\overline{\text{MDEN}}$	47	28	O	Memory Data Bus Enable. When $\overline{\text{MDEN}}$ is driven low by DICEP, it indicates that there is a valid data on MA/MD0 through MA/MD15. This output is used to control the output of bidirectional bus buffer on the MA/MD0 through MA/MD15.
MA/MD0	1	8	I/O, 3-state output	Memory Address Data Bus. This is multiplexed address/data bus for document image bus operation. MA/MD0 to MA/MD15 are used as follows: 1) Output address lines when the $\overline{\text{MAEN}}$ is low and the MAS is high. 2) Input data lines when both $\overline{\text{MAEN}}$ and $\overline{\text{MDEN}}$ are low during read cycle. 3) Output data lines when both $\overline{\text{MAEN}}$ and $\overline{\text{MDEN}}$ are low during write cycle.
MA/MD1	36	6		
MA/MD2	2	10		
MA/MD3	37	7		
MA/MD4	3	12		
MA/MD5	38	9		
MA/MD6	4	13		
MA/MD7	39	11		
MA/MD8	5	15		
MA/MD9	40	14		
MA/MD10	6	17		
MA/MD11	41	16		
MA/MD12	7	19		
MA/MD13	42	18		
MA/MD14	8	20		
MA/MD15	43	21		

DICEP Pin Descriptions (3 of 4)
< Document Image Bus Interface Pins > (continued)

Signal	Pin No. PC-72	Pin No. DP-64S	I/O	Descriptions
$\overline{MR}$	48	29	3-state output	Memory Read. The DICEP drives $\overline{MR}$ low to read data from the document image memory.
$\overline{MW}$	14	31	3-state output	Memory Write. The DICEP drives $\overline{MW}$ low to write data into the document image memory.
$\overline{IOR}$	17	36	3-state output	I/O Read. The DICEP drives $\overline{IOR}$ low to read data from an I/O device on the document image bus. However, $\overline{IOR}$ is used only for data transfer between buses or for DMA transfer through the document image bus during coding operation.
$\overline{IOW}$	51	37	3-state output	I/O Write. The DICEP drives $\overline{IOW}$ low to write data into an I/O device on the document image bus. However, $\overline{IOW}$ is used only for data transfer between buses or for DMA transfer through the document image bus during decoding operation.
DRQTI	53	40	I	DMA Request Input. DRQTI is driven high when an I/O device on the document image bus sends a DMA request to the DICEP.
$\overline{DACKO}$	52	39	O	DMA Acknowledge Output. When this output is driven low, it notifies the peripherals on the document image bus that they have been granted a DMA operation.
$\overline{DMA}$	49	33	O	Direct Memory Access. When $\overline{DMA}$ is driven low, it indicates that the DICEP is executing a DMA transfer. During coding operation, data is transferred from the I/O device (scanner) to the document image memory. During decoding operation, data is transferred from the document image memory to the I/O device (printer).
DTC	18	38	O	DMA Terminal Count. When DTC is driven high, it indicates that DMA transfer of a scan line has been completed.
READY	34	2	I	When READY is high during a read or write to the document image memory or the I/O devices, it indicates that the memory or I/O device is ready to send or receive data. If READY is low, the DICEP will wait until READY becomes high.

DICEP Pin Descriptions (4 of 4)
<Power Supplies And Other>

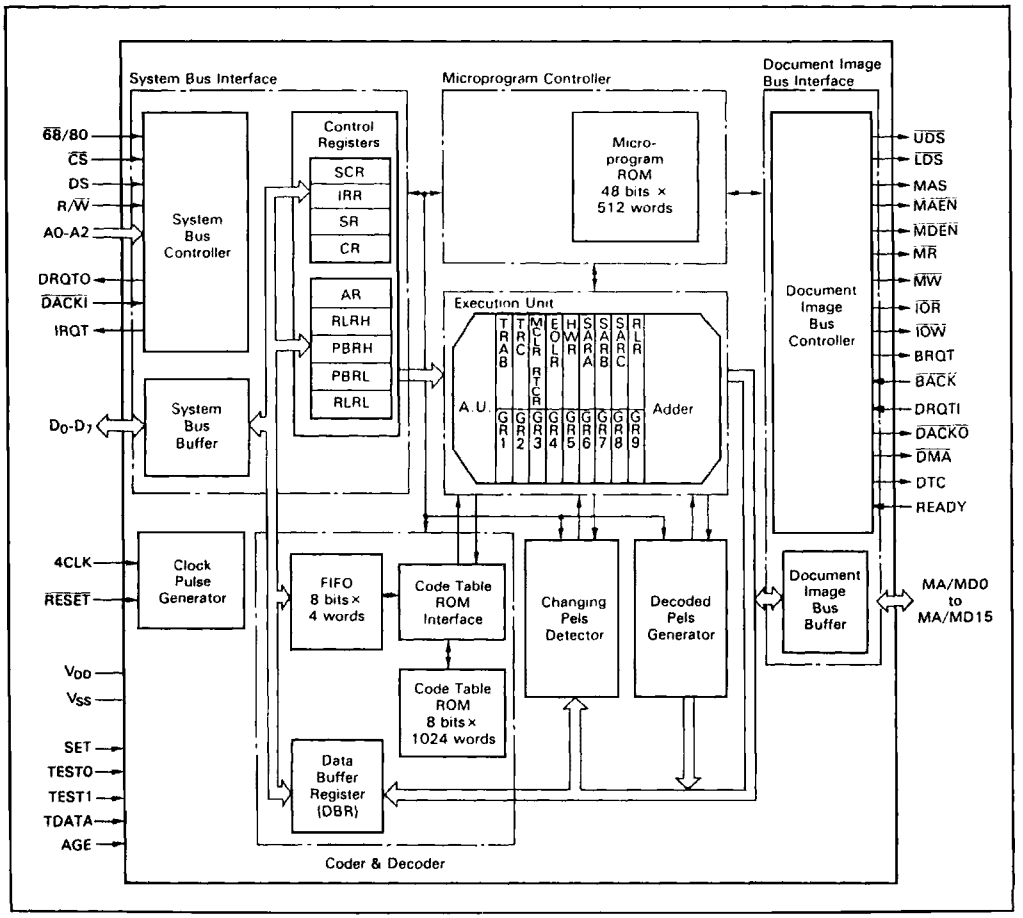
Signal	Pin No. PC-72	Pin No. DP-64S	I/O	Descriptions
V_{DD}	28,33, 61,66	1,32, 48	–	Supply voltage (+5V)
V_{SS}	9,16, 44,50	4,22, 35,50	–	Ground
SET	15	34	I	These pins must be fixed low.
TEST0	10	23		
TEST1	45	25		
TDATA	12	27		
AGE	20	42		

DICEP Functional Summary

Item	Function
Coding Scheme	HM, MR, M²R, Run Length
Maximum Scan-line Length	64k pels
Document Image Bus Memory Address Space size	Document Image Memory ……64k bytes I/O Devices ……64k bytes
Maximum DMA Transfer Rate	4M byte/sec *
Maximum Changing Pels Detect Speed	3.2M byte/sec *
Maximum Decoded Pels Generation Speed	3.2M byte/sec *

* : Input clock frequency is 32 MHz.

Block Diagram



Block Configurations

System Bus Interface

The system bus interface has a timing specification compatible with 8-bit MPUs (HD6800/HD64180). This block includes control registers which can be directly accessed by the MPU.

Microprogram Controller

The microprogram controller stores coding and decoding programs in the microprogram ROM to control all other blocks of the DICEP. This block consists of the microprogram ROM with 512 words of 48 bits, the sequence controller and the pipeline register.

Execution Unit

The execution unit generates document image memory addresses, and calculates the position of changing pels, run lengths, and the relative distance between changing pels on the coding line and those on the reference line.
This block consists of eighteen 16-bit registers, the arithmetic unit (A.U.) and the adder. Nine registers (TRAB, TRC, MCLR/RTCR, EOLR, HWR, SARA, SARB, SARC, and RLR) can be programmed by the MPU via the control registers in the system bus interface. These nine registers are called "parameter registers".

Coder and Decoder

The coder generates the addresses of the code table ROM from input run lengths or relative distances, and generates appropriate code words by looking up the code table ROM.
On the other hand, the decoder generates the addresses of the code table ROM from input code words, and generates run lengths or relative addresses by looking up the code table ROM.

This block consists of the code table ROM with 1024 words of 8 bits, the code table ROM interface, the First-In First-Out memory (FIFO) with 4 words of 8 bits, and the Data Buffer Register (DBR). The code table ROM stores the data which is referenced for coding and decoding operations. The code table ROM interface generates the addresses of the code table ROM. The FIFO temporarily stores code words during coding or decoding operation. The DBR is a intermediate buffer which is used to transfer data between the system bus and the document image bus.

Changing Pels Detector

The changing pels detector detects a changing pel whose color (white or black) is different from that of the previous pel on the same scan line. It can detect a changing pel in a word (8 bits/16 bits) of the document image memory within an instruction cycle time.
This block consists of two changing pels detectors: the reference line detector and the coding line detector. For detailed infomation of the reference line and the coding line.

Decoded Pels Generator

The decoded pels generator can generate at most a word (8 bits/16 bits) of decoded pels within an instruction cycle time, using the information of the positions of changing pels.

Document Image Bus Interface

The document image bus interface provides an interface between the DICEP and the document image bus. It has a 16-bit multiplexed address/data bus.
This block has the following functions:
- it has bus arbitration technique.
- it outputs control signals for the document image bus.

System Configurations

Independent Bus System

Figure 1 shows a system configuration diagram as an example of the independent bus system.
The features of this system are as follows:
- This system includes two independent buses (the system bus and the document image bus)
- The DICEP can perform document image bus operation independently of the MPU, which enhances the system throughput.
- This type of system can also be used in G4 facsimile apparatus.

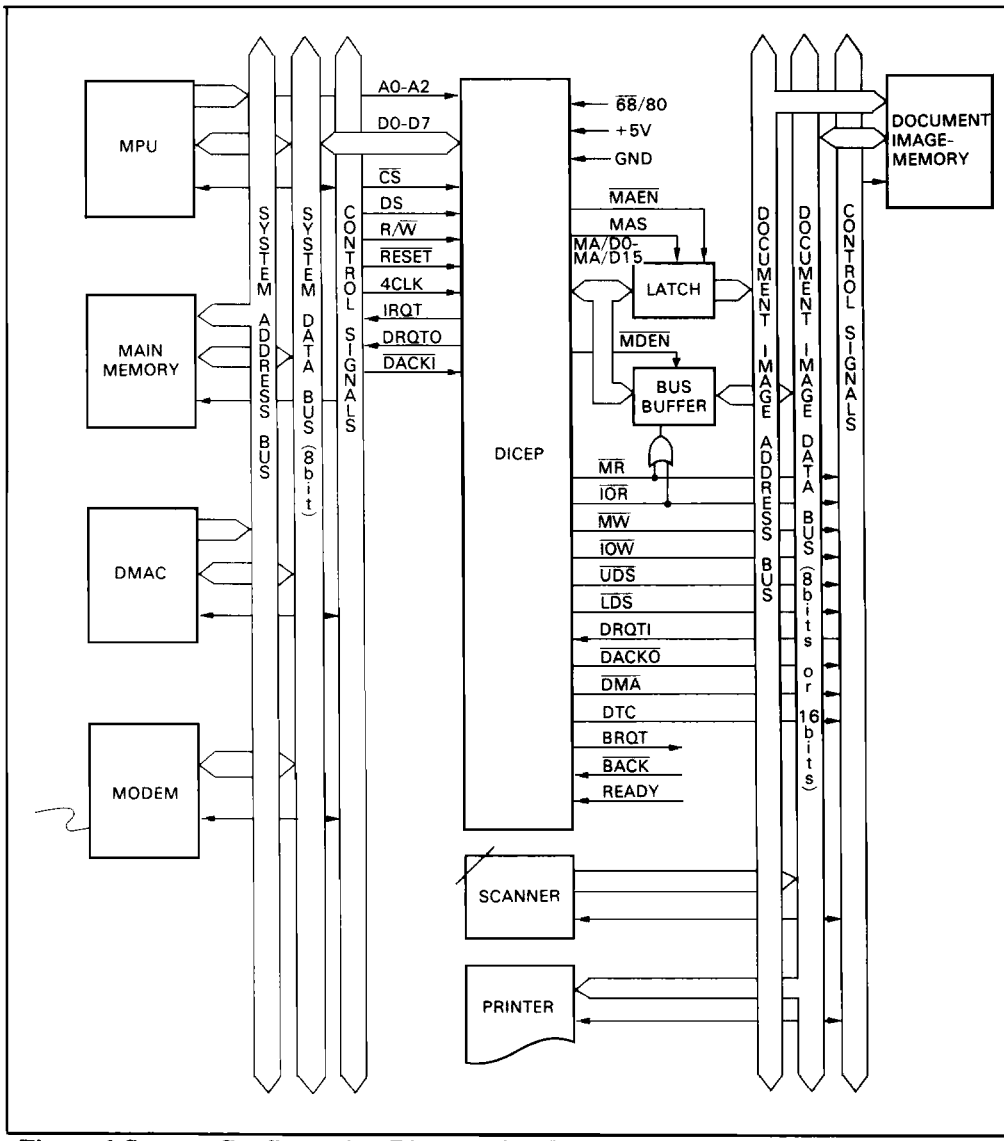


Figure 1 System Configuration Diagram (an Example of Independent Bus System)

Common Bus System

Figure 2 shows a system configuration diagram as an example of the common bus system.

The features of this system are as follows:

- This system includes a common bus which is used as both the system bus and the document image bus.
- The bus arbitration technique realizes this system.
- The MPU can read/write document image data directly.
- This type of system is recommended to be used in G3 facsimile apparatus.

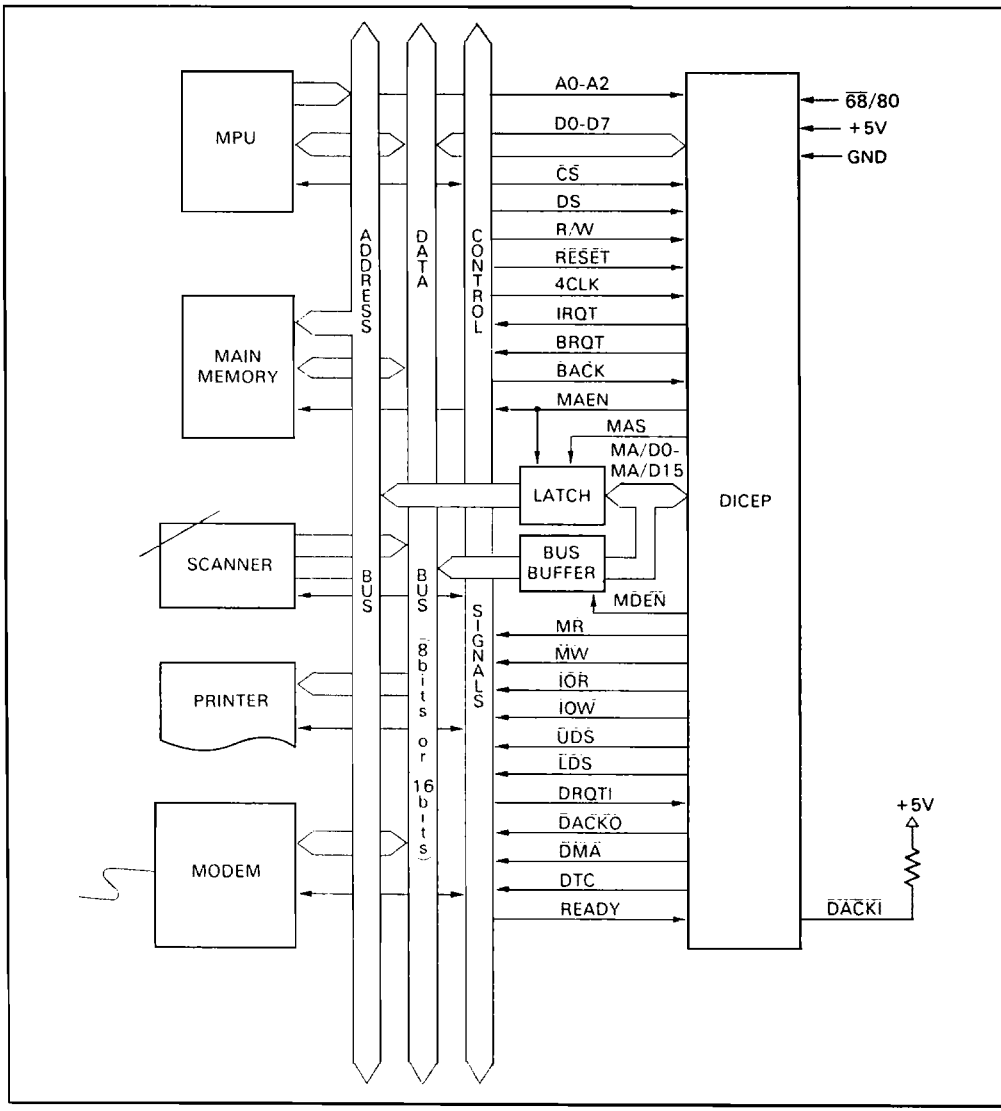


Figure 2 System Configuration Diagram (an Example of the Common Bus System)

Internal Registers

Figure 3 illustrates a DICEP register programming model. DICEP registers can be classified into two groups: registers that are directly accessible by the MPU, and registers that can be accessed via the parameter buffer registers (PBRH, PBRL). The following describes the access methods used for each type of register.

1. Registers directly accessible from the MPU

The control registers (CR), data buffer register (DBR) and FIFO can be accessed directly from the MPU, in accordance with A_0 to A_2, when $\overline{CS}$ is low level.

Table 1 shows the directly accessible registers.

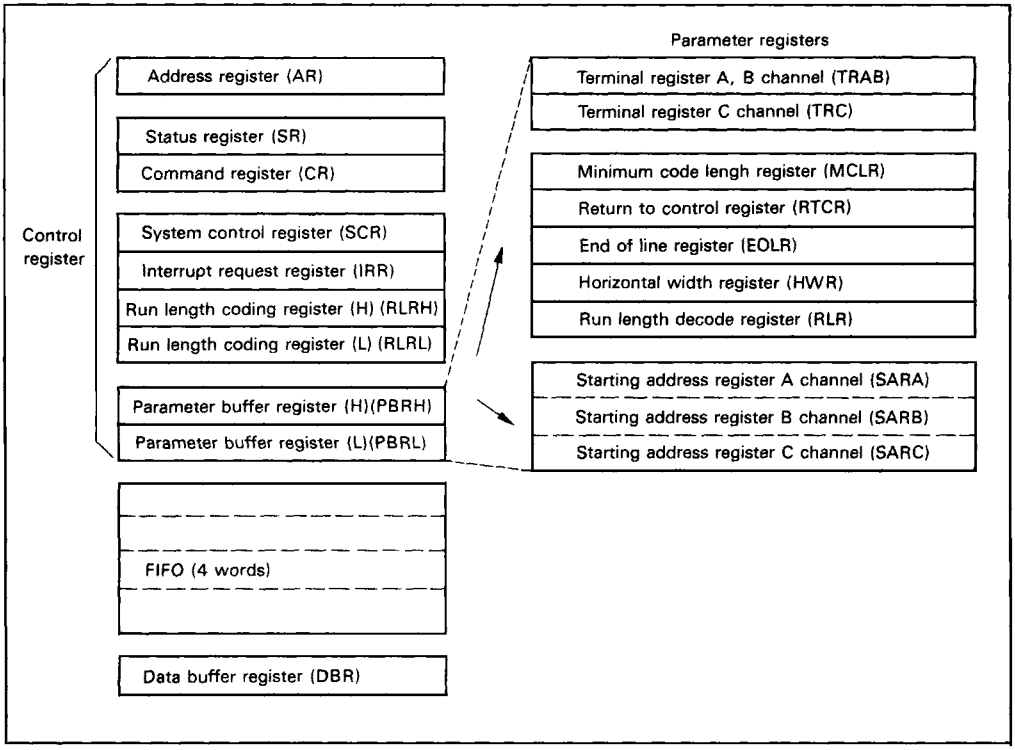


Figure 3 Register Programming Model

Table 1 Control Registers, FIFO and DBR

Address			R/W	Symbol	Full Name
A2	A1	A0			
0	0	0	R/W	SCR	System Control Register
0	0	1	R	IRR	Interrupt Request Register
0	1	0	R	SR	Staus Register
			W	CR	Command Register
0	1	1	R/W	FIFO	First-In First-Out Memory
1	0	0	R/W	DBR	Data Buffer Register
1	0	1	R/W	AR	Address Register
1	1	0	R	RLRH	Run Length coding Register High
			W	PBRH	Parameter Buffer Register High
1	1	1	R	RLRL	Run Length coding Register Low
			W	PBRL	Parameter Buffer Register Low

Table 2 Command

3	2	1	0	Command
0	0	0	0	Encode Initial Command
0	0	0	1	MH Coding Command
0	0	1	1	Transfer Command
0	1	0	1	MR One Dimensional Coding Command
0	1	1	0	MR Two Dimensional Coding Command
1	0	0	0	Decode Initial Command
1	0	0	1	MH Decoding Command
1	0	1	0	MR Decoding Command
1	0	1	1	Transfer Command

System Control Register (SCR)

The SCR is an 8-bit read/write register which controls several DICEP options.
The MPU must write desired bits to the SCR before issuing a command. Reading this register, the MPU can know the current status information of the DICEP.
During reset, the SCR is initialized to zero.
The SCR is shown in figure 4 and the individual bits are defined in the following paragraphs.

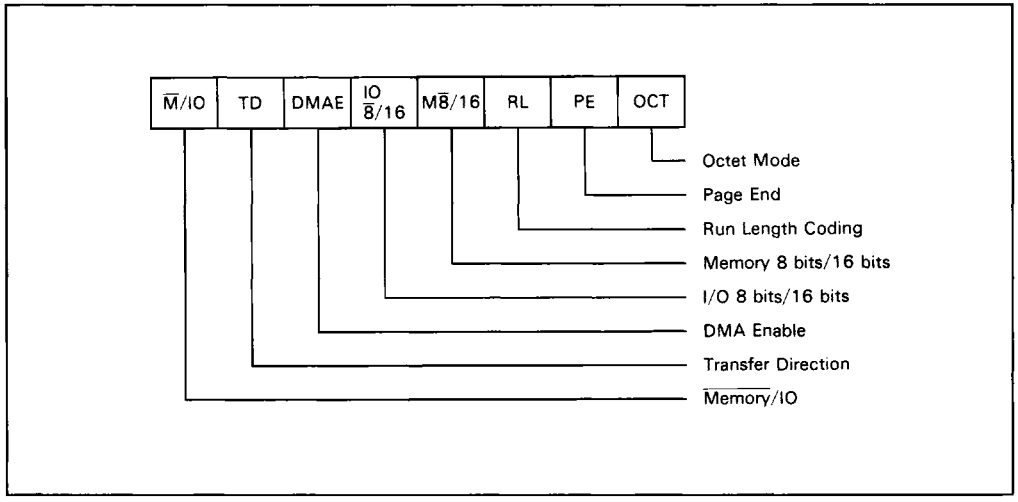


Figure 4 System Control Register (SCR)

Bit 0 Octet Mode bit (OCT)

If this bit is set, coded data must be 8-bit boundary conditioned.
when resulting coded data does not meet this requirement, Fill bits will be automatically added just after a data line to ensure that coded data is 8-bit boundary conditioned.
If this bit is clear, all of the coded data may not be sent to a memory on the system bus, because the transfer of data through the system bus is performed on 8-bit basis.
In M^2R coding scheme, however, fill bits must not added in any other place than the end of a page. Thus, when this coding scheme is used, OCT bit can be set only at the end of a page.

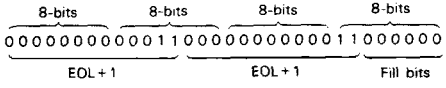
Bit 1 Page End bit (PE)

This bit must be set when a page of data has been coded.
If the MPU issues a coding command with PE set, the DICEP will generate the following RTC code words:

- If the MPU issues MH coding command, the DICEP will generate EOL code words. The number of EOLs must be specified by End of Line Register (EOLR)*.
- If the MPU issues MR one dimensional coding command, the DICEP will generate EOL + 1 code words. The number of EOL + 1 code words must be specified by EOLR.
- If the MPU issues MR two dimensional coding command, the DICEP will generate EOL + 0 code words. The number of EOL + 0 code words must be specified by EOLR.

(Note *) The End of Line Register (EOLR) specifies the number of EOL code words to be generated by the DICEP.

If the MPU issues MR one dimensional coding command when the EOLR contains "2" and both OCT bit and PE bit are set, the DICEP will generate the following code bits (provided preceding coded data are 8-bit boundary conditioned).



Bit 2 Run Length Coding bit (RL)

If the MPU issues MH coding command, MR one dimensional coding command or MH decoding command when Run Length coding bit is set, the DICEP will perform run length coding or decoding.
However, the MPU must not issue MR two dimensional coding command or MR decoding command with this bit set.

Bit 3 Memory 8 bits/16 bits (M$\overline{8}$/16)

The M$\overline{8}$/16 bit is used to specify the size of the document image bus. If the M$\overline{8}$/16 bit is set, the document image bus has a 16-bit size; if clear, the size is 8 bits.

Bit 4 I/O 8 bits/16 bits (IO$\overline{8}$/16)

The IO8/16 bit is used to specify the word size of the I/O devices on the document image bus.
If the IO8/16 bit is set, the I/O devices has a 16-bit wide size; if clear, the size is 8 bits.

!!CAUTION!!

When the document image bus has a 8-bit size, the I/O devices must not have a 16-bit word size. Thus, if M8/16 is clear, IO8/16 must not be set.

Bit 5 DMA Enable bit (DMAE)

The DMAE bit is used to enable DMA operation between the I/O devices and the document image memory.
If the DMAE bit is set, the DICEP accepts the DRQTI signal from the I/O devices.
The DMAE bit is cleared at the completion of DMA transfer of a scan line.

Bit 6 Transfer Direction bit (TD)

The TD bit is used to determine the direction of data transfer between the system bus and the document image bus. If the TD bit is clear, data is transferred from the system bus to the document image bus; if set, data is transferred from the document image bus to the system bus.

Bit 7 $\overline{\text{Memory}}$/IO bit ($\overline{\text{M}}$/IO)

The $\overline{\text{M}}$/IO bit is used during data transfer between the system bus and the document image bus. If the M/IO bit is clear, data will be transferred from or to the document image memory; if set, data will be transferred from or to the I/O devices.

Command Register (CR)

The CR is a 4-bit write-only register which is used to specify a command for the DICEP operation.
Responding to an MPU write to the CR, the DICEP starts execution of an indicated command. In other words, the MPU can issue the desired command by setting the corresponding CR bits.
All of the CR bits are cleared after initialization by $\overline{\text{RESET}}$ input.
When using this register, the user must give consideration to the followings:

- If the MPU writes a new data into the CR during a command execution, the DICEP may enter a new command execution without completing the current command.
- The state of Bit 3 in the CR determines the direction of DMA transfer through the document image bus.
  Be careful that changing the state of this bit during DMA transfer changes the direction of transfer.
- The direction of DMA transfer when an encode command is issued while DMA transfer is being performed is from I/O to image memory. Conversely, the direction of DMA transfer when a decode command is issued while DMA transfer is being performed is from image memory to I/O.

Figure 5 shows the relationship between the individual CR bits and the commands to be specified.

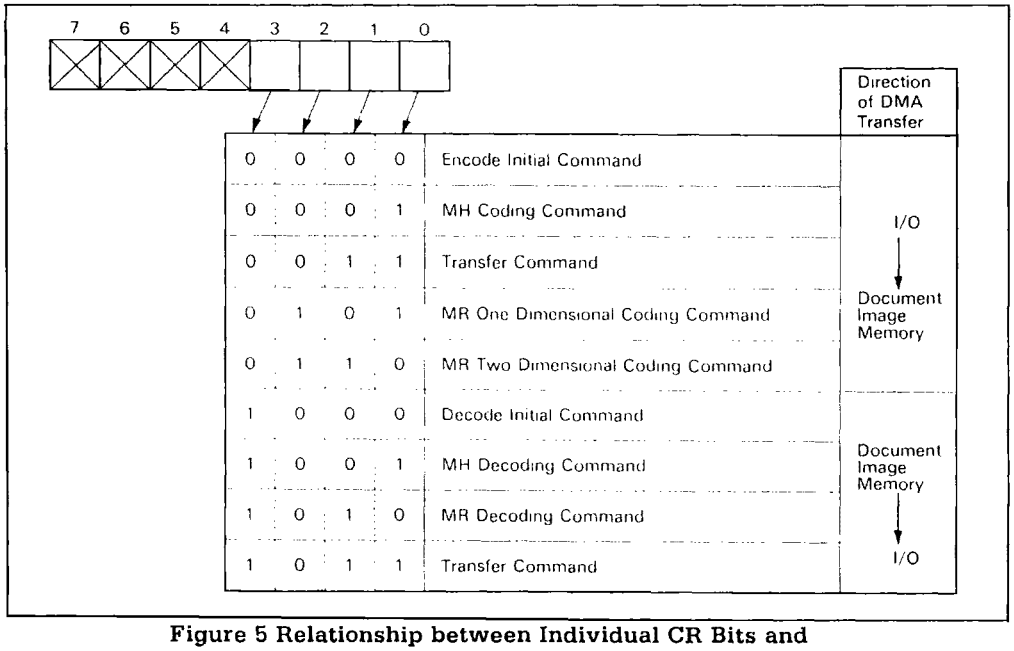


Figure 5 Relationship between Individual CR Bits and the Command to be Specified

The individual commands to be specified are described in the following paragraphs.

Encode Initial Command

The Encode Initial Command initializes the DICEP for coding operation, which clears the FIFO and clears the FIFO Ready Flag bit in the Status Register (SR). We recommend that this command should be issued at the start of a page coding.

The MPU must not issue the Encode Initial Command during DMA operation, because no interrupt is requested to the MPU at the completion of this command.

MH Coding Command

When the MPU issues the MH coding command, the DICEP will execute MH coding if the RL bit in the SCR is clear; if the RL bit is set, the DICEP executes run length coding.

MR One Dimensional Coding Command

When the MPU issues the MR one dimensional coding command, the DICEP will execute the one dimensional coding in the MR coding scheme if the RL bit is clear; if the RL bit is set, the DICEP executes run length coding.

MR Two Dimensional Coding Command

When the MPU issues the MR two dimensional coding command, the DICEP will execute the two dimensional coding in the MR coding scheme or the M^2R coding.

Transfer Command

When the MPU issues the transfer command, the DICEP will execute the transfer of data between the system bus and the document image bus. The direction of the transfer depends on the TD bit in the SCR.

Decode Initial Command

When the MPU issues the decode initial command, the DICEP is initialized for decoding operation. The FIFO is cleared and the FIFO Ready Flag bit in the Status Register (SR) is set to one.
The decode initial command must not be issued during DMA transfer.

MH Decoding Command

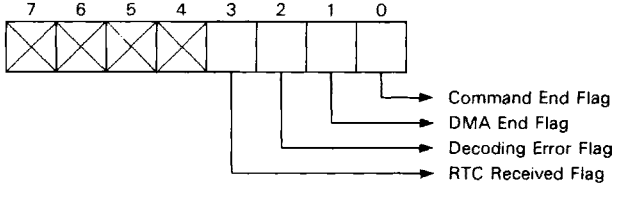
When the MPU issues the MH decoding command, the DICEP will execute the MH decoding if the RL bit in the SCR is clear; if the RL bit is set, the DICEP executes the run length decoding.

MR Decoding Command

When the MPU issues the MR decoding command, the DICEP will execute the MR decoding or the M^2R decoding.

Interrupt Request Register (IRR)

The IRR is a 4-bit read-only register. When the MPU receives an interrupt request from the DICEP, it can know what is the cause of the interrupt by reading the IRR.
After reset, the IRR is cleared to zero.
Figure 6 shows the relationship between the causes of interrupts and the states of individual IRR bits.



3	2	1	0	Indicates:
0	0	0	1	Completion of a Command
0	1	0	1	Occurrence of Decoding Error
1	0	0	1	Reception of RTC Code
		1	0	Completion of DMA Transfer
		0	0	No Interrupt Cause

Figure 6 Relationship between Causes of Interrupts and States of IRR Bits

The individual bits are defined as follows.

Bit 0 Command End Flag bit

This bit is set to indicate that a command has been executed to completion. During a decoding operation, this bit can give the MPU more information depending on the state of bit 2 or bit 3.

Bit 1 DMA End Flag bit

This bit is set to indicate that DMA transfer of a scan line has been completed.
When a command execution or a DMA operation is completed, either Bit 0 or Bit 1 is set to one to assert the IRQT. Bit 0 and Bit 1 never be set together. An MPU read of IRR clears Bit 0 and Bit 1 to negate the IRQT.
If the MPU reads the IRR when the IRQT is negated, the interrupt which occurs during the read cycle may not affect the IRR or the IRQT.

Bit 2 Decoding Error Flag bit

If both the Decoding Error Flag bit and the Command End Flag bit are set during a decoding operation, it indicates that an error has been found in the coded data.

Bit 3 RTC Received Flag bit

If both the RTC Received Flag bit and the Command End Flag bit are set during a decoding operation, it indicates that the DICEP has received RTC codes.
Both Bit 2 and Bit 3 are cleared to zero after a new command is issued.

First-In First-Out Memory (FIFO)

The FIFO is 4 words × 8 bits memory which is positioned in the Encoder and Decoder block of the DICEP. The FIFO stores coded data temporarily when the DICEP performs a coding or decoding operation.
During a coding operation, the DICEP encodes an image data and stores the coded data in the FIFO. Then either the MPU or the DMAC transfers the data into a memory on the system bus.
During a decoding operation, either the MPU or the DMAC transfers a coded data from a memory on the system bus to the FIFO. Then the DICEP decodes the data.
The state of the FIFO affects the FIFO Ready Fiag bit in the Status Register (SR) and the DRQTO signal.

Data Buffer Register (DBR)

The DBR is a bidirectional register which stores data temporarily during data transfer between the system bus and the document image bus.
If the TD bit in the SCR is zero, either the MPU or the DMAC transfers data from a memory on the system bus to the DBR.
Then the DICEP writes the data into the peripherals on the document image bus responding to the transfer command.
If the TD bit is one, the DICEP reads a data from a peripheral on the document image bus and writes the data into the DBR responding to the transfer command. Then either the MPU or the DMAC reads the data from the DBR.
The state of the DBR affects the DBR Ready Flag bit in the Status Register (SR) and the DRQTO signal.

Address Register (AR)

The AR is used to specify the address of a parameter register. In addition, the MPU can know which parameter is specified by reading the AR.
The MPU must verify that the PBR Ready Flag bit is set before changing the contents of the AR.
The AR is shown in figure 7.

The five low-order bits of the AR can be read and written, but Bit 7 is read-only bit.

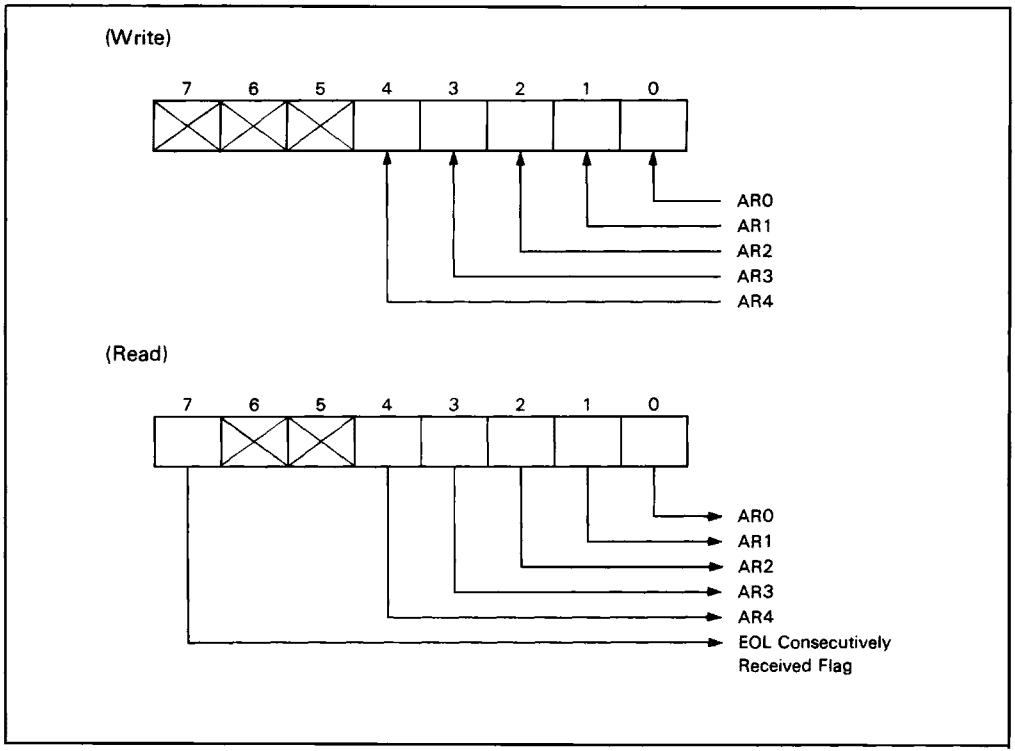


Figure 7 Address Register (AR)

Bit 7 in the Address Register has following features:

- becomes zero when the DICEP has received two or more consecutive EOLs, and
- becomes one after the $\overline{\text{RESET}}$ input or an initiation of a decoding command.

Because of these features, the Bit 7 is used as EOL Consecutively Received Flag bit during a decoding operation.

Figure 8 shows the relationship between the coded data received by the DICEP during a decoding operation and the Bit 7.

When receiving an EOL, the DICEP recognizes that a command is completed, then applies an interrupt to the MPU. Responding to this interrupt, the MPU issues a decoding command.
Issuing an decoding command clears the Bit 7 to one. Then if the DICEP receives another EOL code word, the Bit 7 is set to zero. If the DICEP does not receive any more EOL code word, the Bit 7 remains one.

Thus, if the MPU reads the AR after a decoding of a scan line prior to an initiation of a new command, the state of the Bit 7 indicates whether the DICEP has received two or more consecutive EOL code words at the start of the decoded scan line.

If the Bit 7 is zero, it indicates that the DICEP has received two or more EOL code words just before the data line. If the Bit 7 is one, it indicates that the DICEP has received an EOL code word just before the data line.

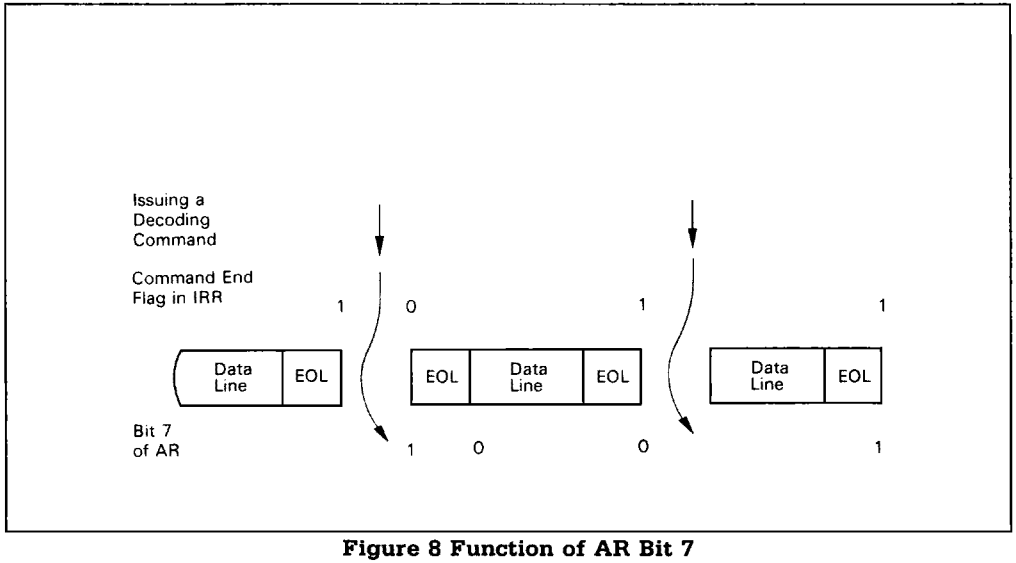


Figure 8 Function of AR Bit 7

Parameter Buffer Register Low and Parameter Buffer Register High (PBRL & PBRH)

If the MPU writes a data into the PBRH, then the PBRL, the data will be automatically written as a parameter into a parameter register specified by the AR.
The MPU must verify that the PBR Ready Flag bit is set before the write to the PBRH and the PBRL.
The AR, the PBRL and the PBRH will contain the current data until a new data is written.

Run Length Register Low and Run Length Register High (RLRL & RLRH)

The MPU can monitor the run length by reading the RLRH, then the RLRL during the run length coding operation.
Before the read of these registers, the MPU must verify that the RLR Ready Flag bit in the Status Register (SR) is set.

Status Register (SR)

This 4-bit read-only register indicates to the MPU the current status information of the FIFO, the DBR, the PBRH, the PBRL, the RLRH and the RLRL.
The SR is shown in figure 9 and the individual bits are defined as follows.

Bit 4 RLR Ready Flag bit

This bit is set to indicate that the RLRH and the RLRL contain valid run length codes. This bit is cleared after the MPU issues a new command.

Bit 5 FIFO Ready Flag bit

If this bit is set during a coding opration, it indicates that the FIFO contains valid coded data of more than 1 byte, which allows either the MPU or the DMAC to read the data from the FIFO.
If set during a decoding operation, it indicates that the FIFO has empty area of more than 1 byte, which allows either the MPU or the DMAC to write coded data into the FIFO.
Thus, this bit is cleared after the MPU issues the encode initial command and set after the MPU issues the decode initial command.
During a coding or decoding operation, the state of this flag bit affects the DRQTO signal.
This bit is cleared after initialization by the $\overline{\text{RESET}}$ input.

Bit 6 DBR Ready Flag bit

During the transfer of data from the system bus to the document image bus (that is, when the TD bit in the SCR is clear), this flag is set to indicate that the DBR is empty, which allows either the MPU or the DMAC to write data into the DBR.
During the transfer of data from the document image bus to the system bus (that is, when the TD bit is set), this flag is set to indicate that the DBR contains valid data, which allows either the MPU or the DMAC to read the data from the DBR.
If the MPU issues the data transfer command with the TD bit clear, the DBR Ready Flag bit will be set to one. If the MPU issues the transfer command when the TD bit is set, the DBR Ready Flag bit will be clear until the DICEP writes a new data into the DBR.
While the transfer command is executed, this flag affects the DRQTO signal.

Bit 7 PBR Ready Flag bit

This bit is set to indicate that both the PBRL and the PBRH are empty, which indicates that the MPU can write a new data into the PBRL and the PBRH. This flag bit is set after initialization by the $\overline{\text{RESET}}$ input or the initiation of a new command.

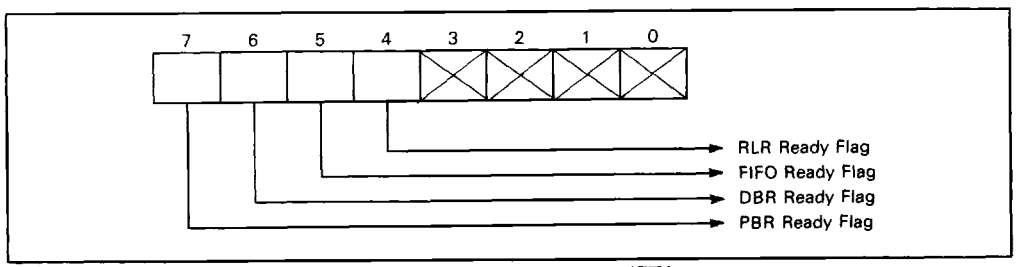


Figure 9 Status Register (SR)

Parameter Registers

The DICEP provides Parameter registers as listed in table 3

Table 3 Parameter Registers

Address (AR)							
AR4	AR3	AR2	AR1	AR0	Coding	Decoding	Name
0	0	0	0	0	○	○	Terminal Register A, B Channel (TRAB)
0	0	0	0	1	○	○	Terminal Register C Channel (TRC)
0	0	0	1	0	○	Not Uesd	Minimum Code Length Register (MCLR)
					Not Uesd	○	Return to Control Register (RTCR)
0	0	0	1	1	○	○	End of Line Register (EOLR)
0	0	1	0	0	○	○	Horizontal Width Register (HMR)
0	0	1	0	1	○	○	Starting Address Register A Channel (SARA)
0	0	1	1	0	○	○	Starting Address Register B Channel (SARB)
0	0	1	1	1	○	○	Starting Address Register C Channel (SARC)
0	1	0	0	0	×	○	Run Length Decode Register (RLR)

(Note 1) ○·····Writable ×·····Not Writable
(Note 2) The other addresses than above listed must not be written in the AR.
(Note 3) A Channel is :
- the coding line during the coding operation
- the decoding line during the decoding operation
- the transfer line during the data transfer

B Channel is : the reference line
C Channel is : the DMA line

Register accessible via the parameter buffer registers (PBRH, PBRL)

The parameter registers can be accessed via the parameter buffer registers (PBRH, PBRL). The MPU specifies a parameter register using the address register (AR). A parameter written to the parameter buffer registers is then written to the corresponding parameter register. The MPU writes parameters to parameter registers in the following sequence:

The MPU can write a desired parameter data into these registers by a sequence which :
- verifies that the PBR Ready Flag bit is set,
- writes the address of an intended parameter register into the AR, then
- writes a desired parameter data into PBRH then PBRL.

An MPU write to PBRL indicates to the DICEP that the address and the parameter data are ready. Then the parameter data is written into the parameter register specified by the address.

Registers other than the SARA, the SARB and the SARC hold the written data.
The individual parameter registers will be described in the following paragraphs.

Terminal Register A, B Channel (TRAB)

The TRAB specifies the number of pels along an A or B channel scan line to be processed on a bit basis.
When the document image bus has an 8-bit size, the three least significant bits of this register must be zeroes. When the document image bus has a 16-bit size, the four least significant bits must be zeroes.

(ex.) If the number of pels along an A or B channel line to be processed is 1728 pels, the individual bits of TRAB will be as follows.

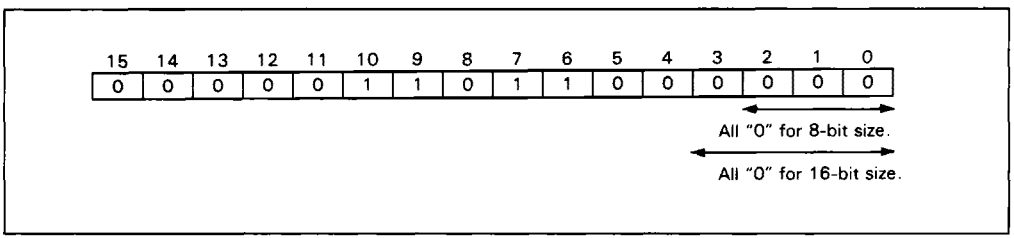


Figure 10 Terminal Register A, B Channel (TRAB)

Terminal Register C Channel (TRC)

The TRC specifies the number of bits on a scan line to be processed during a DMA transfer through the document image bus. When the document image bus has an 8-bit size, the three least significant bits of this register must be zeroes. When the document image bus has a 16-bit size, the four least significant bits must be zeroes.

Minimum Code Length Register (MCLR)

The MCLR specifies the minimum length of a coded scan line on a bit basis. If the actual coded line is shorter than the specified one, the Fill bits will be added.
The MCLR can be used to specify the minimum transmission time of a coded scan line. The MPU can specify the minimum transmission time of 10 msec for the facsimile with transmission rate of 9600 bit/sec by writing 96 into the MCLR.
Clearing the MCLR leads the DICEP to generate no Fill bits.

Return to Control Register (RTCR)

The RTCR contains the number of consecutive EOL code words which should be recognized as a RTC code word during a decoding operation.

End of Line Register (EOLR)

During a coding operation, the EOLR is used to specify the number of EOL code words which will be generated at the start of every coded line. If the EOLR is clear, the DICEP generates no EOL code word.
The EOLR is also used to specify the number of EOL code words which should be recognized as a RTC code word at the end of a page (when the PE bit in the SCR is set).
During a decoding operation, either one or zero is writtin to the EOLR. If zero has been written, it indicates that the coded data includes no EOL code word.

Horizontal Width Register (HWR)

The Horizontal width Register specifies the lingth of a scan line on a byte basis. When the document image bus has a 16-bit size, the least significant bit must be zero.
The width of an ISO A4 document is 1728 pels. However, when the document is to be coded, it is recommended to set 2048 pels as the scan-line length for effective use of 64k Byte of document image memory.

(ex.) If the scan-line length is 2048 pels, 256 is written into the HMR. (2048÷8=256)

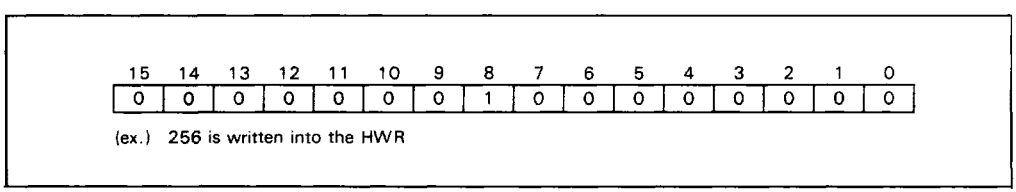


Figure 11 Horizontal Width Register (HWR)

Starting Address Register A Channel (SARA)

The Starting Address Register A Channel specifies the starting address of a document memory space which stores the current A channel line.
As the SARA stores parameters on a byte basis, if the document image bus has a 16-bit size, the least significant bit of the SARA must be zero. However, when the data transfer is performed between 8-bit word size I/O device and the system bus, this requirement is ignored.
During a coding operation, the SARA specifies the starting address of a document image memory space which stores image data to be coded.
During a decoding operation, the SARA specifies the starting address of a document image memory space which will store decoded image data.
During a data transfer between two buses, the SARA specifies the starting address of a document image memory space which stores the data transferred to or from the system bus.
Upon completion of coding, decoding or transfer of every line, the SARA is automatically updated to the following value.

(Current Value of SARA)+(Value of HWR)=(New Value of SARA)

If the starting address of the next scan line is the same as the automatically updated address, the MPU don't have to write the starting address to this register on every scan line.

Starting Address Register B Channel (SARB)

The starting Address Register B Channel specifies the starting address of the document image memory space which stores the current reference line.
As the SARB stores parameters on a byte basis, if the document image bus has a 16-bit size, the least significant bit must be zero.
This register is automatically updated on every scan line in the same way as the SARA.

(CAUTION)
If an error is detected during a decoding operation, the contents of SARA or SARB will not updated.

Starting Address Register C Channel (SARC)

The Starting Address Register C Channel specifies the starting address of the document image memory space which stores the current DMA line.
As the SARC stores parameters on a byte basis, if the document image bus has a 16-bit size, the least significant bit of the SARC must be zero.
The content of this register is automatically updated on every scan line in the same way as SARA and SARB.

Run Length Register (RLR)

The Run Length Register contains run length codes during a run length decoding operation. When a line of run length codes are written into the RLR, the DICEP will decode the data.

Coding and Decoding Scheme

MH Coding scheme

In the MH coding scheme, one dimensional coding is performed on all lines of data, One dimensional coding encodes run lengths of white pels and black pels which alternate on a scan line.
A one dimensionally coded scan line is made of a data line, End of Line code words and, if necessary, Fill bits.

MR Coding Scheme

In MR coding scheme, the one dimensional coding is performed on a scan line, then the two dimensional coding is performed on at most K-1 successive lines. The maximum value of K shall be 2 if standard vertical resolution is used and shall be 4 if higher vertical resolution is used.

M^2R Coding Scheme

M^2R coding scheme is used for the Group 4 facsimile apparatus. In this scheme, all lines of data are coded two dimensionally. At the coding of the first line of a page, a white reference line is imaginarily set immediately above the coding line. This scheme requires neither fill bits nor line synchronization code words.

Run Length Coding Scheme

In addition to the above mentioned coding schemes, the DICEP provides run length coding scheme. In run length coding scheme, the run length of all white or black is generated without data compression (below shown figure 12).

The DICEP is designed to realize a wide variety of user applications. These applications are organized into two groups, that is the independent bus system and the common bus system.
This section offers examples of the two types of applications.

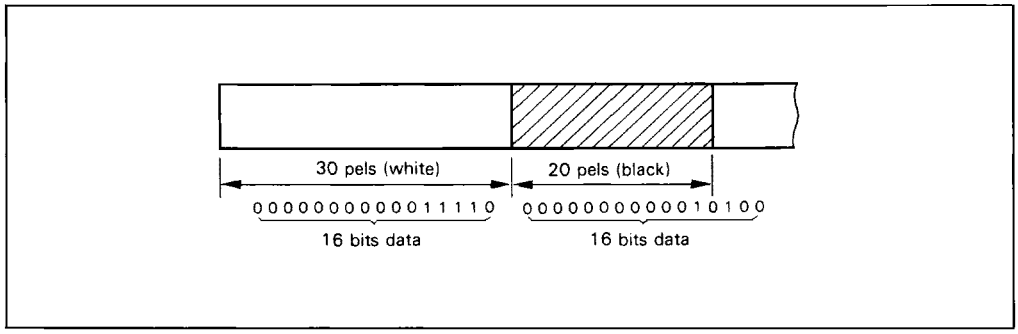


Figure 12 Coding Data (Run length coding scheme)

Absolute Maximum Rating

Item	Symbol	Value	Unit
Supply Voltage	V_{DD} *	-0.3 to +0.7	V
Input Voltage	V_{in} *	-0.3 to V_{DD}+0.3	V
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150 (PC-72)	°C
		-55 to +125 (DP-64S)	

* Voltages referenced to V_{SS}=0V.

Recommended Operating Conditions

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{DD} *	4.75	5	5.25	V
Input Voltage	V_{IL} *	-0.3	–	0.8	V
	V_{IH}	2.2	–	V_{DD}+0.3	V
Operating Temperature	T_{OPR}	0	25	70	°C

* Voltages referenced to V_{SS}=0V.

<Use Precautions>

(1) Pay attention to dielectric breakdown. In handling, ground your body through a high resistance (500 or 600k to 1MΩ).
(2) This device operates at a high speed. Wire its signal lines with care to prevent noise caused by crosstalk of reflection.
(3) It is recommended to put a bypass capacitor between V_{DD} and V_{SS} (GND) to eliminate wire noise. (C=1μF min.)
(4) CMOS has the following specific problem: If the input signal level goes to the intermediate value (V_{IL} MAX ≦ V_{IN} ≦ V_{IH} MIN), I_{DD} increases and may cause a latch-up event. Pay special attention to the case as the buses, input terminals or unused terminals float at a power-on time.

Electrical Characteristics

DC Characteristics (V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit	Test Condition
Input High Voltage	V_{IH}	2.2	–	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	-0.3	–	0.8	V	
Input Leakage Voltage	I_{IN}	-10	–	10	μA	V_{in}=0 to 5.25V
Three-State (Off State) Leakage Current	I_{TSI}	-10	–	10	μA	V_{in}=0 to 5.25V
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH}=-400μA
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL}=2mA
Power Dissipation	P_D	–	150	250	mW	

AC Characteristics

Clock Timing (V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C unless otherwise noted.)

Item	Symbol	min	typ	max	Unit	Application Terminal	Test Condition
4CLK Cycle Time	ϕ_{4CLK}	31.25	–	500	ns	4CLK	Figure 13

System Bus Timing

Using a 68 Type MPU (V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C Cout=140pF unless otherwise noted.)

Item	Symbol	min	typ	max	Unit	Application Terminal	Test Condition
DS Cycle Time	t_{CYCE}	500	–	–	ns	DS	Figure 14, 17
DS Pulse Width	PW_{EH} PW_{EL}	220	–	–	ns	DS	
DS Rise or Fall Time	t_{Er} t_{Ef}	–	–	25	ns	DS	
Address Setup Time	t_{AS}	70	–	–	ns	$\overline{CS}$, A0-A2, R/$\overline{W}$	Figure 14
Address Hold Time	t_{AH}	30	–	–	ns	$\overline{CS}$, A0-A2, R/$\overline{W}$	
Output Data Delay Time	t_{DDR}	–	–	180	ns	D0-D7	Figure 14, 17
Output Data Hold Time	t_{DHR}	10	–	–	ns	D0-D7	
Input Data Setup Time	t_{DSW}	60	–	–	ns	D0-D7	
Input Data Hold Time	t_{DHW}	40	–	–	ns	D0-D7	
IRQT Inactive Delay Time	t_{IRQT}	ϕ_{4CLK} ×4+180	–	ϕ_{4CLK} ×8+180	ns	IRQT	Figure 14
$\overline{DACKI}$ Setup Time	t_{AS}	70	–	–	ns	$\overline{DACKI}$	Figure 17
$\overline{DACKI}$ Hold Time	t_{AH}	30	–	–	ns	$\overline{DACKI}$	
DRQTO Inactive Delay Time	t_{DRQTO}	–	(90)	180	ns	DRQTO	

Using an 80 Type MPU

(V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C Cout=140pF unless otherwise noted.)

Item	Symbol	min	typ	max	Unit	Application Terminal	Test Condition
Address Setup Time	t_{AR}	70	–	–	ns	$\overline{CS}$, A0-A2,	Figure 15
Address Hold Time	t_{RA}	30	–	–	ns	$\overline{CS}$, A0-A2,	
Output Data Delay Time	t_{RD}	–	–	180	ns	D0-D7	Figure 15, 18
Output Data Hold Time	t_{DR}	10	–	–	ns	D0-D7	
Read Pulse Width	t_{RW}	200	–	–	ns	DS	
Adress Setup Time	t_{AW}	70	–	–	ns	$\overline{CS}$, A0-A2	Figure 16
Adress Hold Time	t_{WA}	30	–	–	ns	$\overline{CS}$, A0-A2	
Input Data Setup Time	t_{WD}	60	–	–	ns	D0-D7	Figure 16, 19
Input Data Hold Time	t_{DW}	40	–	–	ns	D0-D7	
Write Pulse Width	t_{WW}	200	–	–	ns	R/$\overline{W}$	
IRQT Inactive Delay	t_{IRQT}	ϕ_{4CLK} ×4+180	–	ϕ_{4CLK} ×8+180	ns	IRQT	Figure 15
$\overline{DACKI}$ Setup Time	t_{AR}	70	–	–	ns	$\overline{DACKI}$	Figure 18
$\overline{DACKI}$ Hold Time	t_{RA}	30	–	–	ns	$\overline{DACKI}$	
$\overline{DACKI}$ Setup Time	t_{AW}	70	–	–	ns	$\overline{DACKI}$	Figure 19
$\overline{DACKI}$ Hold Time	t_{WA}	30	–	–	ns	$\overline{DACKI}$	
DRQTO Inactive Delay	t_{DRQTO}	–	(90)	180	ns	DRQTO	Figure 18, 19

Document Image Bus Timing

V_{DD}=5.0V±5%, V_{SS}=0V, Ta=0 to +70°C Cout=140pF unless otherwise noted. However, the values in the parentheses are the values at Cout=50pF.

Item	Symbol	min	typ	max	Unit	Application Terminal	Test Condition
Address Enable Active Delay Time	t_{DAEL}	–	(70)	150	ns	$\overline{MAEN}$	Figure 20, 21
Address Enable Inactive Delay Time	t_{DAEH}	–	(70)	140	ns	$\overline{MAEN}$	
Address Strobe Active Delay Time	t_{DASH}	–	(70)	140	ns	MAS	
Address Strobe Inactive Delay Time	t_{DASL}	–	(60)	120	ns	MAS	
Data Strobe Valid Delay Time	t_{DDSV}	–	(60)	140	ns	$\overline{UDS}$, $\overline{LDS}$	
Data Strobe Active Delay Time	t_{DDSL}	–	(75)	140	ns	$\overline{UDS}$, $\overline{LDS}$	
Data Strobe Inactive Delay Time	t_{DDSH}	–	(75)	140	ns	$\overline{UDS}$, $\overline{LDS}$	

(to be continued)

(continued)

Item	Symbol	min	typ	max	Unit	Application Terminal	Test Condition
Data Enable Active Delay Time	t_{DDEL}	–	(80)	130	ns	$\overline{MDEN}$	Figure 20
Data Enable Inactive Delay Time	t_{DDEH}	–	(75)	140	ns	$\overline{MDEN}$	
Read Valid Delay Time	t_{DRDV}	–	(60)	140	ns	$\overline{IOR}$, $\overline{MR}$	Figure 20, 21
Read Active Delay Time	t_{DRDL}	–	(70)	140	ns	$\overline{IOR}$, $\overline{MR}$	
Read Inactive Delay Time	t_{DRDH}	–	(75)	140	ns	$\overline{IOR}$, $\overline{MR}$	
Write Valid Delay Time	t_{DWRV}	–	(60)	140	ns	$\overline{IOW}$, $\overline{MW}$	Figure 20, 21
Write Active Delay Time	t_{DWRL}	–	(70)	140	ns	$\overline{IOW}$, $\overline{MW}$	
Write Inactive Delay Time	t_{DWRH}	–	(80)	140	ns	$\overline{IOW}$, $\overline{MW}$	
Address Valid Delay Time	t_{MAV}	–	(75)	140	ns	MA/MD0-MA/MD15	
Address Hold Delay Time	t_{MAH}	25	(50)	–	ns	MA/MD0-MA/MD15	
Data Setup Time (Read)	t_{DSR}	10	(10)	–	ns	MA/MD0-MA/MD15	Figure 20
Data Hold Time (Read)	t_{DHR}	70	(70)	–	ns	MA/MD0-MA/MD15	
Data Delay Time (Write)	t_{DDW}	–	(95)	170	ns	MA/MD0-MA/MD15	
Data Hold Time (Write)	t_{DHW}	15	(15)	–	ns	MA/MD0-MA/MD15	
DMA Acknowlege Active Delay Time	t_{DAKL}	–	(60)	140	ns	$\overline{DACKO}$	Figure 21
DMA Acknowlege Inactive Delay Time	t_{DAKH}	–	(65)	140	ns	$\overline{DACKO}$	
DMA Active Delay Time	t_{DDMAL}	–	(80)	140	ns	$\overline{DMA}$	
DMA Inactive Delay Time	t_{DDMAH}	–	(70)	140	ns	$\overline{DMA}$	
DTC Active Delay Time	t_{DDTCH}	–	$(\phi_{4CLK}+75)$	$\phi_{4CLK}+140$	ns	DTC	
DTC Inactive Delay Time	t_{DDTCL}	–	(50)	130	ns	DTC	

3

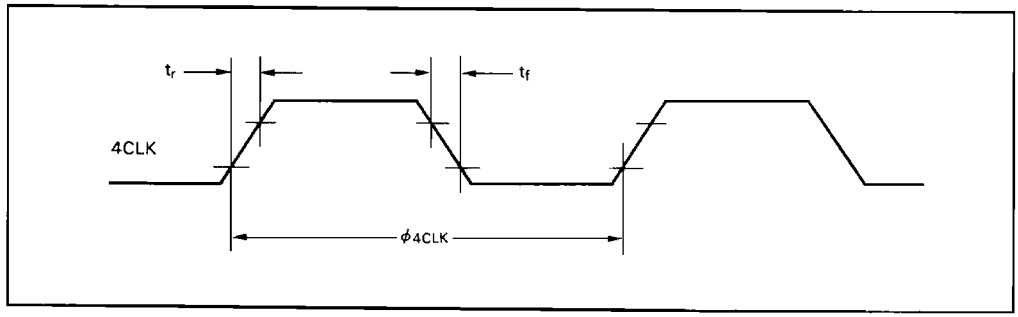


Figure 13 Clock Timing

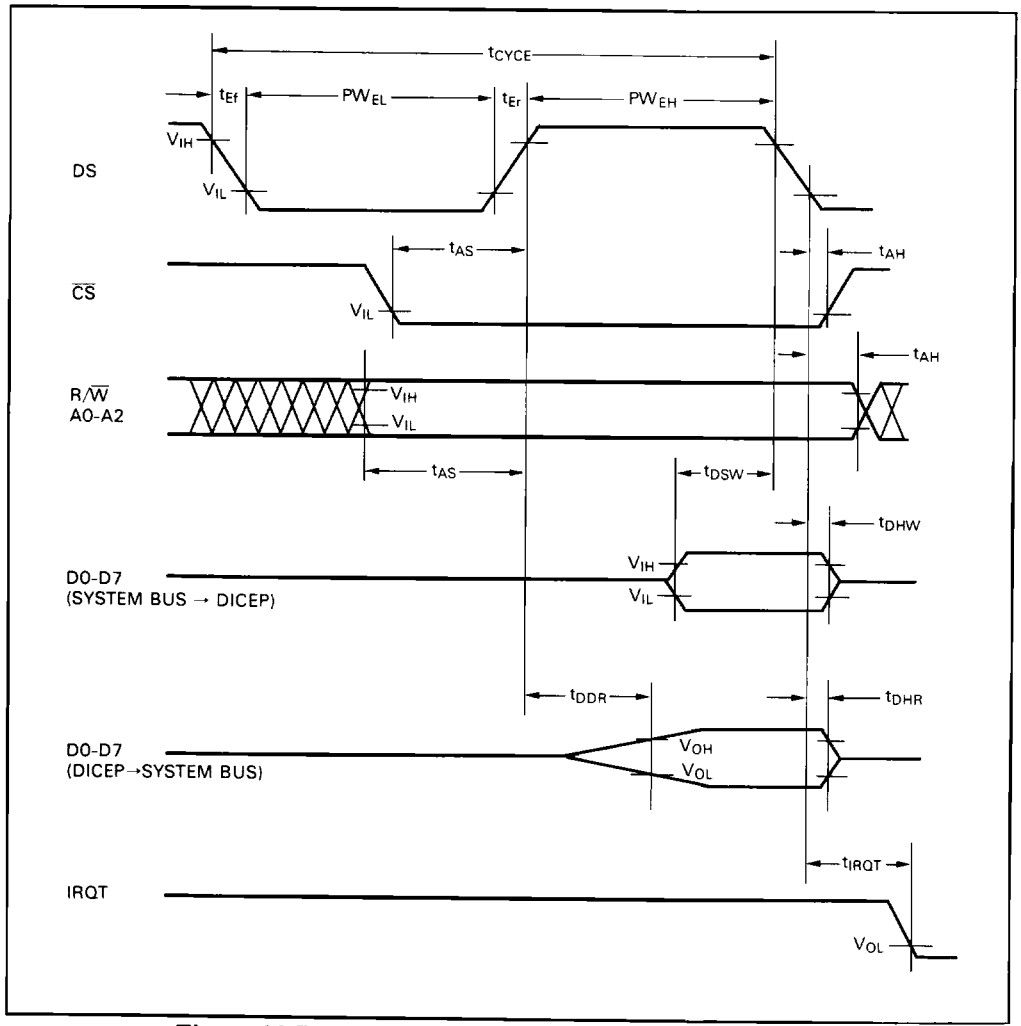


Figure 14 System Bus Read/Write Timing (68 Type MPU)

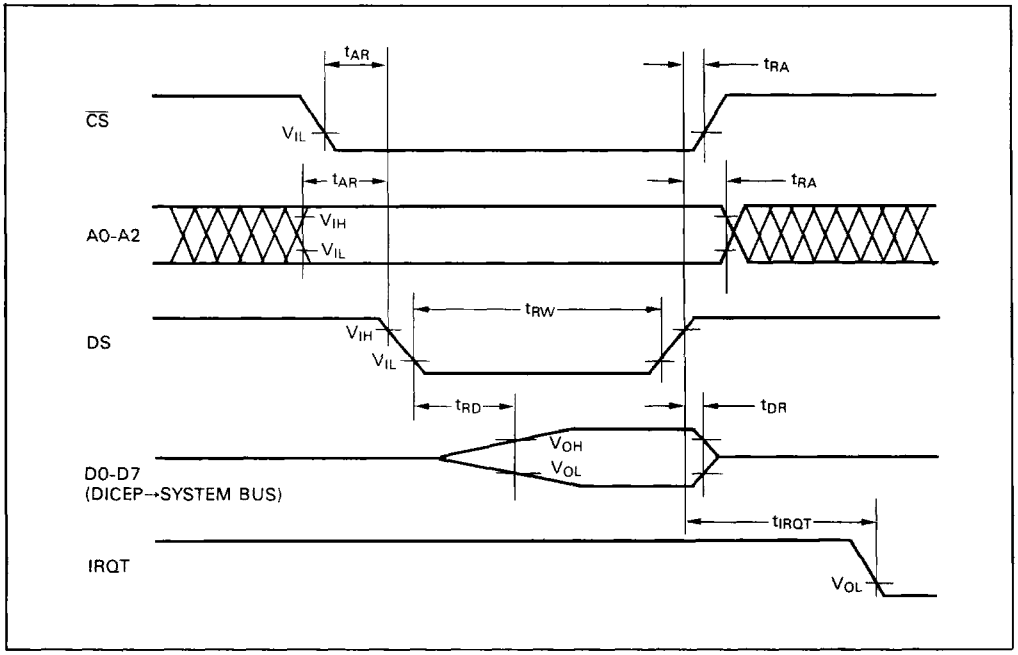


Figure 15 System Bus Read Timing (80 Type MPU)

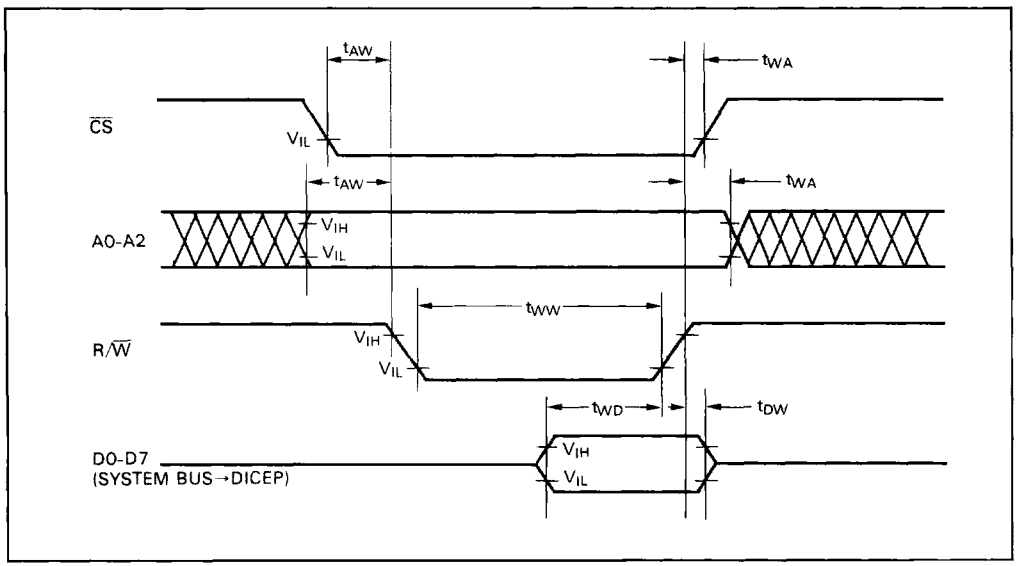


Figure 16 System Bus Write Timing (80 Type MPU)

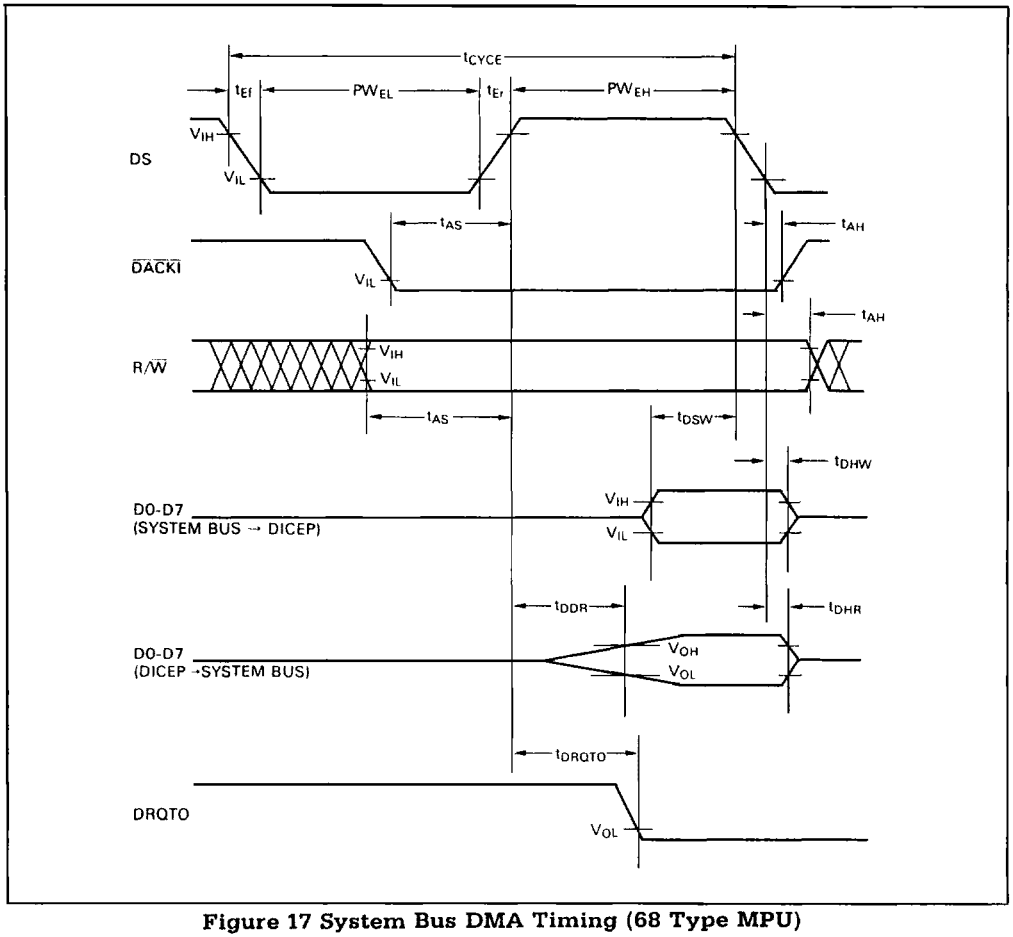


Figure 17 System Bus DMA Timing (68 Type MPU)

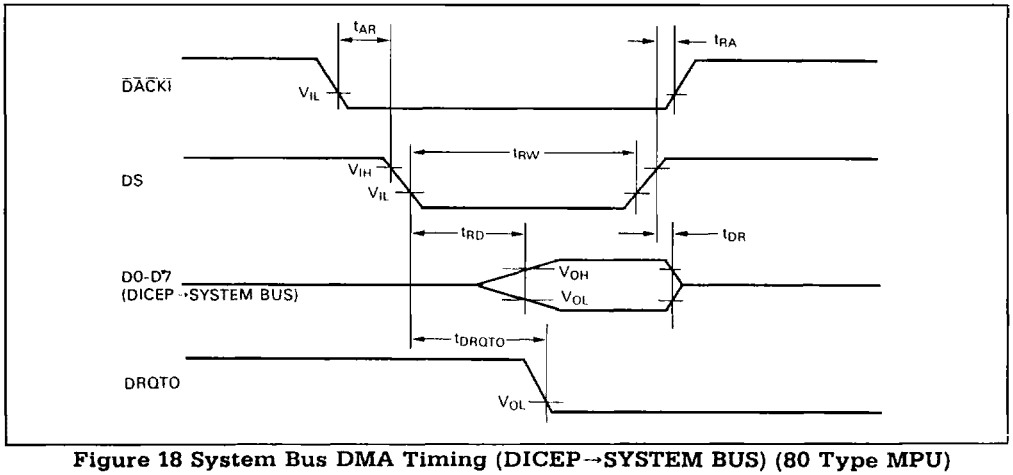


Figure 18 System Bus DMA Timing (DICEP→SYSTEM BUS) (80 Type MPU)

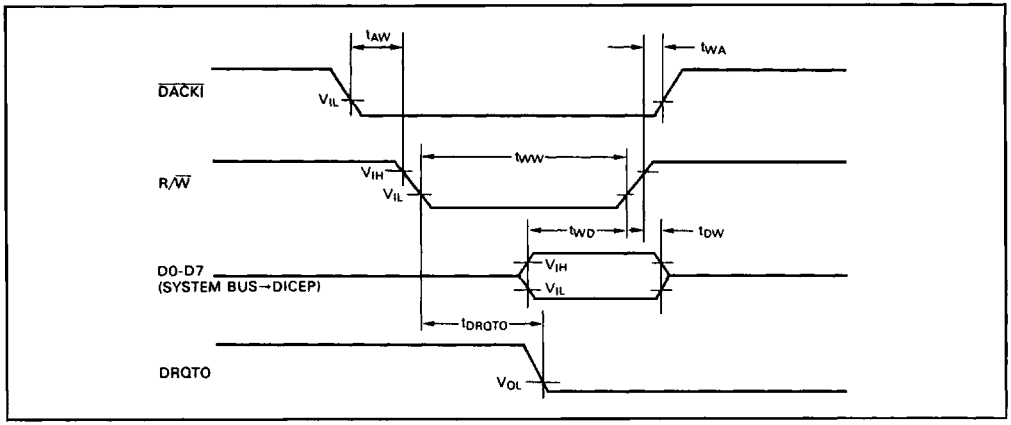


Figure 19 System Bus DMA Timing (SYSTEM BUS→DICEP) (80 Type MPU)

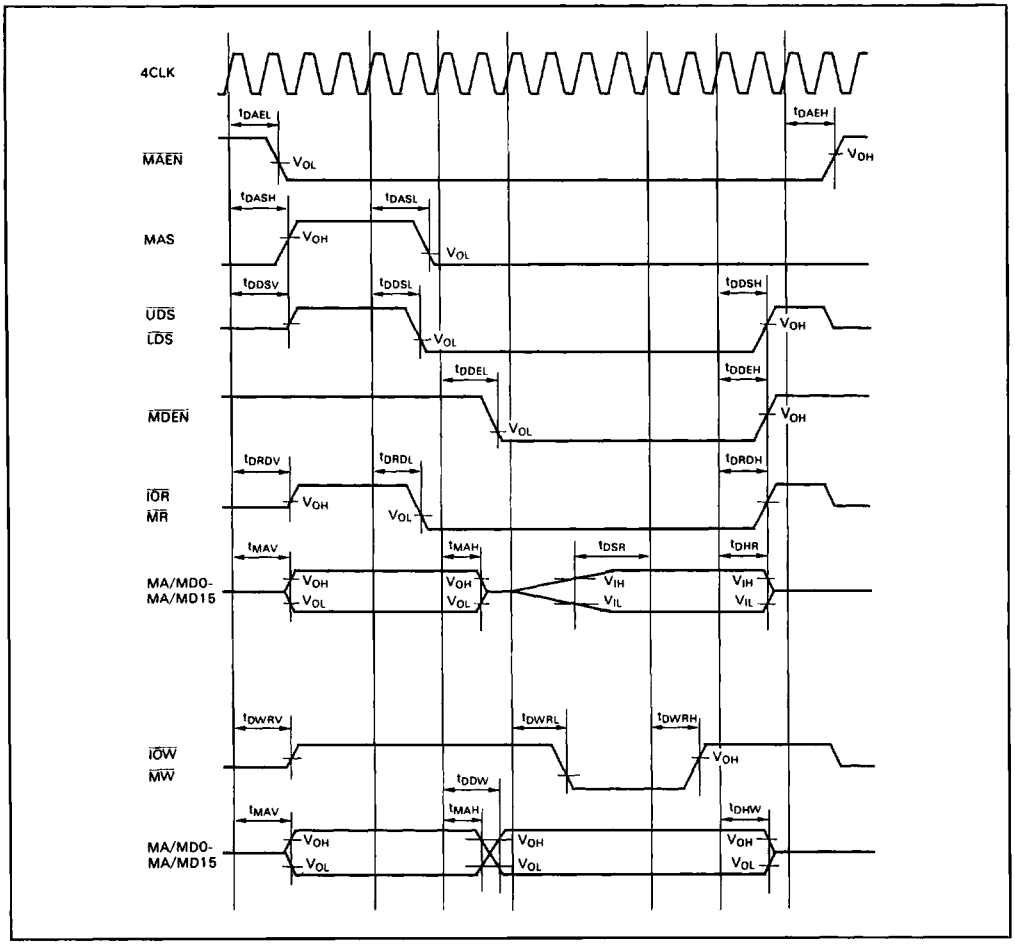


Figure 20 Document Image Bus Read/Write Timing

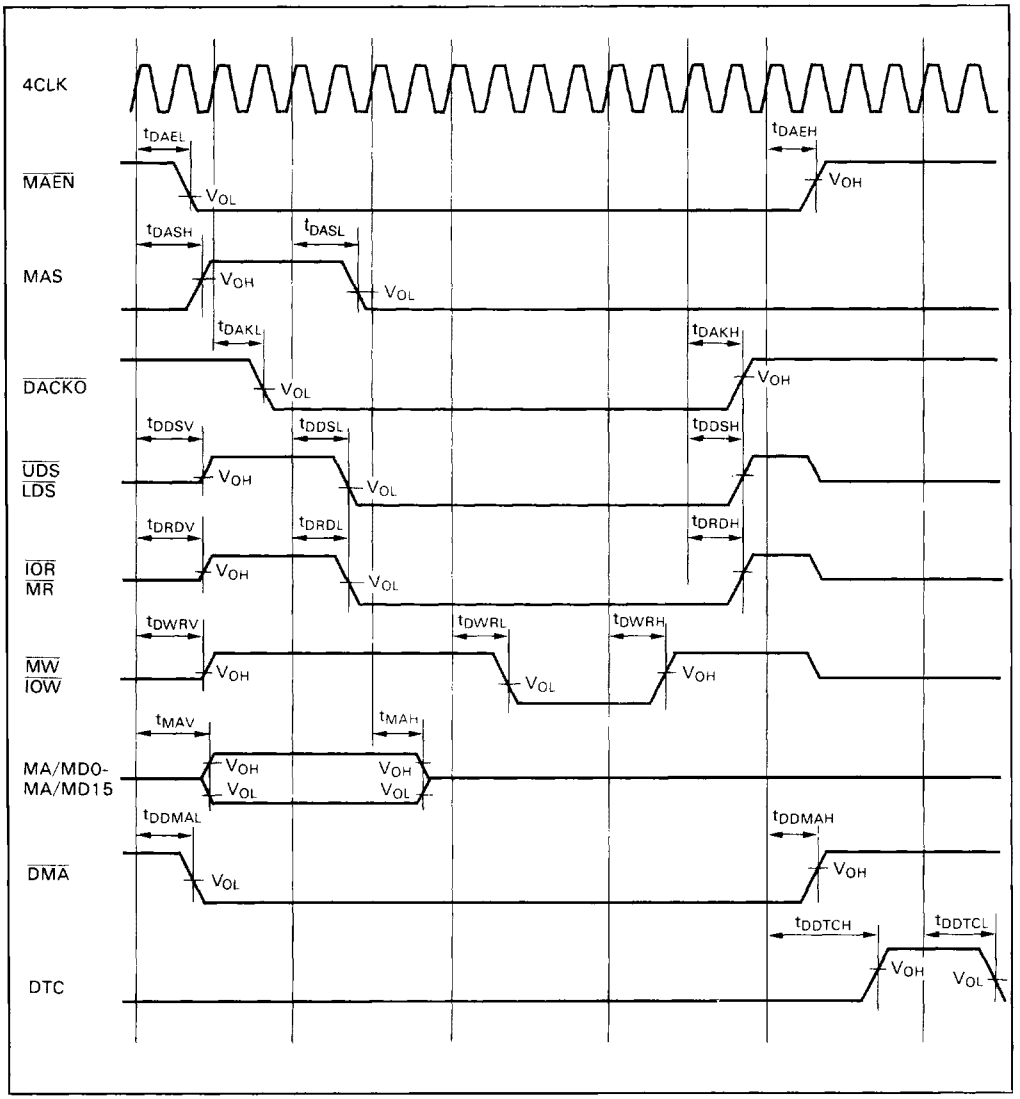


Figure 21 Document Image Bus DMA Timing

Refer to user's manual (No. AD-E0088) for detail of this product.