MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX818 CTCSS Signaling Processor

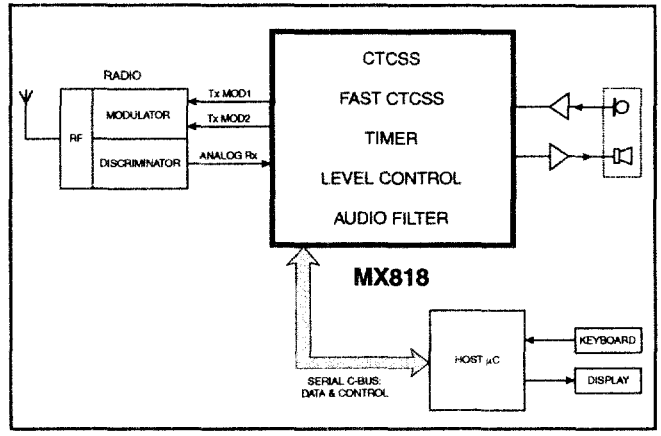
PRELIMINARY INFORMATION

Features

- Fast CTCSS Detection
- Non Predictive Tone Detection
- Low Power 3.3V/5.0V Operation
- Variable Gain Audio Filter
- Programmable:
  - Modulator Drivers
  - Tone Decoder
  - Tone Encoder
- Pin compatible with enhanced function MX828
- Full control via 4-Wire Serial Interface

Applications

- Radio Systems Requiring Sub-Audible Signaling
  - Trunking Control
  - Selective Calling
  - Group Calling
- Increased Efficiency
  - Scanning Systems
  - Trunking Systems



The MX818 is a low power CTCSS Signal Processor designed for use in the latest generation of LMR (Land Mobile Radio) equipment where sub-audible signaling is required for functions such as Trunking Control, Selective Calling and Group Calling applications. The MX818 is full duplex and offers many advanced features to assist in the operation of new CTCSS based systems including: programmable tone decoders to facilitate the decoding of between 1 and 15 programmable CTCSS tones, a CTCSS Fast/Predictive detector which may respond to a single programmed tone in less than 60ms, a high resolution tone encoder that will accurately generate CTCSS tones, and High and Low pass filters for CTCSS and Voice Band signals. The MX818 also provides on chip audio summation and digitally adjustable modulation drivers to facilitate design integration and reduce part count.

The MX818 may be used with a 3.0 to 5.5 volt supply and is available in the following packages: 24-pin SSOP(MX818DS), 24-pin SOIC (MX818DW), and 24-pin PDIP (MX818P).

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1. Block Diagram

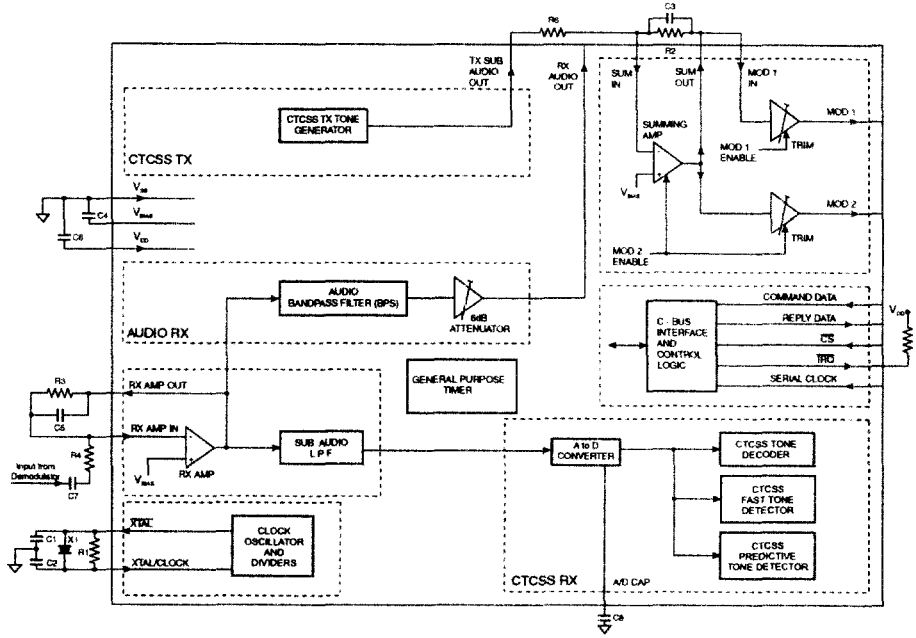


Figure 1: Device Block Diagram

2. Signal List

Pin No.	Name	Type	Description
1	$\overline{\text{XTAL}}$	output	The inverted output of the on-chip oscillator.
2	XTAL/CLOCK	input	The input to the on-chip oscillator, for external Xtal circuit or clock.
3	SERIAL CLOCK	input	The C-BUS serial clock input. This clock, produced by the µC, is used for transfer timing of commands and data to and from the device. See Figure 4
4	COMMAND DATA	input	The C-BUS serial data input from the µC. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the SERIAL CLOCK. See Figure 4
5	REPLY DATA	output	The C-BUS serial data output to the µC. The transmission of REPLY DATA bytes is synchronized to the SERIAL CLOCK under the control of the $\overline{\text{CS}}$ input. This tri-state output is held at high impedance when not sending data to the µC. See Figure 4
6	$\overline{\text{CS}}$	input	The C-BUS data loading control function: this input is provided by the µC. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Figure 4.
7	$\overline{\text{IRQ}}$	output	This output indicates an interrupt condition to the µC by going to a logic 0. This is a wire-ORable output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µC. This pin has a low impedance pulldown to logic 0 when active and a high-impedance when inactive. An external pullup resistor is required. The conditions that cause interrupts are indicated in the IRQ FLAG register and are effective if not masked out by a corresponding bit in the IRQ MASK register.
8	N/C		*No internal connection. Do not make any connection to these pin*
9	N/C		No internal connection. Do not make any connection to these pin
10	A/D CAP	output	An internal reference voltage for the A to D, decoupled to V_{SS} by an external capacitor.
11	N/C		No internal connection. Do not make any connection to this pin.
12	V_{SS}	power	Negative supply (ground).
13	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$. This pin must be bypassed by a capacitor mounted close to the device pins.
14	RX AMP IN	input	The inverting input to the Rx input amplifier.
15	RX AMP OUT	output	The output of the Rx input amplifier and the input to the audio filter section.
16	RX AUDIO OUT	output	Output of the Rx audio filter section.
17	N/C		No internal connection. Do not make any connection to this pin.
18	SUM IN	input	Input to the audio summing amplifier.
19	SUM OUT	output	Output of the audio summing amplifier, internally tied to input of MOD2
20	MOD1 IN	input	Input to MOD1 audio gain control.
21	TX SUB AUDIO OUT	output	Output of the CTCSS tone generator.
22	MOD1	output	Output of MOD1 audio gain control.
23	MOD2	output	Output of MOD2 audio gain control.
24	V_{DD}	power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.

3. External Components

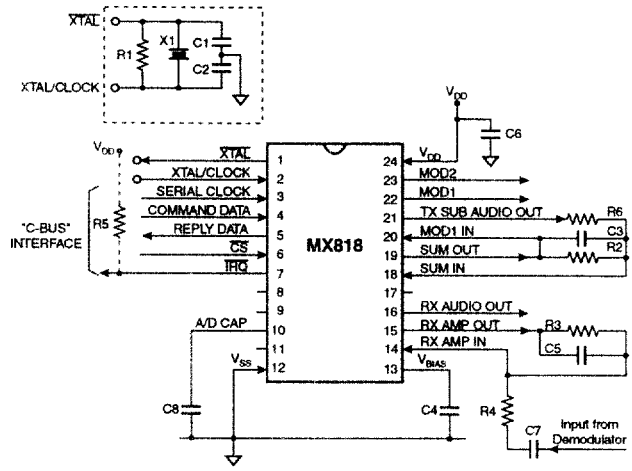


Figure 2: Recommended External Components

R1		1MΩ	±5%	C3	Note 2	100pF	±20%
R2	Note 2	100kΩ	±10%	C4		0.1µF	±20%
R3	Note 3	100kΩ	±10%	C5	Note 3	100pF	±20%
R4	Note 3, 4		±10%	C6		0.1µF	±20%
R5		22kΩ	±10%	C7	Note 3, 4		±20%
R6	Note 2		±10%	C8		0.1µF	±20%
C1		22pF	±20%				
C2		22pF	±20%	X1	Note 1	4.032MHz	±100ppm

Table 1: Recommended External Components

Recommended External Components Notes:

1. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
2. R2, R6 and C3 form the gain components for the Summing Amplifier. R6 should be chosen as required from the system specification, using the following formula:

   $$\text{Tx Sub Audio Gain} = -\frac{R2}{R6}$$

3. R3, R4, C5 and C7 form the gain components for the Rx Input Amplifier. R4 should be chosen as required by the signal level, using the following formula:

   $$\text{Gain} = -\frac{R3}{R4}$$

4. C7 x R4 should be chosen so as not to compromise the low frequency performance of this product.

4. General Description

The MX818 is a programmable CTCSS sub-audio encoder/decoder for use in land mobile radio equipment.

The receiver section of the MX818 has a fast/predictive tone detector which operates in parallel with a tone decoder. The latter decodes a user-programmable set of up to 15 tones and performs a more accurate (but slower) analysis of the tones detected by the fast/predictive tone detector, which is a single detector that is switchable to provide either a fast response to any CTCSS tone (FAST DETECT mode) or a fast response to a single user-programmed CTCSS tone (PREDICTIVE mode).

The high pass audio filter is designed to filter out the CTCSS sub-audio tones. The summing and modulation amplifiers allow the audio modulation to be controlled digitally via the C-BUS. A general purpose timer is included.

Each function, and the routing of signals, is flexible and may be configured or controlled by the user's software.

4.1 Software Description

4.1.1 Command Summary

The following table contains a brief description of all valid Commands. Details follow below.

				DATA BYTE(S)	
REGISTER NAME	**SECTION**	**HEX ADDRESS COMMAND**	**READ / WRITE**	**BYTE 1**	**BYTE 2**
General Reset	4.1.3.1	$01	W	none	none
Sub-Audio Control	4.1.3.2	$80	W	Refer to Bit Description	none
Sub-Audio Status	4.1.4, 4.1.5.1	$81	R	Refer to Bit Description	none
Sub-Audio Set-Up	4.1.3.3	$82	W	Refer to Bit Description	none
CTCSS TX/ Fast RX Frequency	4.1.3.7	$83	W	Specify Tx or Fast Rx Frequency per command $80 & $83 Bit descriptions	
CTCSS RX Program	4.1.3.8	$84	W	1 of 15 possible Register Select & Decode Frequencies	
General Control	4.1.3.4	$88	W	Refer to Bit Description	none
Audio Control	4.1.3.9	$8A	W	Mod 1 Attenuation	Mod 2 Attenuation
General Purpose Timer	4.1.3.5	$8B	W	Refer to Bit Description	none
IRQ Mask	4.1.3.6	$8E	W	Refer to Bit Description	none
IRQ Flag	4.1.4, 4.1.5.2	$8F	R	Refer to Bit Description	none

Table 2: Command Summary

4.1.2 Address/Commands

Instructions and data are transferred, via C-BUS, in accordance with the timing information provided in Figure 4.

Instruction and data transactions to and from the MX818 consist of an Address/Command (A/C) byte followed by either:

a. further instruction or data (0,1, or 2 bytes)
b. status or Rx data reply (1 byte)

4.1.2.1 8-bit Write Only Registers

HEX ADDRESS COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$01	GENERAL RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$80	SUB-AUDIO CONTROL	CTCSS TX ENABLE	CTCSS DECODE RX ENABLE	CTCSS FAST DETECT ENABLE	0	0	0	0	0
$82	SUB-AUDIO SET-UP	CTCSS DECODER BANDWIDTH MSB BIT 3	BIT 2	BIT 1	LSB BIT 0	FAST CTCSS MODE DETECT/ PREDICTIVE	0	0	0
$88	GENERAL CONTROL	AUDIO BAND-PASS FILTER BPF ENABLE	BPF UN-MUTE	BPF 6dB PAD	0	0	0	TIMER ENABLE	TIMER RE-CYCLE
$8B	GENERAL PURPOSE TIMER	GENERAL PURPOSE TIMER (GPT) MSB BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$8E	IRQ MASK	0	GPT IRQ MASK	0	0	CTCSS IRQ MASK	CTCSS FAST IRQ MASK	0	0

Table 3: 8-bit Write Only Register

4.1.2.2 16-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$83	CTCSS TX/ FAST RX FREQUENCY (1)	CTCSS (TX) NOTONE	0	0	CTCSS TX / FAST RX FREQUENCY MSB BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
	CTCSS TX/ FAST RX FREQUENCY (2)	CTCSS TX / FAST RX FREQUENCY BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$84	CTCSS RX PROGRAM (1)	CTCSS TONE ADDRESS MSB BIT 3	BIT 2	BIT 1	LSB BIT 0	CTCSS FREQUENCY MSB BIT 11	BIT 10	BIT 9	BIT 8
	CTCSS RX PROGRAM (2)	CTCSS FREQUENCY BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$8A	AUDIO CONTROL (1)	0	0	MOD 1 ENABLE	MOD 1 MSB BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
	AUDIO CONTROL (2)	0	0	MOD 2 ENABLE	MOD 2 MSB BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0

Table 4: 16-bit Write Only Registers

4.1.3 Write Only Register Description

4.1.3.1 GENERAL RESET (Hex address $01)

The reset command has no data attached to it. It sets the device registers into the specific (all powersaved) states as listed below:

REGISTER NAME	HEX ADDRESS	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
SUB-AUDIO CONTROL	$80	0	0	0	0	0	0	0	0
SUB-AUDIO STATUS	$81	0	0	0	0	X	X	X	X
SUB-AUDIO SET-UP	$82	0	0	0	0	0	0	0	0
CTCSS TX / FAST RX FREQUENCY (1)	$83	0	0	0	0	0	0	0	0
CTCSS TX / FAST RX FREQUENCY (2)		0	0	0	0	0	0	0	0
CTCSS RX PROGRAM (1)	$84	0	0	0	0	0	0	0	0
CTCSS RX PROGRAM (2)		0	0	0	0	0	0	0	0
GENERAL CONTROL	$88	0	0	0	0	0	0	0	0
AUDIO CONTROL (1)	$8A	0	0	0	0	0	0	0	0
AUDIO CONTROL (2)		0	0	0	0	0	0	0	0
GENERAL PURPOSE TIMER	$8B	0	0	0	0	0	0	0	0
IRQ MASK	$8E	0	0	0	0	0	0	0	0
IRQ FLAG	$8F	0	0	0	0	0	0	0	0

X = undefined

Table 5: General Reset (Hex Address $01)

4.1.3.2 SUB-AUDIO CONTROL Register (Hex address $80)

This register is used to control the functions of the device as described below:

CTCSS TX ENABLE and DECODER ENABLE (Bits 7 and 6)	Bit 7 and Bit 6 enable and disable the CTCSS decoder (Rx) or transmitter (Tx) according to Table 7. See Note 1
CTCSS FAST DETECT ENABLE (Bit 5)	When bit 5 is set to 1, the FAST CTCSS DETECT or FAST CTCSS PREDICTIVE mode is enabled, depending upon the setting of FAST CTCSS MODE (Bit 3 SUB-AUDIO SET-UP Register, $82). When this bit is 0, both FAST CTCSS DETECT and FAST CTCSS PREDICTIVE tone detectors are disabled. See Note 2
(Bits 4, 3, 2, 1 and 0)	Reserved for future use. These bits should be set to 0.

Table 6: Sub-Audio Control Register (Hex Address $80)

Tx Bit 7	Rx Bit 6	Function
0	0	Tx disabled, Rx disabled
0	1	Tx disabled, Rx enabled
1	0	Tx enabled, Rx disabled
1	1	Tx enabled, Rx enabled

Table 7: CTCSS Tx Enable and Decoder Enable

Notes:

1. Bit 7 should be set to 0 if CTCSS FAST DETECT ENABLE (Bit 5 SUB-AUDIO CONTROL Register, $80) is set to 1.
2. Bit 5 should be set to 0 if CTCSS TX ENABLE (Bit 7 SUB-AUDIO CONTROL Register, $80) is set to 1.

4.1.3.3 SUB-AUDIO SET-UP Register (Hex address $82)

This register is used to define the CTCSS parameters, as described below:

CTCSS DECODER BANDWIDTH (Bits 7, 6, 5 and 4)	These four bits set the bandwidth of the CTCSS tone decoder according to Table 9
FAST CTCSS MODE (Bit 3)	When CTCSS FAST DETECT ENABLE (Bit 5 SUB-AUDIO CONTROL Register, $80) is 1, this bit selects the FAST CTCSS DETECT or the FAST CTCSS PREDICTIVE mode, according to Table 10.
(Bits 2, 1 and 0)	Reserved for future use. These bits should be set to 0.

Table 8: Sub-Audio Set-up Register (Hex Address $82)

				BANDWIDTH	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Will Decode**	**Will Not Decode**
1	0	0	0	±1.1%	±2.4%
1	0	0	1	±1.3%	±2.7%
1	0	1	0	±1.6%	±2.9%
1	0	1	1	±1.8%	±3.2%
1	1	0	0	±2.0%	±3.5%
1	1	0	1	±2.2%	±3.7%
1	1	1	0	±2.5%	±4.0%
1	1	1	1	±2.7%	±4.2%

Table 9: CTCSS Decoder Bandwidth

DETECT/PREDICTIVE Bit 3	FUNCTION
0	DETECT mode
1	PREDICTIVE mode

If the CTCSS FAST DETECT ENABLE bit is 0 then both modes are deselected.

Table 10: Fast CTCSS Mode

4.1.3.4 GENERAL CONTROL Register (Hex address $88)

This register is used to control the functions of the device as described below

BPF ENABLE (Bit 7)	When this bit is 1 the audio band-pass filter is enabled. When this bit is 0 the audio band-pass filter is disabled (powersaved).
BPF UN-MUTE (Bit 6)	When this bit is 1 the audio band-pass filter output is switched to the RX AUDIO OUT pin. When this bit is 0 the output of the filter is disconnected from RX AUDIO OUT, which is then in a high impedance state. This control, along with BPF ENABLE, allows the filter to power up and settle internally before switching the output on, to avoid clicks when coming out of powersave.
BPF 6dB PAD (Bit 5)	When this bit is 1 a 6dB attenuator is inserted into the output of the audio band-pass filter. When this bit is 0 the output of the audio band-pass filter is not attenuated.
(Bits 4, 3 and 2)	Reserved for future use. These bits should be set to 0.
TIMER ENABLE (Bit 1)	When this bit goes to a 1 the general purpose timer is restarted and its internal register is re-loaded from the value specified in the GENERAL PURPOSE TIMER Register (Hex address $8B). It will then count down from the count held in its internal register. When this bit is 0 the count down is disabled and the last pre-programmed value is retained in the timer's internal register.
TIMER RE-CYCLE (Bit 0)	When this bit is 1 the general purpose timer will re-load its internal register from the value specified in the GENERAL PURPOSE TIMER Register (Hex Address $8B) when the count in the internal register reaches zero (i.e. the timeout has expired). It then restarts the count down, so that the timer continuously cycles. When this bit is 0 the general purpose timer will stop when the count in the internal register reaches zero (i.e. the timeout has expired). The timer can only be restarted by reloading a value into the GENERAL PURPOSE TIMER Register (Hex address $8B). If this bit is switched from 1 to 0 while the timer is enabled then the timer will complete the present count before stopping.

Table 11: General Control Register (Hex Address $88)

4.1.3.5 GENERAL PURPOSE TIMER (GPT) Register (Hex address $8B)

This register is used to preset the value of a countdown timer. Once a binary value has been loaded into this register, it will be automatically transferred to an internal register within the timer. This internal register is then decremented at each count interval (0.95ms) until it reaches zero. On reaching zero, the GPT IRQ FLAG in the IRQ FLAG Register (Hex address $8F) is set to 1. An interrupt is generated on the $\overline{IRQ}$ pin if the GPT IRQ MASK in the IRQ MASK Register (Hex address $8E) is 1 otherwise the GPT IRQ FLAG remains set to 1 and no interrupt is generated.

When the internal register has reached a count of zero, the action of the timer depends on the setting of the TIMER RE-CYCLE bit in the GENERAL CONTROL Register (Hex address $88). If the TIMER RE-CYCLE bit is 1 then the timer will re-load the countdown value from the GENERAL PURPOSE TIMER Register and restart the countdown from this value. If the TIME RE-CYCLE bit is 0 then the timer will stop and no further action or timer interrupts will take place until the GENERAL PURPOSE TIMER Register is re-loaded. Loading the GENERAL PURPOSE TIMER with 0 will cause the timer circuitry to be disabled (i.e. powersaved).

4.1.3.6 IRQ MASK Register (Hex address $8E)

This register is used to control the interrupts (IRQs) as described below:

(Bits 7, 5, 4, 1 and 0)	Reserved for future use. These bits should be set to 0.
GPT IRQ MASK (Bit 6)	When bit 6 is set to 1 it enables an interrupt that occurs when GPT IRQ FLAG (Bit 6, IRQ FLAG Register, $8F) changes from 0 to 1. When this bit is 0 the interrupt is masked.
CTCSS IRQ MASK (Bit 3)	When bit is set to 1 it enables an interrupt that occurs when CTCSS IRQ FLAG (Bit 3, IRQ FLAG Register, $8F) changes from 0 to 1. When this bit is 0 the interrupt is masked.
CTCSS FAST IRQ MASK (Bit 2)	When this bit is set to 1 it enables an interrupt that occurs when CTCSS FAST IRQ FLAG (Bit 2, IRQ FLAG Register, $8F) changes from 0 to 1. When this bit is 0 the interrupt is masked.

Table 12: IRQ MASK Register (Hex address $8E)

4.1.3.7 CTCSS TX/FAST RX FREQUENCY Register (Hex address $83)

This is a 16-bit register. Byte (1) is sent first. When the CTCSS fast detector is enabled, bits 0 - 12 defines the receive frequency the fast predictive detector is looking for, according to the formula below:

$$A = \frac{f_{XTAL}\ (Hz)}{16 \times f_{TONE}\ (Hz)}$$

where A is the binary number programmed into the 13 bits.

When the CTCSS transmitter is enabled, bits 0 - 12 control the frequency of the transmitted CTCSS tones, according to the formula above.

When the fast detector and the transmitter are both enabled, bits 0-12 define the receive frequency which the fast predictive detector is looking for and the frequency of the transmitted tone according to the formula above: (i.e. Tx tone = predictive tone).

When Bit 7 (in the first 8 bits) is set to 1, the tone output is set at V_{BIAS} or NOTONE without regard to the number (A) programmed. When Bit 7 is 0 the programmed tone is set on the output. Programming the bits 0 - 12 to 0 puts the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the Tx and the FAST DETECT.

4.1.3.8 CTCSS RX PROGRAM Register (Hex address $84)

This is a 16-bit register. Byte (1) is sent first. Byte 1 and Byte 2 are used to program the center frequencies of up to 15 tones in the sub-audio band that will be decoded by the receiver.

Each tone is identified by its address in bits 7, 6, 5 and 4 of byte (1). The remaining 12 bits contain the data representing the tone frequency according to the formula below. If a tone is not required the 12 bits should be set to zero.

Byte 1								Byte 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	<---------- N ---------->				<---------- R ---------->							
0	0	0	1												
0	0	1	0												
0	0	1	1												
0	1	0	0												
0	1	0	1	N is the binary representation of the				R is the nearest 6-bit binary							
0	1	1	0	following decimal number (n):				representation of (r), where:							
0	1	1	1												
1	0	0	0	$n = INT(948982 \times f_{TONE} / f_{XTAL})$				$r = \{[237245/f_{XTAL}] - [n/(4 \times f_{TONE})]\} \times 8400$							
1	0	0	1												
1	0	1	0												
1	0	1	1												
1	1	0	0												
1	1	0	1												
1	1	1	0												

Table 13: CTCSS RX PROGRAM Register (Hex address $84)

Example: To program 100Hz when using the recommended 4.032MHz Xtal.

$$n = INT(948982 \times 100 / 4.032 \times 10^6)$$
$$= INT(23.536) = 23$$
$$N = 010111 \text{ (binary)}$$

$$r = \{[237245 / 4.032 \times 10^6] - [23 / (4 \times 100)]\} \times 8400$$
$$= 11.26$$
$$R = 11 \text{ (rounding up if exactly halfway)}$$
$$= 001011 \text{ (binary)}$$

This generates the 12-bit code of 010111001011

The Hex address represented by bits 7, 6, 5 and 4 in byte (1) is used as the code to indicate which tone has been decoded. This code appears in bits 3, 2, 1 and 0 of the SUB-AUDIO STATUS Register (Hex address $81). The 15 programmed tones use Hex addresses $0 - $E.

4.1.3.9 AUDIO CONTROL Register (Hex address $8A)

This is a 16-bit register. Byte (1) is sent first. The six least significant bits of the first byte in this register are used to set the attenuation of the Modulator 1 amplifier and the six least significant bits of the second byte in this register are used to set the attenuation of the Modulator 2 amplifier, according to the tables below:

BYTE 1						
5	4	3	2	1	0	Mod. 1 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB
1	0	0	0	0	1	12.0dB
1	0	0	0	1	0	11.6dB
1	0	0	0	1	1	11.2dB
1	0	0	1	0	0	10.8dB
1	0	0	1	0	1	10.4dB
1	0	0	1	1	0	10.0dB
1	0	0	1	1	1	9.6dB
1	0	1	0	0	0	9.2dB
1	0	1	0	0	1	8.8dB
1	0	1	0	1	0	8.4dB
1	0	1	0	1	1	8.0dB
1	0	1	1	0	0	7.6dB
1	0	1	1	0	1	7.2dB
1	0	1	1	1	0	6.8dB
1	0	1	1	1	1	6.4dB
1	1	0	0	0	0	6.0dB
1	1	0	0	0	1	5.6dB
1	1	0	0	1	0	5.2dB
1	1	0	0	1	1	4.8dB
1	1	0	1	0	0	4.4dB
1	1	0	1	0	1	4.0dB
1	1	0	1	1	0	3.6dB
1	1	0	1	1	1	3.2dB
1	1	1	0	0	0	2.8dB
1	1	1	0	0	1	2.4dB
1	1	1	0	1	0	2.0dB
1	1	1	0	1	1	1.6dB
1	1	1	1	0	0	1.2dB
1	1	1	1	0	1	0.8dB
1	1	1	1	1	0	0.4dB
1	1	1	1	1	1	0dB

BYTE 2						
5	4	3	2	1	0	Mod. 2 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB
1	0	0	0	0	1	6.0dB
1	0	0	0	1	0	5.8dB
1	0	0	0	1	1	5.6dB
1	0	0	1	0	0	5.4dB
1	0	0	1	0	1	5.2dB
1	0	0	1	1	0	5.0dB
1	0	0	1	1	1	4.8dB
1	0	1	0	0	0	4.6dB
1	0	1	0	0	1	4.4dB
1	0	1	0	1	0	4.2dB
1	0	1	0	1	1	4.0dB
1	0	1	1	0	0	3.8dB
1	0	1	1	0	1	3.6dB
1	0	1	1	1	0	3.4dB
1	0	1	1	1	1	3.2dB
1	1	0	0	0	0	3.0dB
1	1	0	0	0	1	2.8dB
1	1	0	0	1	0	2.6dB
1	1	0	0	1	1	2.4dB
1	1	0	1	0	0	2.2dB
1	1	0	1	0	1	2.0dB
1	1	0	1	1	0	1.8dB
1	1	0	1	1	1	1.6dB
1	1	1	0	0	0	1.4dB
1	1	1	0	0	1	1.2dB
1	1	1	0	1	0	1.0dB
1	1	1	0	1	1	0.8dB
1	1	1	1	0	0	0.6dB
1	1	1	1	0	1	0.4dB
1	1	1	1	1	0	0.2dB
1	1	1	1	1	1	0dB

X = don't care

MOD1 ENABLE (Bit 5, first byte)	When this bit is 1 the MOD1 attenuator is enabled. When this bit is 0 the MOD1 attenuator is disabled (i.e. powersaved).
MOD2 ENABLE (Bit 5, second byte)	When this bit is 1 the MOD2 attenuator and the SUMMER AMP are enabled. When this bit is 0 they are both disabled (i.e. powersaved).
(Bits 7 and 6, first and second bytes)	Reserved for future use. These should be set to 0

Table 14: AUDIO CONTROL Register (Hex address $8A)

4.1.4 8-bit Read Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
						CTCSS RX TONE			
$81	SUB-AUDIO STATUS	0	CTCSS FAST TONE	0	TONE DECODE	MSB BIT 3	BIT 2	BIT 1	LSB BIT 0
$8F	IRQ FLAG	0	GP TIMER IRQ FLAG	0	0	CTCSS IRQ FLAG	CTCSS FAST IRQ FLAG	0	0

4.1.5 Read Only Register Description

4.1.5.1 SUB-AUDIO STATUS Register (Hex address $81)

This register is used to indicate the status of the device as described below:

(Bit 7)	Reserved for future use. This will be set to 0 and should be ignored by user's software.
CTCSS FAST TONE (Bit 6)	When Bit 5 in the SUB-AUDIO CONTROL Register and Bit 3 in the SUB-AUDIO SET-UP Register are set to enable FAST CTCSS DETECT mode, this bit will be set to 1 if a periodic tone is detected. If no periodic tone is detected this bit will be set to 0. When Bit 5 in the SUB-AUDIO CONTROL Register and Bit 3 in the SUB-AUDIO SET-UP Register are set to enable FAST CTCSS PREDICTIVE mode, this bit will be set to 1 if a periodic tone that matches the frequency programmed in the CTCSS TX/FAST RX Register is detected. If no match is found this bit will be set to 0 When Bit 5 in the SUB-AUDIO CONTROL Register is set to 0 this bit will be a 0.
(Bit 5)	Reserved for future use. This will be set to 0 and should be ignored by the user's software.
TONE DECODE (Bits 4)	This bit indicates the status of the tone decoder. A 1 indicates a tone has been detected (TONE DECODE). A 0 indicates the loss of the tone (NOTONE). TONE DECODE means that a tone has been decoded and its characteristics are defined by the bandwidth (See SUB-AUDIO SET-UP Register bits 7, 6, 5 and 4) and the CTCSS RX TONE number (See SUB-AUDIO STATUS Register bits 3, 2, 1 and 0). When Bit 6 in the SUB-AUDIO CONTROL Register is set to 0 the TONE DECODE bit 4 will be set to 0. Identification of a valid tone which is not in the pre-programmed list of up to 15 tones will cause the decoder to move to the TONE DECODE state with the RX TONE address of 1111 in bits 3, 2, 1 and 0; indicating a valid, but unrecognized, tone. Loss of tone will cause the NOTONE timer to be started. If loss of tone continues for the duration of the time-out period, then the decoder will move to NOTONE state and the identification of pre-programmed tones will start again.
CTCSS RX TONE (Bits 3, 2, 1 and 0)	These four bits hold a Hex number from $0 to $F. Numbers $0 to $E represent the address of the CTCSS tone decoded according to the tones programmed in the CTCSS RX PROGRAM Register, $84. The Hex number $F indicates the presence of any tone that is not described by CTCSS DECODER BANDWIDTH (Bits 7, 6, 5 and 4, SUB-AUDIO SET-UP Register, $82) and CTCSS FREQUENCY (Bits 11 - 0, CTCSS RX PROGRAM Register, $84).

Table 15: SUB-AUDIO STATUS Register (Hex address $81)

4.1.5.2 IRQ FLAG Register (Hex address $8F)

This register is used to indicate when the device requires attention as indicated below.

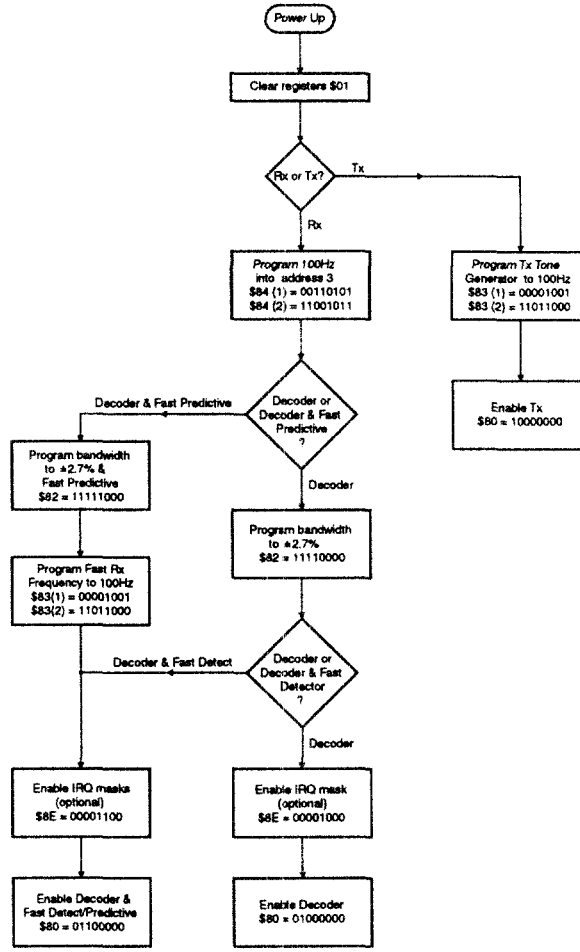
(Bits 7, 5, 4, 1 and 0)	Reserved for future use. These will be set to 0 and should be ignored by user's software.
GPT IRQ FLAG (Bit 6)	When the general purpose timer has reached zero in its internal register, this bit will be set to 1 to indicate the timeout has expired. This bit is cleared to 0 by a read of the IRQ FLAG Register (Hex address $8F).
CTCSS IRQ FLAG (Bit 3)	When CTCSS RX DECODE (Bit 4, SUB-AUDIO STATUS Register, $81) changes state this bit will be set to 1. This bit is cleared to 0 by a read of the IRQ FLAG Register (Hex address $8F).
CTCSS FAST IRQ FLAG (Bit 2)	When CTCSS FAST TONE (Bit 6, SUB-AUDIO STATUS Register, $81) changes state this bit will be set to 1. This bit is cleared to 0 by a read of the IRQ FLAG Register (Hex address $8F).

Table 16: IRQ FLAG Register (Hex address $8F)

The flow chart shows the following modes of operation for the example below:

1. Decode)
2. Decode and Fast Detect) e.g. Address 3 = 100Hz, bandwidth = ±2.7%, interrupt enabled
3. Decode & Fast Predictive)
4. Transmit, e.g. Tx = 100Hz

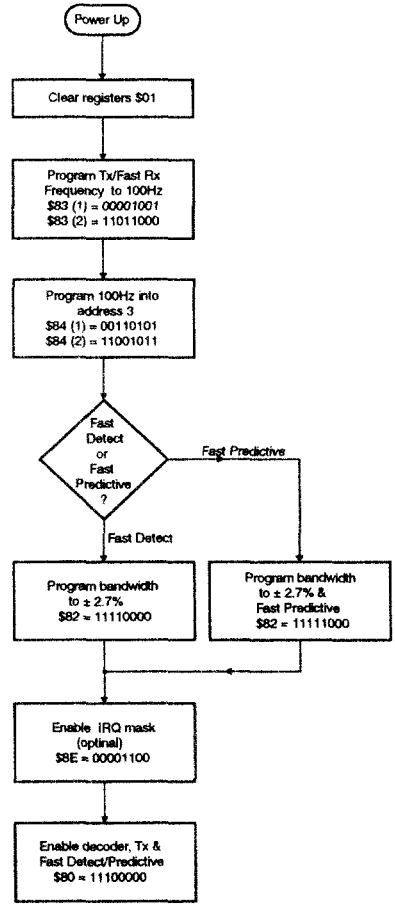
Note: $8X is the Hex address/command.



The flow chart shows the decoder, fast detect/fast predictive and transmitter enabled with the following example.

1. Tx tone generator = 100Hz
2. Decoder programmed with 100Hz in address 3
3. Bandwidth setting = ±2.7%
4. Interrupt enabled

Note: $8X is the Hex address/command.



5. Application

5.1 General

The MX818 is intended for use in radio systems where sub-audio signaling is required for functions such as trunking control, selective calling or group calling.

The CTCSS fast/predictive detector is useful for the detection of occupied channels indicating either the presence of any sub-audio tone, or range of tones, depending if it is set in fast detect or predictive mode. This will increase the efficiency of scanning and trunking systems, reducing the average time allocated to assessing each channel.

The facility to decode any of up to 15 programmed tones allows the use of tones for various signaling functions such as masking a free channel or identifying sub groups within a user's groups.

Adjustable decoder bandwidths permits certainty and signal to noise performance to be traded when congestion or range, limits the system performance.

5.2 Transmitter

The transmitter is enabled with Bit 7 in the SUB-AUDIO CONTROL register ($80).

The Tx frequency is set using Bit 0 to Bit 12 in the CTCSS TX/FAST RX register ($83) using the formula below:

$$A = \frac{f_{XTAL}\ (Hz)}{16 \times f_{TONE}\ (Hz)}$$

where A is the binary number programmed into the 13 bits.

When Bit 7 (in the first 8 bits) is set to 1 the tone output is set at V_{BIAS} or NOTONE without regard to the number (A) programmed. When Bit 7 is 0 the programmed tone is set on the output. Programming the bits 0 to 12 to 0 puts the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the Tx and the FAST DETECT (Bits 7 and 5 in the SUB-AUDIO CONTROL register $80).

5.3 Receiver (Decode)

The CTCSS Receiver (Decoder) should first be set up according to the desired characteristics. This entails setting the CTCSS decoder bandwidth in the SUB-AUDIO SET-UP register ($82), also programming the center frequencies of the desired tones in the CTCSS RX PROGRAM register ($84). (It can hold up to 15 different tones). Any tone can be in any location. During operation when the device is receiving, the tones are scanned in the sequence of their location, i.e. $0 first and $E last and once a tone is detected the remaining tones are not checked. Therefore if two tones are close enough in frequency for their bandwidths to overlap then the one in the lowest location will be detected.

The CTCSS IRQ MASK in the IRQ MASK register ($8E) should also be set as required.

The CTCSS DECODER ENABLE in the SUB-AUDIO CONTROL register ($80) should then be set to 1. While in the Decode mode the FAST DETECT may be enabled (see below).

When the receiver detects a change in its present state an IRQ will be generated and Bit 3 of the IRQ FLAG register ($8F) will indicate this.

The change that occurred can be read from Bit 4 of the SUB-AUDIO STATUS register ($81) and if a tone is indicated by this bit then the number of that tone can be read from Bits 3, 2, 1 and 0 of the same register.

5.4 Receiver (Fast Detect)

This is used for detecting, in the fastest possible time, that sub-audio tones are present on the Rx channel. Response time is optimized for speed at the expense of frequency resolution.

It is enabled using Bit 5 of the SUB-AUDIO CONTROL register ($80). It has an IRQ which may be unmasked with Bit 2 of the IRQ MASK register ($8E). The FAST CTCSS MODE DETECT/PREDICTIVE Bit 3 in the SUB-AUDIO SET UP register ($82) allows for one of two alternatives in the FAST mode. In DETECT mode it will detect any periodic tone in the sub-audio band and when in PREDICTIVE mode it will detect specific tones determined by the frequency set in the CTCSS TX/FAST RX register ($83) and the fixed PREDICTIVE mode bandwidth. Successful detection is indicated by the CTCSS FAST IRQ FLAG Bit 2 in the IRQ FLAG register ($8F), and the CTCSS FAST TONE Bit 6 in the SUB-AUDIO STATUS register ($81).

5.5 General Purpose Timer (GPT)

This may be used in conjunction with the Rx Decoder to form part of the decode algorithm or as a timer for any other purpose. It has an 8-bit value register GENERAL PURPOSE TIMER register ($8B) set in units of 1.0ms, an IRQ FLAG Bit 6 of the IRQ FLAG register ($8F) and an IRQ MASK Bit 6 IRQ MASK register ($8E).

5.6 Tx / Fast Rx Tone Table

The following table lists the commonly used CTCSS tones and the corresponding values for programming the transmitter frequency / fast predictive frequency register (Hex address $83).

Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
67.0	E	B1	**114.8**	8	93	**186.2**	5	49
69.3	E	34	**118.8**	8	49	**189.9**	5	2F
71.9	D	B1	**123.0**	8	1	**192.8**	5	1B
74.4	D	3B	**127.3**	7	BC	**196.6**	5	2
77.0	C	C9	**131.8**	7	78	**199.5**	4	EF
79.7	C	5A	**136.5**	7	36	**203.5**	4	D6
82.5	B	EF	**141.3**	6	F7	**206.5**	4	C4
85.4	B	87	**146.2**	6	BC	**210.7**	4	AC
88.5	B	1F	**151.4**	6	80	**218.1**	4	83
91.5	A	C2	**156.7**	6	48	**225.7**	4	5D
94.8	A	62	**159.8**	6	29	**229.1**	4	4C
97.4	A	1B	**162.2**	6	12	**233.6**	4	37
100.0	9	D8	**167.9**	5	DD	**241.8**	4	12
103.5	9	83	**173.8**	5	AA	**250.3**	3	EF
107.2	9	2F	**179.9**	5	79	**254.1**	3	E0
110.9	8	E0	**183.5**	5	5D			

Table 17: Tx / Fast Rx Tone Table

5.7 Rx Program Tone Table

The following table lists the commonly used CTCSS tones together with the values for programming the "CTCSS RX PROGRAM" register (Hex address $84).

Note: The values for byte 1 and 2 below apply to tone address 0 only. These values will vary depending on the location they are programmed into.

Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
67.0	3	D8	**114.8**	6	C0	**186.2**	A	C9
69.3	4	9	**118.8**	6	D1	**189.9**	B	8
71.9	4	1B	**123.0**	7	10	**192.8**	B	44
74.4	4	4E	**127.3**	7	50	**196.6**	B	83
77.0	4	83	**131.8**	7	C0	**199.5**	B	8A
79.7	4	94	**136.5**	8	2	**203.5**	B	C9
82.5	4	CB	**141.3**	8	44	**206.5**	C	6
85.4	5	2	**146.2**	8	86	**210.7**	C	46
88.5	5	14	**151.4**	8	C9	**218.1**	C	C3
91.5	5	4C	**156.7**	9	C	**225.7**	D	41
94.8	5	87	**159.8**	9	48	**229.1**	D	48
97.4	5	94	**162.2**	9	82	**233.6**	D	89
100.0	5	CB	**167.9**	9	C6	**241.8**	E	8
103.5	6	7	**173.8**	A	B	**250.3**	E	88
107.2	6	45	**179.9**	A	84	**254.1**	E	C7
110.9	6	82	**183.5**	A	C2			

Table 18: Rx Program Tone Table

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW / P Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
DS Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency		4.0315968	4.0324032	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
Xtal Frequency = 4.032MHz
Audio Level 0dB ref. = 308mVrms at 1kHz
V_{DD} = 3.3V to 5.0V, T_{AMB} = 25°C, T_{OP} = -45°C to 85°C.
Composite Signal = 308mV_{RMS} at 1kHz + 75mV_{RMS} Noise + 31mV_{RMS} Sub-Audio Signal
Noise Bandwidth = 5kHz Band Limited Gaussian

		Note	Min.	Typ.	Max.	Units
DC Parameters						
I_{DD}						
All Powersaved						
V_{DD} = 5.0V		1, 2		0.6	1.0	mA
V_{DD} = 3.3V		2		0.35	0.6	mA
Tx/Rx Operating						
V_{DD} = 5.0V		1, 2		3.5	6.0	mA
V_{DD} = 3.3V		2		1.6	2.5	mA
C-BUS Interface						
Input Logic 1			70%			V_{DD}
Input Logic 0					30%	V_{DD}
Input Leakage Current (Logic 1 or 0)			-1.0		1.0	µA
Input Capacitance					7.5	pF
Output Logic 1 (I_{OH} = 120µA)			90%			V_{DD}
Output Logic 0 (I_{OL} = 360µA)					10%	V_{DD}
Off State Leakage Current (V_{OUT} = V_{DD})		6			10	µA
AC Parameters						
CTCSS Decoder						
Sensitivity	(Pure CTCSS Tone)	5		-26.0		dB
Response Time	(Composite Signal)			140		ms
De-Response Time	(Composite Signal)			145		ms
Frequency Range			60		253	Hz
CTCSS Detector - Fast Detect						
Sensitivity	(Pure CTCSS Tone)	5		-26.0		dB
Response Time	(Composite Signal)			56.0		ms
Frequncy Range			60		253	Hz
CTCSS Detector - Fast Predictive						
Sensitivity	(Pure CTCSS Tone)	5		-26.0		dB
Response Time	(Composite Signal)	7		37.0		ms
Frequemcy Range			60		253	Hz
Decode Bandwidth				40		Hz
CTCSS Encoder						
Frequency Range			60		253	Hz
Tone Frequency Resolution					0.3	%
Tone Amplitude Tolerance		1	-1.0	0	1.0	dB
Total Harmonic Distortion		9		2.0		%

Audio Band-Pass Filter						
Passband		8	300		3000	Hz
Passband Gain	(at 1.0kHz)	8		0		dB
Passband Ripple	(wrt gain at 1.0kHz)	8	-2		0.5	dB
Stopband Attenuation		8	33.0			dB
Residual Hum and Noise				-50.0		dBp
Alias Frequency				63		kHz
Output Impedance						
TX SUB-AUDIO OUT	(Enabled)			2.0		kΩ
RX AUDIO OUT	(Disabled)			500		kΩ
Rx Amp and Summing Amp						
Open Loop Gain	(input = 1mV at 100Hz)			70.0		dB
Unity Gain Bandwidth				5.0		MHz
Input Impedance	(at 100Hz)		10			MΩ
Output Impedance	(Open Loop)			6.0		kΩ
Transmitter Modulator Drives:						
Mod.1 Attenuator						
Attenuation (at 0dB)			-0.2	0	0.2	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)			-1.0		1.0	dB
Output Impedance		3		600		Ω
Input Impedance	(at 100Hz)			15.0		kΩ
Mod.2 Attenuator						
Attenuation (at 0dB)			-0.2	0	0.2	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)			-0.6		0.6	dB
Output Impedance		3		600		Ω
General Purpose Timer						
Timing Period Range			1.0		242	ms
Count Interval				0.95		ms
Xtal/Clock Input						
Pulse Width ('High' or 'Low')		4	40.0			ns
Input Impedance (at 100Hz)			10.0			MΩ
Gain (input = $1mV_{RMS}$ at 100Hz)			20.0			dB

Operating Characteristics Notes:

1. At V_{DD} = 5.0V only. Signal levels or currents are proportional to V_{DD}.
2. Not including any current drawn from the device by external circuitry.
3. Small signal impedance.
4. Timing for an external input to the XTAL/CLOCK pin.
5. With input gain components set as recommended in Figure 2.
6. $\overline{IRQ}$ pin.
7. From one tone to another tone.
8. See filter response (Figure 3).
9. Measured at MOD1 or MOD2 output.

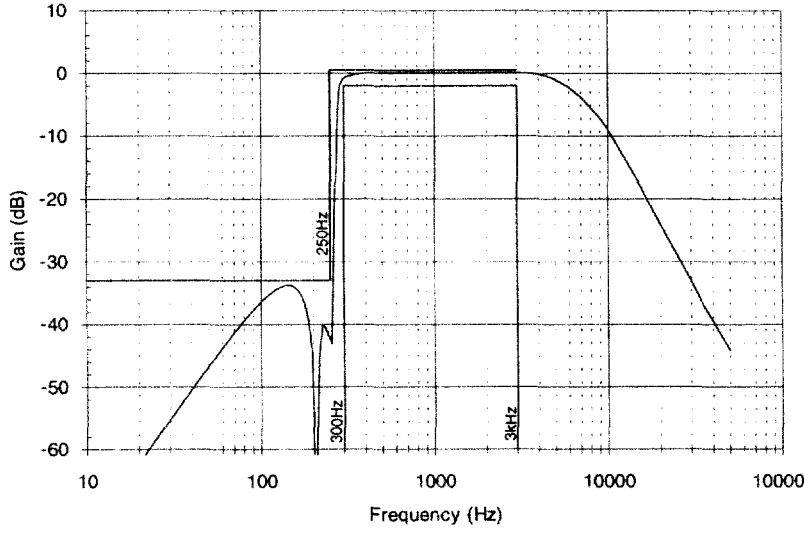


Figure 3: Audio Band-Pass Filter Frequency Response

6.1.4 Timing Diagrams

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz, V_{DD} = 5.0V, T_{AMB} = 25°C.

Parameter		Min.	Typ.	Max.	Units
t_{CSE}	CS-Enable to Clock-High	2.0			µs
t_{CSH}	Last Clock-High to CS-High	4.0			µs
t_{HIZ}	CS-High to Reply Output 3-state			2.0	µs
t_{CSOFF}	CS-High Time between transactions	2.0			µs
t_{NXT}	Inter-Byte Time	4.0			µs
t_{CK}	Clock-Cycle time	2.0			µs

Timing Diagrams Notes

1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into and out of the peripheral on the rising SERIAL CLOCK edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with either polarity SERIAL CLOCK pulses.

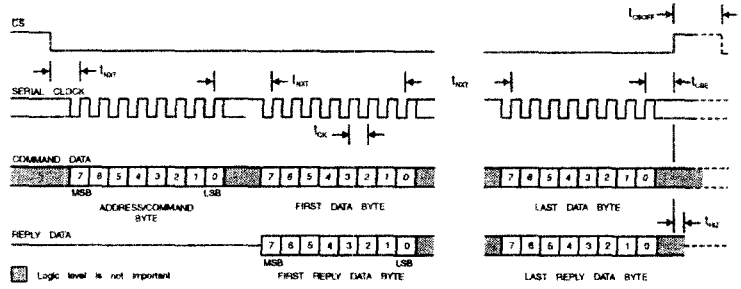
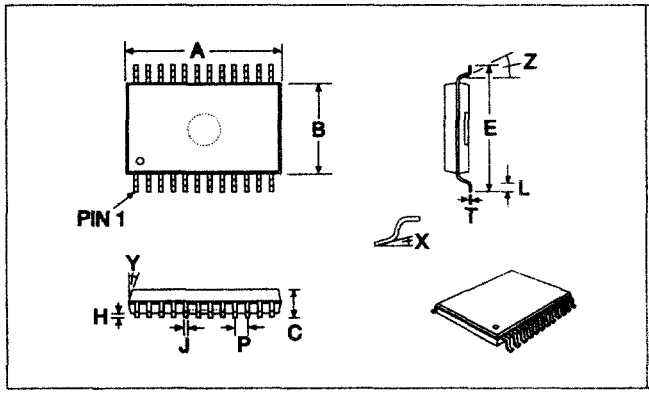


Figure 4: C-BUS Timing

6.2 Packaging

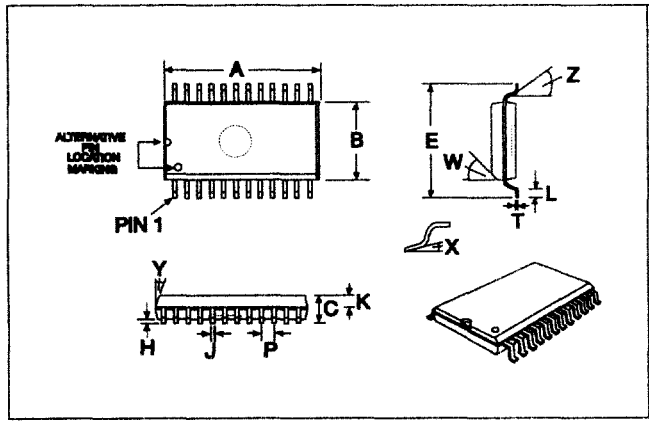


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 24-pin SSOP Mechanical Outline: *Order as part no. MX818DS*

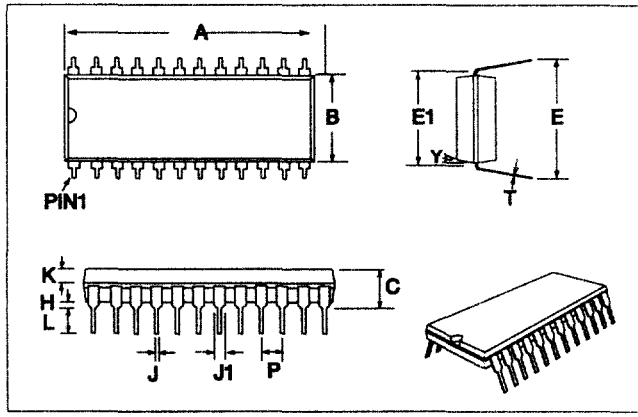


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin SOIC Mechanical Outline: *Order as part no. MX818DW*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 24-pin PDIP Mechanical Outline: ***Order as part no. MX818P***