TC518128AP/ASP/AF/AFW-80/10/12
TC518128APL/ASPL/AFL/AFWL-80/10/12
TC518128AFTL-80/10/12

SILICON GATE CMOS

131,072 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518128A is a 1M bit high speed CMOS pseudo static RAM organized as 131,072 words by 8 bits. The TC518128A utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518128A operates from a single 5V power supply. Refreshing is supported by a refresh ($\overline{RFSH}$) input which enables two types of refreshing - auto refresh and self refresh. The TC518128A features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC518128A is pin-compatible with the 1M bit CMOS static RAM JEDEC standard and is available in a 32-pin, 0.6 inch and 0.3 inch width plastic DIP, a small outline plastic flat package, and a 32-pin thin small outline plastic package (forward type).

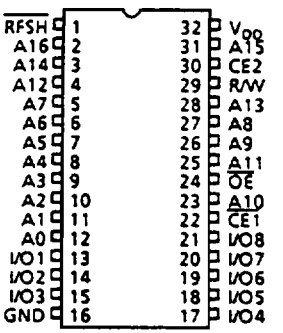
Features

- Organization: 131,072 words x 8 bits
- Single 5V power supply
- Fast access time

	TC518128A Family		
	-80	-10	-12
t_{CEA} CE Access Time	80ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time	35ns	40ns	50ns
t_{RC} Cycle Time	130ns	160ns	190ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	1mA/200μA (L version)		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 512 refresh cycles/8ms
- Auto refresh power down feature
- Pin compatible: 1M SRAM (JEDEC)
- Package
  - TC518128AP/APL : DIP32-P-600
  - TC518128AF/AFL : SOP32-P-450
  - TC518128ASP/ASPL : DIP32-P-300
  - TC518128AFW/AFWL : SOP32-P-525
  - TC518128AFTL : TSOP32-P-0820

Pin Connection (Top View)



TC518128APL / AFL / ASPL / AFWL

TC518128AFTL (Forward)

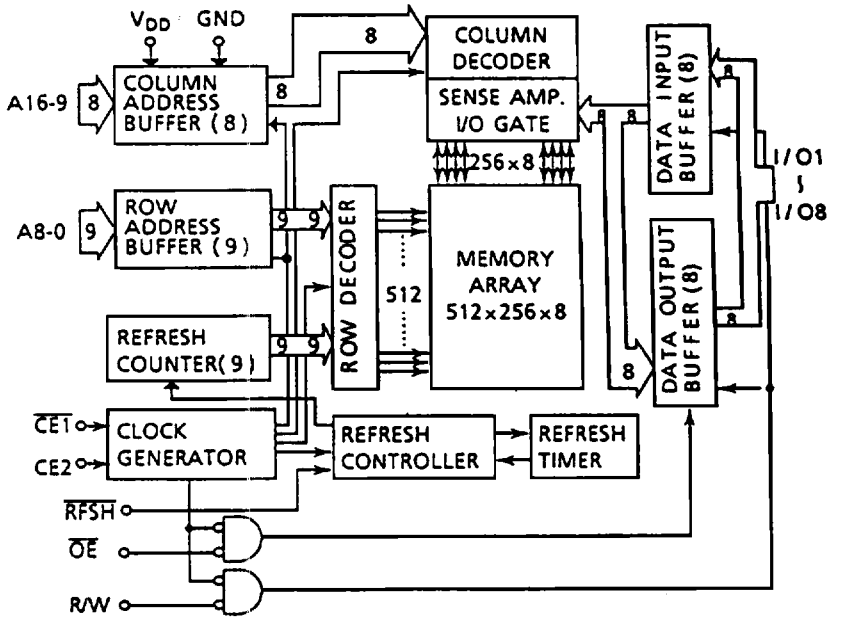
Pin Names

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

(TSOP)

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A_{11}	A_9	A_8	A_{13}	R/W	CE2	A_{15}	V_{DD}	$\overline{RFSH}$	A_{16}	A_{14}	A_{12}	A_7	A_6	A_5	A_4
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A_3	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A_{10}	$\overline{OE}$

Block Diagram



Operating Mode

MODE \ PIN	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O1 ~ 8
Read	L	H	L	H	*	V*	OUT
Write	L	H	*	L	*	V*	IN
CE only Refresh	L	H	H	H	*	V*	HZ
Auto/Self Refresh	H	*	*	*	L	*	HZ
Auto/Self Refresh	*	L	*	*	L	*	HZ
Standby	H	*	*	*	H	*	HZ
Standby	*	L	*	*	H	*	HZ

H = High level input (V_{IH})
L = Low level input (V_{IL})
* = V_{IH} or V_{IL}
V* = At the falling edge of $\overline{CE1}$ (CE2 = H) or the rising edge of CE2 ($\overline{CE1}$ = L), all address inputs are latched. At all other times, the address inputs are "*".
HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	V_{DD} + 1.0	V	
V_{IL}	Input Low Voltage	-1.0	–	0.8	V	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) $\overline{CE1}$, CE2, Address cycling: t_{RC} = t_{RC} min.	80ns version	–	50	70	mA	3,4
		100ns version	–	40	60		
		120ns version	–	35	50		
I_{DDS1}	Standby Current $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} $\overline{RFSH}$ = V_{IH}	Normal version	–	–	2	mA	
		L version	–	–	1		
I_{DDS2}	Standby Current $\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V, $\overline{RFSH}$ = V_{DD} - 0.2V	Normal version	–	–	1	mA	
		L version	–	100	200	µA	
I_{DDF1}	Self Refresh Current (Average) $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} $\overline{RFSH}$ = V_{IL}	Normal version	–	–	2	mA	
		L version	–	–	1		
I_{DDF2}	Self Refresh Current (Average) $\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V, $\overline{RFSH}$ = 0.2V	Normal version	–	–	1	mA	
		L version	–	100	200	µA	
I_{DDF3}	Auto Refresh Current (Average) $\overline{RFSH}$ cycling: t_{FC} = t_{FC} min		–	–	2	mA	
I_{DDF4}	CE only Refresh Current (Average) $\overline{CE1}$, CE2, Address cycling: t_{RC} = t_{RC} min.	80ns version	–	50	70	mA	3
		100ns version	–	40	60		
		120ns version	–	35	50		
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ V_{DD}, All other Inputs not under test = 0V		–	–	±10	µA	
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or R/W = V_{IL}), 0V ≤ V_{OUT} ≤ V_{DD}		–	–	±10	µA	
V_{OH}	Output High Level I_{OH} = -5mA		2.4	–	–	V	
V_{OL}	Output Low Level I_{OL} = 4.2mA		–	–	0.4	V	

Note: For I_{DDS1} and I_{DDF1} with $\overline{CE1}$ = V_{IH} (CE2 = V_{IL}), the specified limits are guaranteed under the condition CE2 = V_{IH} or CE2 = V_{IL} ($\overline{CE1}$ = V_{IH} or $\overline{CE1}$ = V_{IL}).
For I_{DDS2} and I_{DDF2} with $\overline{CE1}$ ≥ V_{DD} - 0.2V (CE2 ≤ 0.2V), the specified limits are guaranteed under the condition CE2 ≥ V_{DD} - 0.2V or CE2 ≤ 0.2V ($\overline{CE1}$ ≥ V_{DD} - 0.2V or $\overline{CE1}$ ≤ 0.2V).

Capacitance* (V_{DD} = 5V, Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE1}$, CE2, $\overline{OE}$, R/W, $\overline{RFSH}$)	–	7	
C_{IO}	Input/Output Capacitance	–	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	–	160	–	190	–	ns	
t_{RMW}	Read Modify Write Cycle Time	195	–	235	–	280	–		
t_{CE}	CE Pulse Width	80	10,000	100	10,000	120	10,000		13
t_P	CE Precharge Time	40	–	50	–	60	–		
t_{CEA}	CE Access Time	–	80	–	100	–	120		
t_{OEA}	$\overline{OE}$ Access Time	–	35	–	40	–	50		
t_{CLZ}	CE to Output in Low -Z	30	–	30	–	30	–		
t_{OLZ}	$\overline{OE}$ to Output in Low -Z	0	–	0	–	0	–		
t_{WLZ}	Output Active from End of Write	0	–	0	–	0	–		
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35		9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35		9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35		9
t_{ODS}	$\overline{OE}$ Output Disable Setup Time	0	–	0	–	0	–		
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	–	10	–	10	–		
t_{RCS}	Read Command Setup Time	0	–	0	–	0	–		
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–		
t_{WP}	Write Pulse Width	60	–	70	–	85	–		
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000		
t_{CWL}	Write Command to CE Lead Time	60	10,000	70	10,000	85	10,000		
t_{DSW}	Data Setup Time from R/W	30	–	35	–	45	–		10
t_{DSC}	Data Setup Time from CE	30	–	35	–	45	–		10
t_{DHW}	Data Hold Time from R/W	0	–	0	–	0	–		10
t_{DHC}	Data Hold Time from CE	0	–	0	–	0	–		10
t_{ASC}	Address Setup Time	0	–	0	–	0	–		11
t_{AHC}	Address Hold Time	20	–	25	–	30	–		11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	–	15	–	15	–		
t_{FC}	Auto Refresh Cycle Time	130	–	160	–	190	–		
t_{RFD}	$\overline{RFSH}$ Delay Time from CE	40	–	50	–	60	–		
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000		12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–		12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–		12
t_{FRS}	CE Delay Time from $\overline{RFSH}$ (Self Refresh)	160	–	190	–	225	–		12
t_{REF}	Refresh Period (512 cycles, A0 ~ A8)	–	8	–	8	–	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	
t_{CES}	CE2 Low Setup Time	5	–	5	–	5	–	ns	14
t_{CEH}	CE2 Low Hold Time	5	–	5	–	5	–	ns	14

Notes:

1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.

2) All voltages are referenced to GND.

3) I_{DDO} and I_{DDF4} depend on the cycle time.

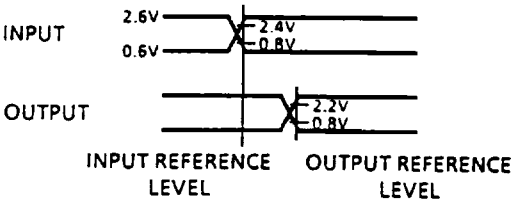
4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.

5) An initial pause of 100μs with high $\overline{CE1}$ or low CE2 is required after power-up before proper device operation is achieved.

6) AC measurements assume t_T = 5ns.

7) Timing reference levels

Input Levels	:	V_{IH} = 2.6V V_{IL} = 0.6V
Input Reference Levels	:	V_{IH} = 2.4V V_{IL} = 0.8V
Output Reference Levels	:	V_{OH} = 2.2V V_{OL} = 0.8V



8) Measured with a load equivalent to 2 TTL loads and 100pF.

9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10) For write cycles, the input data is latched at the earlier of R/W or $\overline{CE1}$ rising edge (CE2 falling edge). Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).

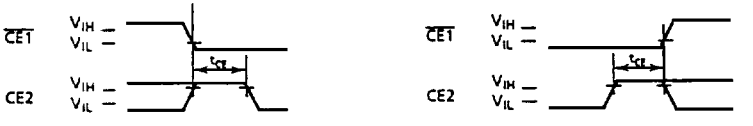
11) All address inputs are latched at the falling edge of $\overline{CE1}$ (rising edge of CE2). Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC}.

12) The two refresh operations, auto refresh and self refresh, are defined by the $\overline{RFSH}$ pulse width under the condition $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}.

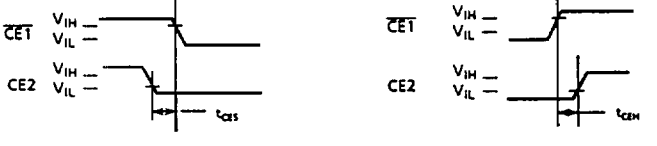
Auto refresh : $\overline{RFSH}$ pulse width ≤ t_{FAP} (max.)
Self refresh : $\overline{RFSH}$ pulse width ≥ t_{FAS} (min.)

The timing parameter t_{FRS} must be met for proper device operation under the following conditions:
- after self refresh
- if $\overline{RFSH}$ = "L" after power-up

13) The timings, t_{CE} (min.) and t_{CE} (max.) must be met for proper device operation.

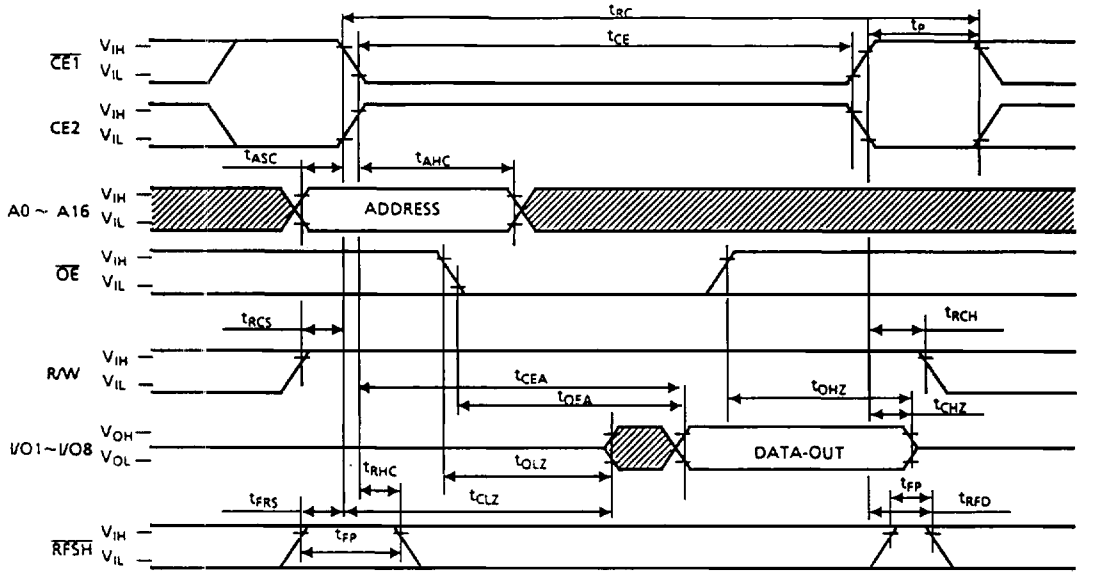


14) The timings, t_{CES} (min.) and t_{CEH} (min.) must be met when using $\overline{CE1}$ and CE2 as shown below.

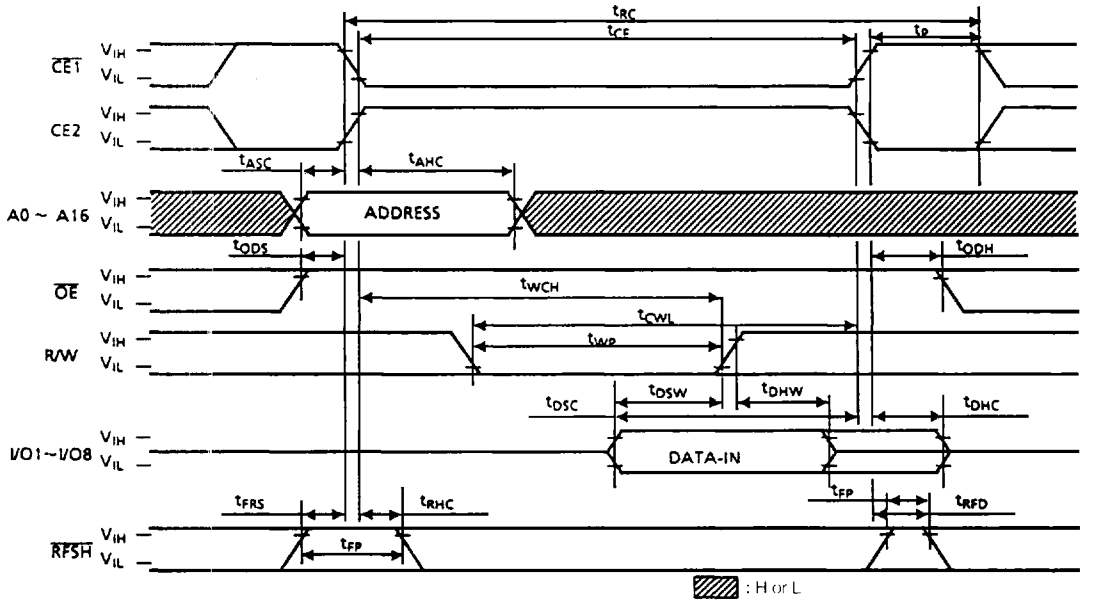


Timing Waveforms

Read Cycle

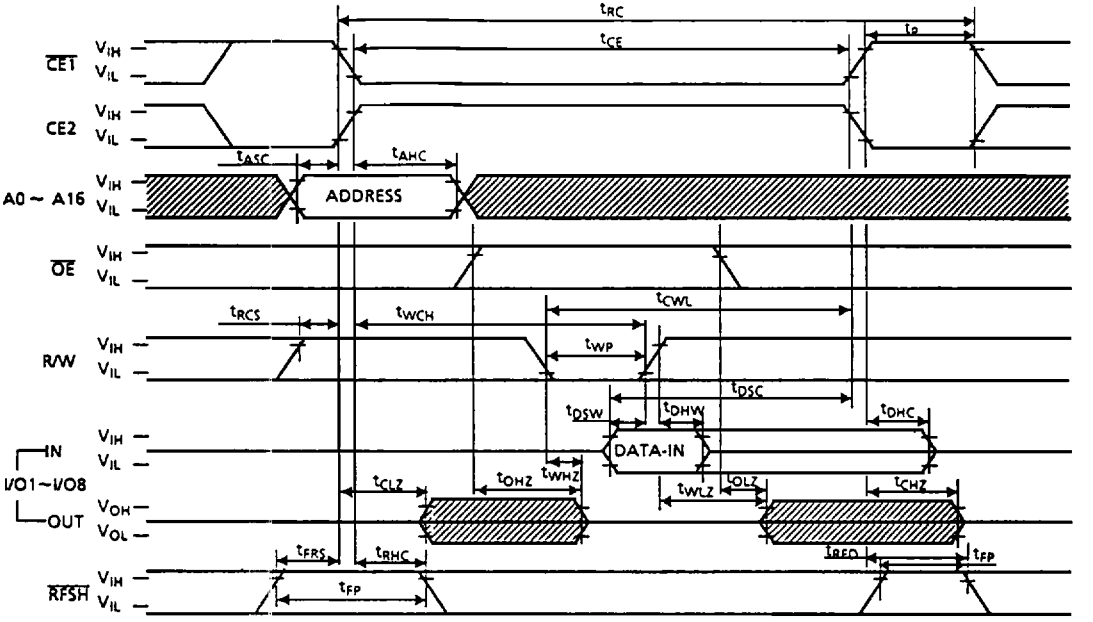


Write Cycle 1 ($\overline{OE}$ Fixed High)

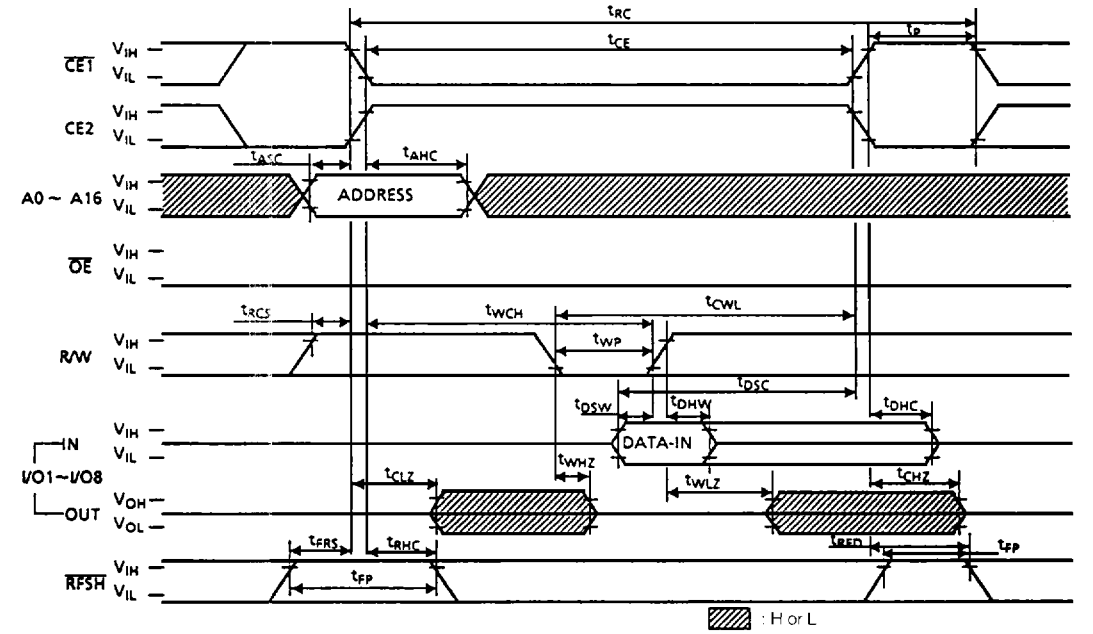


Note: The device can be operated by cycling $\overline{CE1}$ (or CE2) only provided that CE2 (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

Write Cycle 2 ($\overline{OE}$ Clocked)

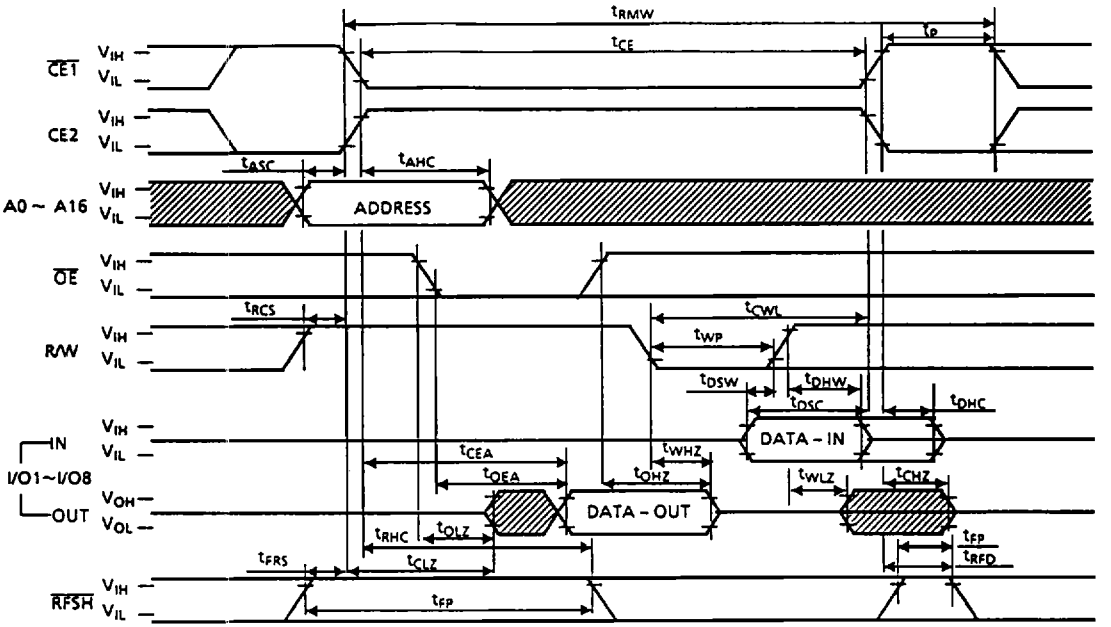


Write Cycle 3 ($\overline{OE}$ Fixed Low)

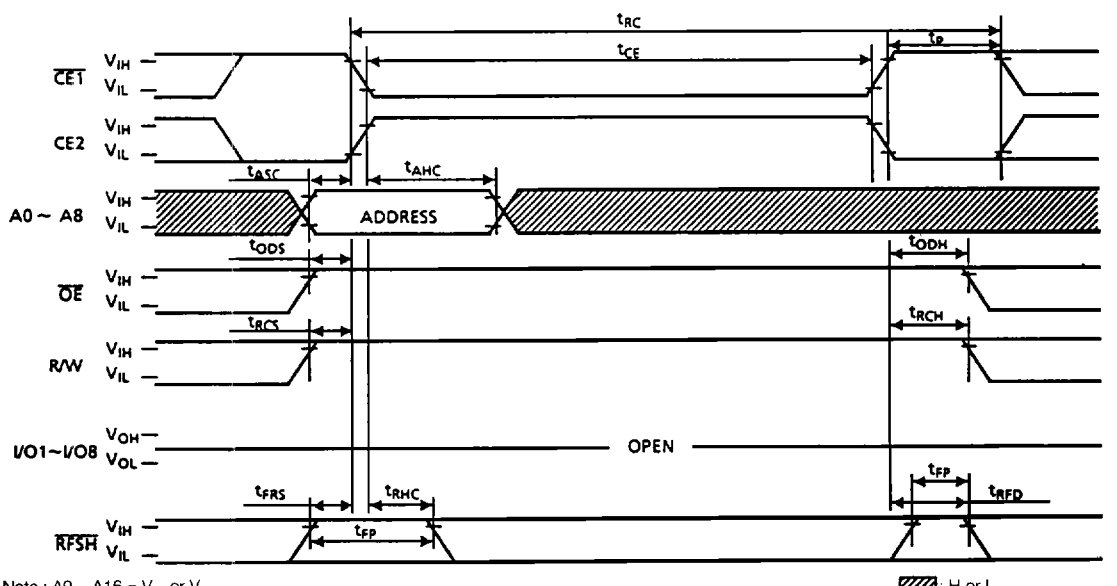


Note: The device can be operated by cycling $\overline{CE1}$ (or CE2) only provided that CE2 (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

Read Modify Write Cycle



CE Only Refresh

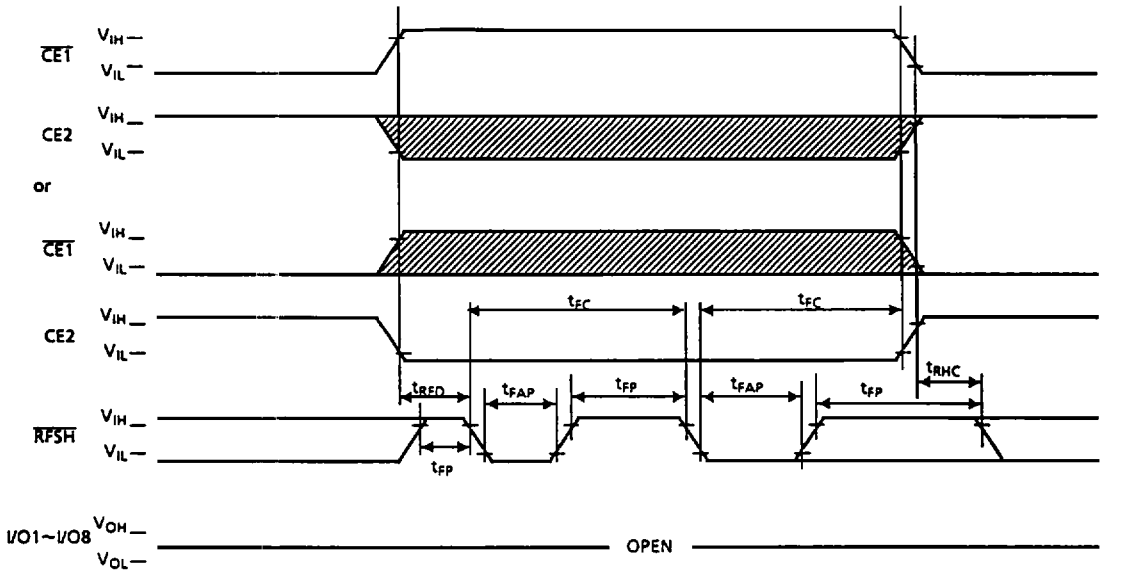


Note : A9 ~ A16 = V_{IH} or V_{IL}

▨ : H or L

Note: The device can be operated by cycling $\overline{CE1}$ (or CE2) only provided that CE2 (or $\overline{CE1}$) is connected to V_{IH} (or V_{IL}).

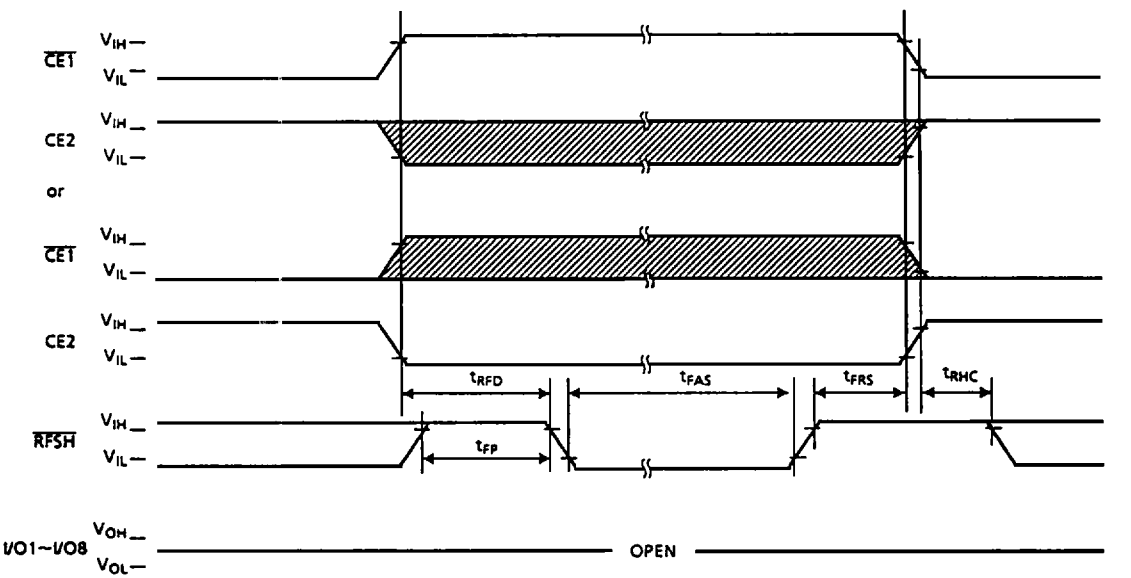
Auto Refresh



Note : $\overline{OE}$, R/W, A0 ~ A16 = V_{IH} or V_{IL}

: H or L

Self Refresh



Note : $\overline{OE}$, R/W, A0 ~ A16 = V_{IH} or V_{IL}

: H or L