TENTATIVE

TOSHIBA CCD LINEAR IMAGE SENSOR CCD(Charge Coupled Device)

TCD1501C

The TCD1501C which includes sample-and-hold circuit is a high sensitive and low dark current 5000 elements CCD image sensor.

The sensor is designed for facsimile, imagescanner and OCR.

The device contains a row of 5000 elements photodiodes which provide a 16 lines/mm (400DPI) across a A3 size paper. The device is operated by 5V (pulse), and 12V power supply.

FEATURES

Number of Image Sensing Elements: 5000 elements

Image Sensing Element Size

: $7\mu m$ by $7\mu m$ on $7\mu m$ centers

Photo Sensing Region: High sensitive and low voltage

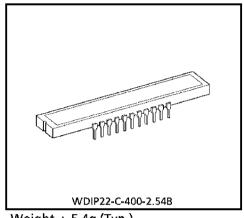
dark signal pn photodiode

Clock : 2 Phase (5V) Internal Circuit : S/H circuit : 22pin DIP Package

MAXIMUM RATINGS (Note 1)

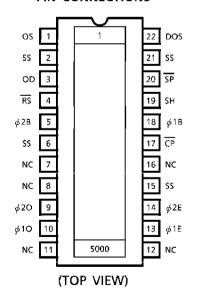
CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	Vø		>
Shift Pulse Voltage	VsH		
Reset Pulse Voltage	VRS	-0.3~8	
Clamp Pulse Voltage	VCP		
Sample and Hold Pulse Voltage	VSP		
Power Supply Voltage	V _{OD}	- 0.3~15	
Operating Temperature	Topr	- 25∼60	°C
Storage Temperature	T _{stg}	- 40~100	°C

All voltage are with respect to SS terminals (Note 1) (Ground).



Weight: 5.4g (Typ.)

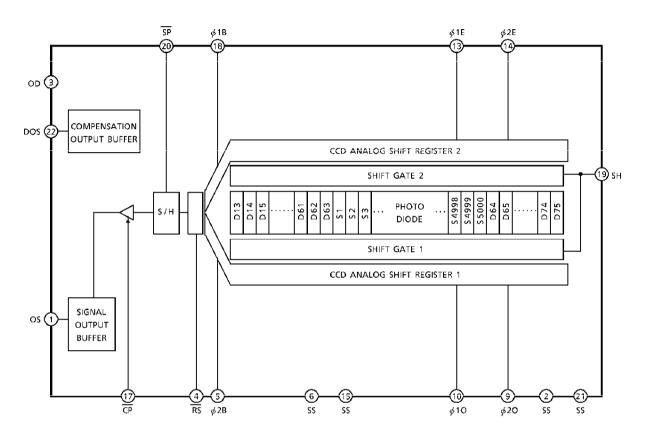
PIN CONNECTIONS



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CIRCUIT DIAGRAM



PIN NAME

φ1E, Ο	Clock (Phase 1)
φ2E, Ο	Clock (Phase 2)
φIB	Final Stage Clock (Phase 1)
ø2B	Final Stage Clock (Phase 2)
SH	Shift Gate
RS	Reset Gate
SP	Sample and Hold Gate
CP	Clamp Gate
OS	Signal Output
DOS	Compensation Output
QD	Power
SS	Ground
NC	Non Connection

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OPTICAL / ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{OD} = 12V, V_{ϕ} = $V_{\overline{RS}}$ = V_{SP} = $V_{\overline{CP}}$ = 5V, f_{ϕ} = 0.5MHz, f_{RS} = 1MHz, t_{INT} (INTEGRATION TIME) = 10ms, LIGHT SOURCE = DAYLIGHT FLUORESCENT LAMP, LOAD RESISTANCE = 100k Ω)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Sensitivity	R	10.4	13	15.6	V/lx·s	
BL 4 B N. H. H	PRNU	_	_	10	%	(Note 2)
Photo Response Non Uniformity	PRNU (3)	_	6	10	mV	(Note 9)
Register Imbalance	RI	_	_	3	%	(Note 3)
Saturation Output Voltage	VSAT	2	3	_	V	(Note 4)
Saturation Exposure	SE	0.13	0.23	_	lx·s	(Note 5)
Dark Signal Voltage	VDRK	_	1	2	mV	(Note 6)
Dark Signal Non Uniformity	DSNU	_	2	3	m۷	(Note 6)
DC Power Dissipation	PD	_	240	325	mW	
Total Transfer Efficiency	TTE	92	_	_	%	
Output Impedance	Zo	_	0.5	1	kΩ	
Dynamic Range	DR	_	3000	_	_	(Note 7)
DC Signal Output Voltage	Vos	4	5	6.5	V	(Note 8)
DC Compensation Output Voltage	V _{DOS}	4	5	6.5	V	(Note 8)
DC Differential Error Voltage	Vos-V _{DOS}	_	_	400	mV	

(Note 2) Measured at 50% of SE (Typ.)

Definition of PRNU : PRNU = $\frac{\Delta \chi}{\overline{\chi}} \times 100 \, (\%)$

Where \overline{x} is average of total signal output and Δx is the maximum deviation from \overline{x} under uniform illumination.

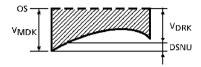
(Note 3) Measured at 50% of SE (Typ.) RI is defined as follows:

RI =
$$\frac{\frac{2 \times 1}{100} |x_{1} - x_{1} + 1|}{4999 \times x} \times 100 (\%)$$

Where χn and $\chi n + 1$ are signal output of each pixel. $\overline{\chi}$ is average of total signal output.

(Note 4) V_{SAT} is defined as minimum saturation output voltage of all effective pixels.

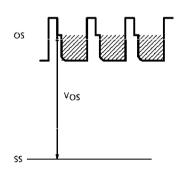
- (Note 5) Definition of SE : SE = $\frac{V_{SAT}}{R}$ (I x-s)
- (Note 6) V_{DRK} is defined as average dark signal voltage of all effective pixels. DSNU is defined as different voltage between V_{DRK} and V_{MDK} when V_{MDK} is maximum dark signal voltage.

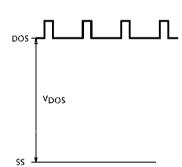


(Note 7) Definition of DR : DR = $\frac{V_{SAT}}{V_{DRK}}$

 $V_{\mbox{\footnotesize{DRK}}}$ is proportional to $t_{\mbox{\footnotesize{INT}}}$ (Integration Time). So the shorter $t_{\mbox{\footnotesize{INT}}}$ condition makes wider DR values.

(Note 8) DC signal output voltage and DC compensation output voltage are defined as follows:





(Note 9) PRUN (3) is defined as maximum voltage with next pixel, where measured 5% of SE (Typ.).

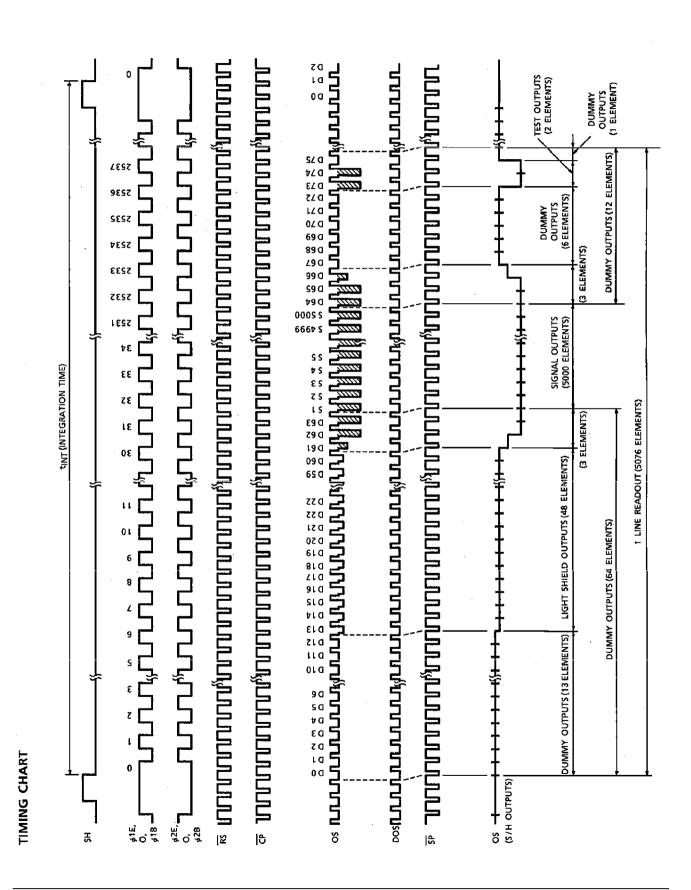
OPERATING CONDITION

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Voltage	"H" Level	Vø1E, O	4.5	5	5.5	V
	"L" Level	Vφ2Ε, Ο	0	_	0.5	V
Final Stage Clock Voltage	"H" Level	V ø 1B	4.5	5	5.5	V
	"L" Level	V <i>∲</i> 2B	0	_	0.5	V
Shift Pulse Voltage	"H" Level	V _{SH}	4.5	5	5.5	٧
	"L" Level		0	_	0.5	
Poset Bulsa Valtage	"H" Level	V _{RS}	4.5	5	5.5	V
Reset Pulse Voltage	"L" Level		۷RS	0	_	0.5
Claren Bules Valtare	"H" Level	V _{CP}	4.5	5	5.5	٧
Clamp Pulse Voltage	"L" Level		0		0.5	
Sample and Hold Pulse Voltage *	"H" Level	V _{SP}	4.5	5	5.5	٧
	"L" Level		0	_	0.5	
Power Supply Voltage		V _{OD}	11.4	12.0	13.0	٧

^{*} Supply "L" level to \$\overline{SP}\$ terminal when sample-and-hold circuitry is not used.

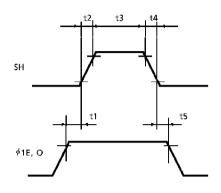
CLOCK CHARACTERISTICS (Ta = 25°C)

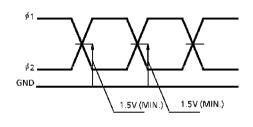
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Frequency	f¢	_	0.5	6.0	MHz
Reset Pulse Frequency	f RS	_	1.0	12.0	MHz
Sample and Hold Pulse Frequency	f <u>SP</u>	_	1.0	2.0	MHz
Clock Capacitance	CφE	_	350	450	рF
	CφO	_	350	450	
Final Stage Clock Capacitance	C∳B	_	10	20	pF
Shift Gate Capacitance	CSH	_	10	20	pF
Reset Gate Capacitance	CRS	_	10	20	рF
Clamp Gate Capacitance	CCÞ	_	10	20	pF
Sample and Hold Gate Capacitance	CSP	_	10	20	pF



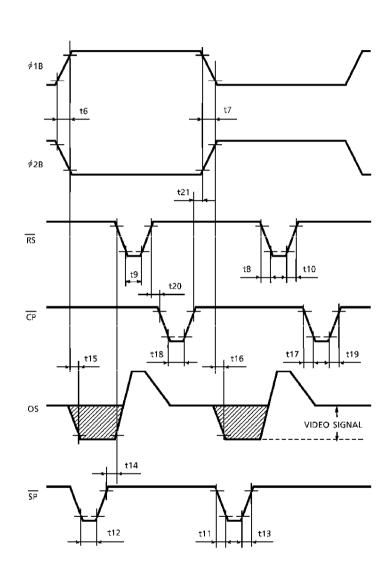
TIMING REQUIREMENTS

SH, ϕ 1 TIMING





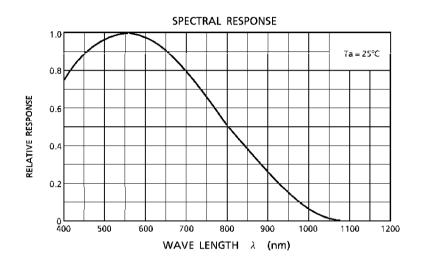
 ϕ 1, ϕ 2, \overline{RS} , \overline{CP} , OS, \overline{SP} TIMING



CHARACTERISTIC	SYMBOL	MIN.	TYP. (Note 10)	MAX.	UNIT
Pulse Timing of SH and	t1, t5	100	300	_	ns
SH Pulse Rise Time, Fall Time	t2, t4	0	50	_	ns
SH Pulse Width	t3	500	1000	_	ns
φ1, φ2 Pulse Rise Time, Fall Time	t6, t7	0	100	_	ns
RS Pulse Rise Time, Fall Time	t8, t10	0	20	_	ns
RS Pulse Width	t9	20	250	_	ns
SP Pulse Rise Time, Fall Time	t11, t13	0	20	_	ns
SP Pulse Width	t12	20	_	_	ns
Pulse Timing of SP and RS	t14	0	50	_	ns
Video Data Delay Time (Note 11)	t15, t16	_	30	_	ns
CP Pulse Rise Time, Fall Time	t17, t19	0	20	_	ns
CP Pulse Width	t18	20	_	_	ns
Pulse Timing of RS and CP	t20	0	_	_	ns
Pulse Timing of	t21	0	_	_	ns

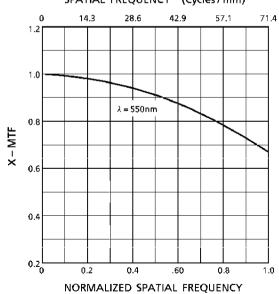
(Note 10) TYP. is the case of $f_{\mbox{RS}}$ = 1.0MHz (Note 11) Load Resistance is 100k Ω

TYPICAL PERFORMANCE CURVES



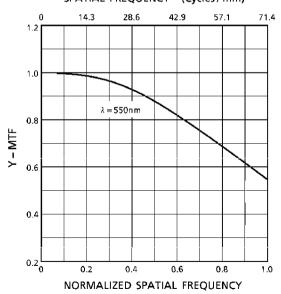


SPATIAL FREQUENCY (Cycles/mm)

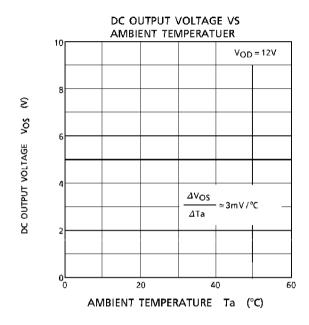


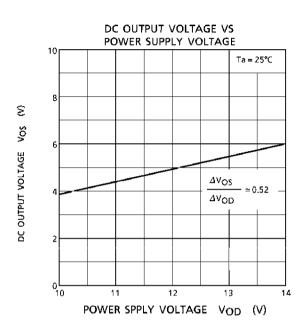
MODULATION TRANSFER FUNCTION OF Y-DIRECTION

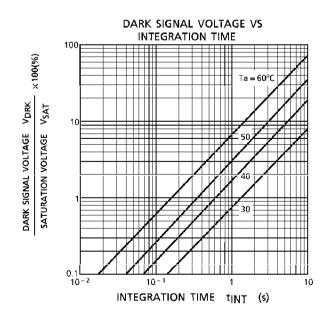
SPATIAL FREQUENCY (Cycles/mm)



TYPICAL PERFORMANCE CURVES (Cont'd)







CAUTION

1. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N₂.

Care should be taken to avoid mechanical or thermal shock because the glass window iseasily to damage.

2. Electrostatic Breakdown

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

3. Incident Light

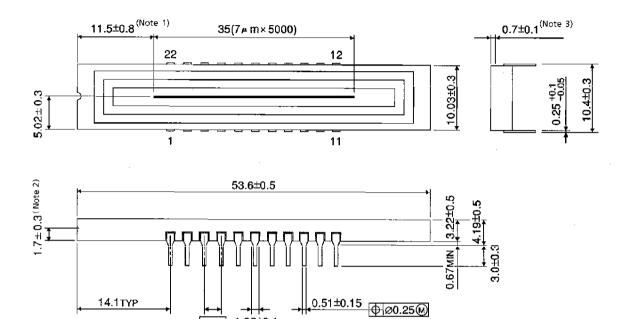
CCD sensor is sensitive to infrared light.

Note that infrared light component degrades resolution and PRNU of CCD sensor.

PACKAGE OUTLINE

WDIP22-C-400-2.54B (A)

Unit in mm



- (Note 1) No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.
- (Note 2) TOP OF CHIP TO BOTTOM OF PACKAGE.
- (Note 3) GLASS THICKNES (n = 1.5)

2.54 1.02±0.1

Weight: 5.4g (Typ.)

14.1TYP