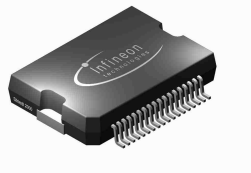
TLE 6288 R : Smart 6 Channel Peak&Hold Switch

Features

- **3 Channel high side with adjustable P&H current control**
- **3 Channel high / low side configurable**
- **Protection**
  - Over Current (current limitation)
  - Overtemperature
  - Overvoltage (active clamping)
- **Diagnosis**
  - Over Current
  - Over Temperature
  - Open Load (Off-State)
  - Short to Ground (Off-state, lowside configuration)
  - Short to Vbb (Off-state, highside configuration)
- **Interface and Control**
  - 16 Bit Serial Peripheral Interface *(2bit/CH)*
  - Device programming via SPI
  - Separate diagnosis output for each CH (DIAG1 – 6)
  - General Fault Flag + Overtemperature Flag
  - Direct parallel control of all channels
  - General enable signal to control all channels simultaneously
- Low Quiescent Current
- Compatible with 3.3V and 5V Microcontrollers
- **E**lecto**s**tatic **d**ischarge (ESD) protection of all pins

Product Summary

Supply voltage	V_S	4.5 – 5.5	V
On resistance	$R_{ON\ 1\text{-}6}$	0.15	Ω
Lowside clamping voltage	$V_{cll\ (max)}$	+55	V
Highside clamping voltage	$V_{clh\ (max)}$	-19	V
Peak current range	I_{pk}	1.2 - 3.6	A
Hold current range	I_{hd}	0.7 - 2	A
Peak time range	I_p	0 - 3.6	ms
Fixed off time range	I_{fo}	100 – 400	µs



P-DSO 36-12

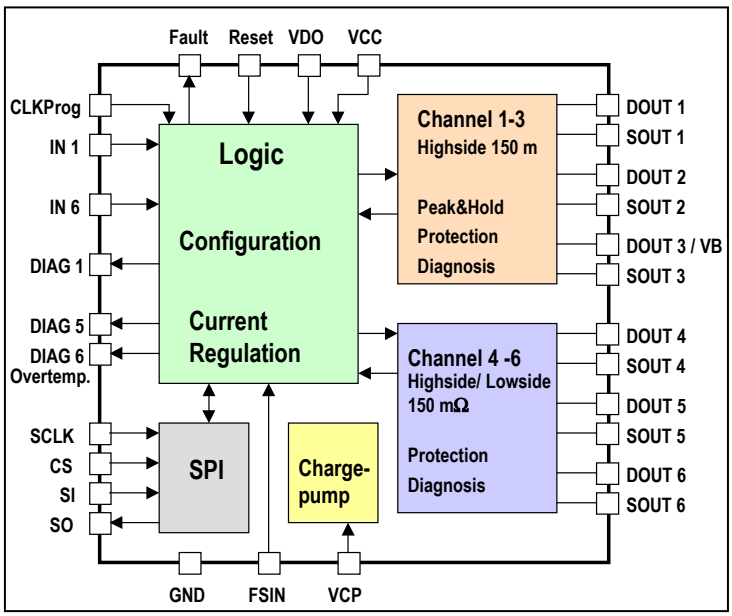
Ordering Code:

Application

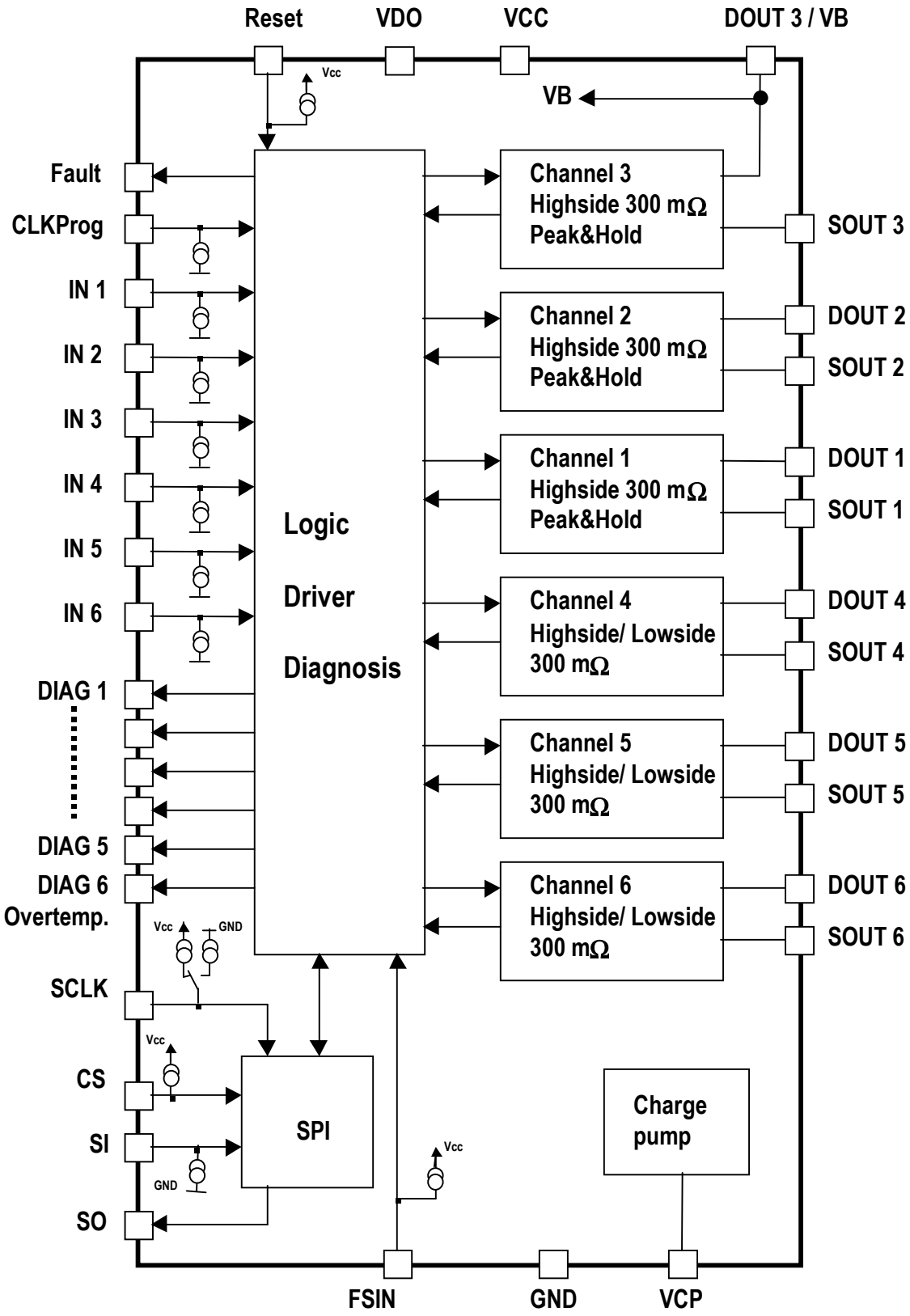
- **Solenoids, Relays and Resistive Loads**
- **Fast protected Highside Switching (PWM up to >10kHz)**
- **Peak and Hold Loads (valves, coils)**

General description

The TLE6288 R is a 6-channel (150mΩ) Smart Multichannel Switch in SPT4 Technology. The IC has embedded protection, diagnosis and configurable functions. Channel 1-3 are highside channels with integrated charge pump and can be programmed individually to do autonomous peak and hold current regulation with PWM. Channel 4-6 (also with integrated charge pump) can be configured to work as highside Switch or lowside Switch. This IC can be used to drive standard automotive loads in highside or lowside applications with switching frequencies up to 10kHz. In addition the TLE6288R can be used to drive autonomously up to 3 inductive Peak&Hold (valves, coils) loads with programmable peak and hold current values.



1. Block Diagram



2. Functional description

Block diagram will be added

Channel 1..3:

Only High Side Drive with Charge Pump.

Current Control

Default 2.4A peak and 1A hold with adjustable values by SPI

Types of current control are switched by SPI. (Refer to Fig. 1)

Current regulation: Peak Current Controller with fixed Off-Time

Peak Current, Peak Time, Hold Current and Off-Time can be selected by SPI to set average and ripple current for a given load

Channel 4..6:

Either High or Low Side Drive is configurable (by SPI)

Open load detection and switch bypassed detection can be deactivated by SPI

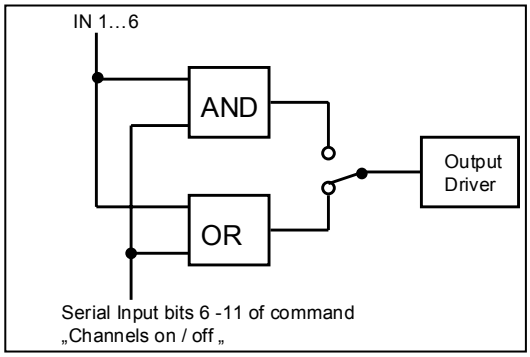
Protection: The TLE6288R has integrated protection functions[1] for overload and short circuit (active current limitation), Overtemperature, ESD at all pins and overvoltage at the power outputs (zener clamping).

Output Stage Control: Parallel Control and SPI Control

A Boolean operation (either AND or OR) is performed on each of the parallel inputs IN 1..6 and respective SPI data bits, in order to determine the states of the respective outputs. The type of Boolean operation performed is programmed via the serial interface. Both, parallel inputs and respective SPI datatabits are high active.

Truth table

parallel Input	SPI Bit	Output OR	Output AND
0	0	OFF	OFF
0	1	ON	OFF
1	0	ON	OFF
1	1	ON	ON



Each output is independently controlled by an output latch and a common reset line FSIN, which disables all outputs. A logic high input ‘data bit’ turns the respective output channel ON, a logic low ‘data bit’ turns it OFF.

Overtemperature Behavior:

Each channel has an overtemperature sensor and is individually protected against overtemperature. As soon as overtemperature occurs the channel is immediately turned off. In this case here are two different behavoirs of the affected channel that can be selected by SPI (for all channels generally).
Autorestart: as long as the input signals of the channel remains on (e.g. parallel input high) the channel turns automatically on again after cooling down.
Latching: After overtemperature shutdown the channel stays off until the this ovetemperature latch is reset by a new L→H transition of the input signal.
Note: These overtemperature sensors of the channels are only active if the channel is turned on.

An additional overtemperature sensor is located in the logic of the device. I monitors permanently the IC temperature. As soon as the IC temperature reaches a specified level an overtemperature fault will be indicated.

[1] Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

Current Regulator : Peak current control with fixed off-time

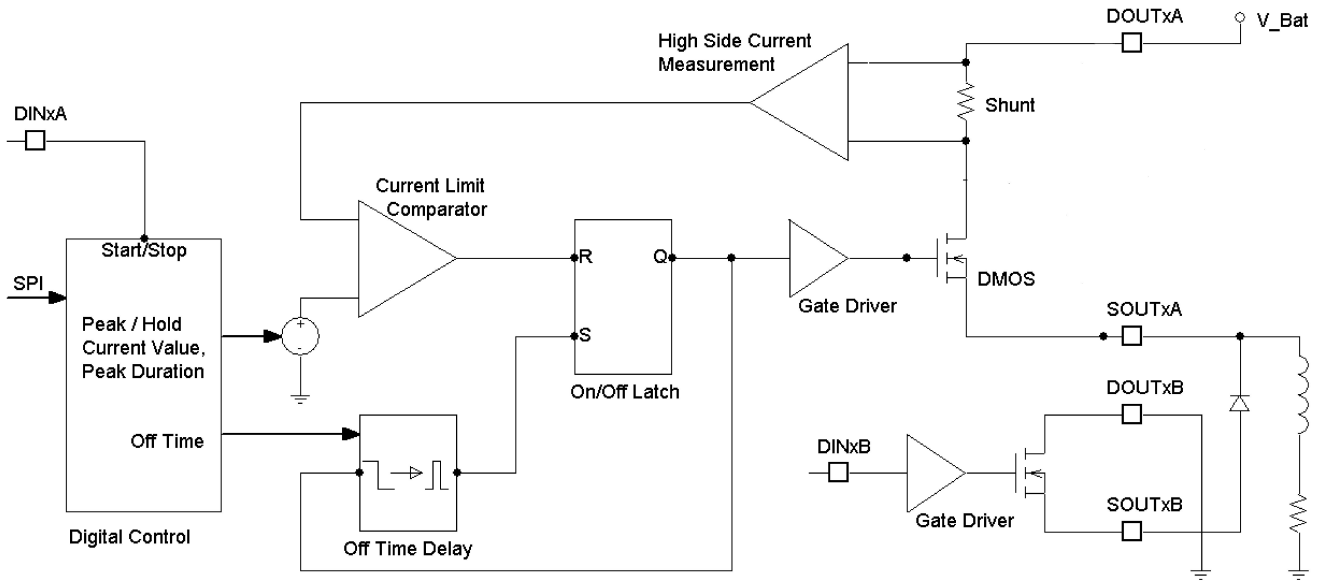
Hold only : When the channel is turned on externally (SPI or parallel input) the current rises to the programmed hold current level. Then the channel is internally turned off and a timer is started for a constant off-time (e.g. 200µs). After this time the channel is internally turned on again until the hold current level is reached again and so on. This regulation workes automatically until the channel is turned of externally.

Peak and hold mode with minimum peak time: When the channel is turned on the current rises to the programmed peak current level. Then the channel is internally turned off, the current regulator changes to hold current values and a timer is started for a constant off-time. After this time the channel is internally turned on again until the hold current value is reached and then again turned off for the fixed off time. This regulation workes automatically until the channel is turned of externally.

Peak and hold mode with programmed peak time: When the channel is turned on the current rises to the programmed peak current level. Then the channel is internally turned off and a timer is started for a constant off-time. After this time the channel is internally turned on again until the peak current value is reached and then again turned off. This works until the programmed peak time is over. Then the current regulator changes to hold current values and workes as described under "hold only".
Peak Current, Peak Time, Hold Current and fixed Off-Time can be set via SPI.

To avoid regulation disturbances by current transients during switching (e.g. caused by ESD capacitors at the outputs) the current regulator has a "leading edge blanking" of typical 20µs in all three regulation modes. After turning on the DMOS (internally or externally) the current regulation circuit is deactivated for the first 20µs. This guarantees that switching of the DMOS itself or charging of small capacitors at the output (e.g. ESD) is not disturbing the current regulation.

Simplified functional block diagram:



Current Waveforms of the different current control modes

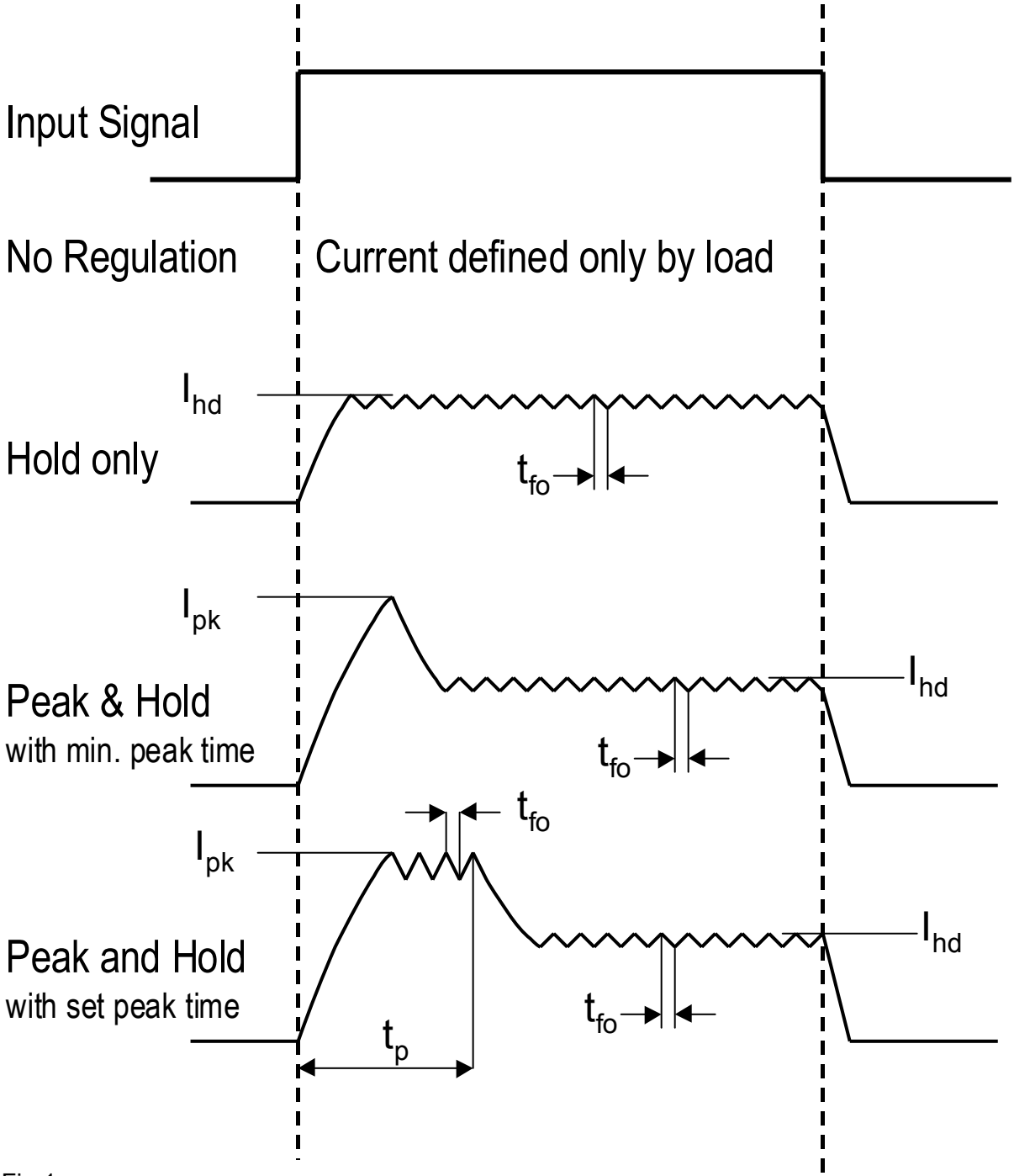
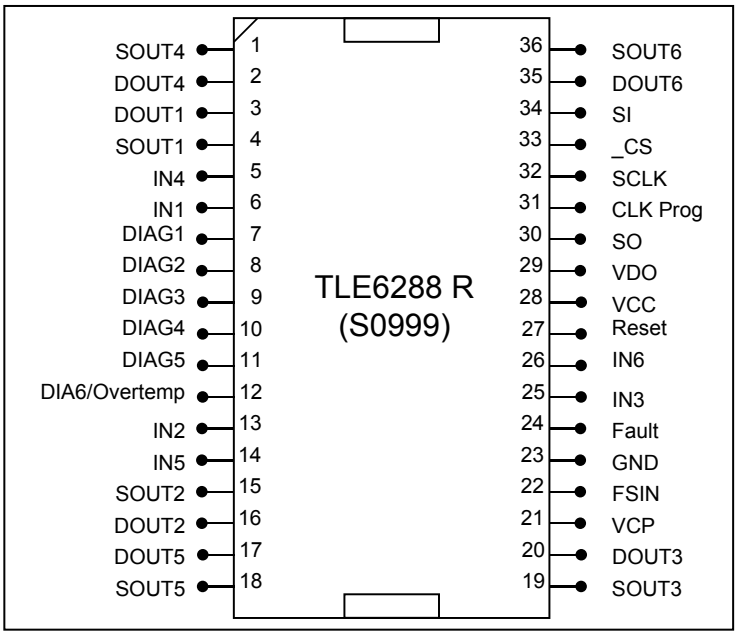


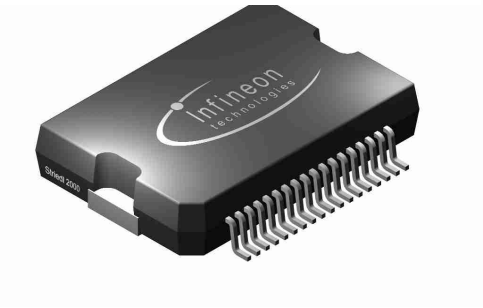
Fig.1

Current forms of the different current control modes of channel 1-3

3. Pin Configuration



Package: Power-P-DSO-36
0.65mm Pitch



Pin Nr.	Name	Function	Pin Nr.	Name	Function
1	SOUT4	Source Output CH 4 (high / low side)	**19**	SOUT3	Source Output CH 3 (high side)
2	DOUT4	Drain Output CH 4 (high / low side)	**20**	DOUT3	Drain Output CH 3(high side)
3	DOUT1	Drain Output CH 1(high side)	**21**	VCP	Charge Pump pin
4	SOUT1	Source Output CH 1 (high side)	**22**	FSIN	All Channels Enable / Disable
5	IN4	Control Input Channel 4	**23**	GND	Logic Ground
6	IN1	Control Input Channel 1	**24**	Fault	General Fault Flag
7	DIAG1	Diagnostic Output CH 1	**25**	IN3	Control Input Channel 3
8	DIAG2	Diagnostic Output CH 2	**26**	IN6	Control Input Channel 6
9	DIAG3	Diagnostic Output CH 3	**27**	Reset	Reset pin (+ Standby Mode)
10	DIAG4	Diagnostic Output CH 4	**28**	VCC	Logic Supply Voltage (5V)
11	DIAG5	Diagnostic Output CH 5	**29**	VDO	Supply Pin for digital outputs
12	DIAG6/Overtemp	Diagnostic Output CH 6 / Overtemp	**30**	SO	SPI Serial Data Output
13	IN2	Control Input Channel 2	**31**	CLKProg	Program pin of SPI Clock
14	IN5	Control Input Channel 5	**32**	SCLK	SPI Serial Clock
15	SOUT2	Source Output CH 2 (high side)	**33**	$\overline{CS}$	SPI Chip Select
16	DOUT2	Drain Output CH 2(high side)	**34**	SI	SPI Serial Data Input
17	DOUT5	Drain Output CH 5 (high / low side)	**35**	DOUT6	Drain Output CH 6 (high / low side)
18	SOUT5	Source Output CH 5 (high / low side)	**36**	SOUT6	Source Output CH 6 (high / low side)

4. Pin description:

DOUT 1-3 – Drain of the 3 highside channels. These pins must always be connected to the same power (battery) supply line.

SOUT 1-3 – Source of the three highside channels. Outputs of the highside channels where the load is connected.

DOUT 4-6 – Drain pins of the three configurable channels. In highside configuration they must be connected to the same voltage as DOUT 1-3. In lowside configuration they are the output pins and connected to the load.

SOUT 4-6 – Source of the three configurable channels. In highside configuration they are the outputs and connected to the load. In lowside configuration they must be connected with GND.

IN 1-6 – Parallel input pins for the 6 power outputs. These pins have an internal pull down structure.

GND – Logic ground pin.

FSIN – Disable pin. If the FSIN pin is in a logic low state, it switches all outputs OFF. An internal pull-up structure is provided on chip.

Reset – Reset pin. When the reset is low all channels are off, the internal biasing is deactivated, all internal registers are cleared and the supply-current consuption is reduced (standby mode). An internal pull-up structure is provided on chip.

Fault – General Fault pin. There is a general fault pin (open drain) which shows a high to low transition as soon as an error is latched into the diagnosis register. When the diagnosis register is cleared this flag is also reset (high state). This fault indication can be used to generate a µC interrupt.

CLKProg – Programming pin for the SPI Clock signal. This pin can be used to configure the clock signal input of the SPI. In low state the SPI will read data at the rising clock edge and write data at the falling clock edge. In high state the SPI will read data at the falling clock edge and write data at the rising clock edge The pin has an internal pull down structure.

DIAG1..5; DIAG6 / Overtemp. – Parallel diagnostic pins (push-pull) change state according to the input signal of the corresponding channel. As soon as an error occurs at the corresponding channel (Overload and overtemperature is detected in on state and open load /switch bypass in off state) the DIAG output shows the inverted input signal. An fault is detected only if it lasts for longer than the fault filtering time. The fault information is not latched in a register.

If DIAG6 is configured as Overtemperature Flag: This is a general fault pin which shows a high to low transition as soon as an overtemperature error occurs for any one of the six channels (for longer than the fault filtering time) or the IC logic. This fault indication can be used to differ between overload and overtemperature errors in one of the six channels or to detect a general IC overtemperature.

VCP – Pin to connect the external capacitor of the integrated charge pump.

VDO – Supply pin of the push-pull digital output drivers. This pin can be used to vary the high-state output voltage of the SO pin and the DIAG1-6 pins.

VCC – Logic supply pin. This pin is used to supply the integrated circuitry.

$\overline{\textbf{CS}}$ – Chip Select of the SPI

SO – Signal Output of the **S**erial **P**eripheral **I**nterface

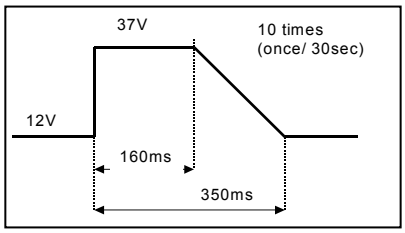
SI – Signal Input of the **S**erial **P**eripheral **I**nterface. The pin has an internal pull down structure.

SCLK – Clock Input of the **S**erial **P**eripheral **I**nterface. The pin has an internal pull up structure (if CLKProg=L) or an pull down structure (if CLKProg=H).

For more details about the SPI see Chapter 9.SPI.

5. Maximum ratings

No.	Parameter	Symbol	Value	Unit	Pin / Comment
1	Power Supply Voltage 1 static dynamic : 1min. 0°C dynamic : Test cond. Fig.1	V_B V_B V_B	-0.3 …20 24 37	V V V	DOUT1-3 DOUT1-3 DOUT1-3
2	Power Supply Voltage 2	V_{CC}, V_{DO}	- 0.3 ... 7	V	VCC, VDO
3a	Continuous Drain Source Voltage (lowside configuration)	V_{DSL}	40	V	DOUT – SOUT (channel 4-6)
3b	Continuous Source Voltage (Highside configuration)	V_{SH}	-9 ... V_B	V	SOUT - GND (channel 4-6)
4	Input Voltage	V_{IN}	-0.3 … V_{CC}+ 0.3	V	IN1-6, Reset, FSIN, CS, SCK, SI, CLKProg
5a	Output Voltage	V_{OUT}	-0.3 … V_{CC}+ 0.3	V	Fault
5b	Output Voltage	V_{OUT}	-0.3 … V_{DO}+ 0.3	V	DIAG1-6, SO
5c	Output Voltage	$V_{CP\ OUT}$	V_B +10	V	VCP ; no voltage must be applied
6	Operating Temperature	T_a T_j	-40 … +105 -40 … +150	°C °C	
7	Storage Temperature	T_{stg}	-55 … +150	°C	
8	Power Dissipation (R_{thja}= 20K/W) (R_{thja}= 30K/W)	P_{dmax}	 2,25 1,5	W	
9	Reverse Current (1ms)	I_{rev}	-4	A	between DOUT and-SOUT; Channel 4 to 6
10	ESD (Human Body Model) C= 100pF, R=1.5kΩ Applied to all terminals 3 times	V_{ESDb}	2000	V	
11	ESD (Machine Model) C= 200pF, R=0Ω Applied to all terminals 3 times	V_{ESDm}	250	V	
12	Single Switch off load Inductance		see Fig.2		DOUT, SOUT



Test cond. Fig.1

Fig.2

added after characterisation

6. Electrical Characteristics

V_{CC} = 4.5 to 5.5 V ; T_j = - 40 °C to + 150 °C ; V_B = 6V to 16V ; Reset = H ; V_{DO} = V_{CC} (unless otherwise specified)

No.	Parameter	Sym-bol	Condition	Value			Unit	Pin / Comment
				min	typ	max		
1	**Power Supply, Reset**							
1.1	Power Supply Current 1	I_b	Ch1-Ch6: Off			10	mA	DOUT1-3
1.2	Power Supply Current 2	I_{cc}				10	mA	VCC
1.3	Power Supply Current 3 in Standby Mode	I_{cc}+I_b	Reset = L			50	µA	DOUT1-3, VCC
1.4	Minimum Reset Duration	$t_{Re-set,min}$		50			µs	
1.5	Wake up time after reset	t_{wakeup}	C_{cp} = 10 nF			5	ms	
2	**Power Outputs**							
2.1	On Resistance	$R_{DS(ON)}$	I_D =2.4A V_B=10V			350	mΩ	DOUTx – SOUTx
2.2	Forward Voltage Revers Diode	V_{RDf}	I_D = -4A T_j = 150°C			2	V	SOUTx – DOUTx
2.3	Peak Current range	I_{pk}			1.2 -- 3.6		A	
2.4	Peak Current accuracy	I_{pka}	Tj= 25, 150° Tj=-40			± 15 ± 20	%	
2.5	Hold Current range	I_{hd}			0.7 -- 2		A	
2.6	Hold Current accuracy	I_{hda}	Tj= 25, 150° Tj=-40			± 15 ± 20	%	
2.7	Peak time range	t_p			0.8 -- 3.6		ms	
2.8	Peak time accuracy	t_{pa}				±20	%	
2.9	Fixed off Time range	t_{fo}			100 -- 400		µs	
2.10	Fixed off Time accuracy	t_{foa}	100µs			±30	%	
2.11	Fixed off Time accuracy		200µs-400µs			±20	%	

V_{CC} = 4.5 to 5.5 V ; T_j = - 40 °C to + 150 °C ; V_B = 6V to 16V ; Reset = H ; V_{DO} = V_{CC} (unless otherwise specified)

No.	Parameter	Sym-bol	Condition	Value			Unit	Pin / Comment
				min	typ	max		
2.12	Output ON Delay time1	t_{dON}	Fig.3			10	µs	
2.13	Output ON Rise time1	t_r	Fig.3			10	µs	
2.14	Output OFF Delay time1	t_{dOFF}	Fig.3 HS- Mode LS- Mode			 20 20	 µs	
2.15	Output OFF Fall time1	t_f	Fig.3			10	µs	
2.16	Leackage Current		Reset = L			10	µA	
2.17	Leak Current in OFF (highside configuration)	I_{loff}				-250	µA	SOUT1-6
2.18	Leak Current in OFF (lowside configuration)	I_{loff}				500	µA	DOUT4-6
2.19	Output Clamp Voltage Highside Configuration	V_{clh}	Referes to GND level	-9	-14	-19	V	SOUT1-6
2.20	Output Clamp Voltage Lowside Configuration	V_{cll}	Referes to GND level	40		55	V	DOUT4-6
2.21	Current limitation (Channel 1-3)	$I_{Dlim1-3}$		4		6	A	
2.22	Current limitation (Channel 4-6)	$I_{Dlim4-6}$		3		6	A	
2.23	IC Overtemp. Warning Hysteresis	T_{ot} T_{hys}		160	 10	180	°C °C	
3	**Digital Inputs**							
3.1	Input Low Voltage	V_{INL}				1	V	all digit. inputs
3.2	Input High Voltage	V_{INH}		2			V	all digit. inputs
3.3	Input Voltage Hysteresis	V_{INHys}			100		mV	all digit. inputs
3.4	Input Pull Down current	I_{pd}	V_{IN} = 5V	20	50	100	µA	IN1-6; CLKProg
3.5	Input Pull Up current	I_{pu}	V_{IN} = GND	20	50	100	µA	Reset; FSIN
3.6	SPI Input Pull Down current	I_{pd}	V_{IN} = 5V	10	20	50	µA	SI, SCLK (CLKProg=H)
3.7	SPI Input Pull Up current	I_{pd}	V_{IN} = GND	10	20	50	µA	CS;SCLK (CLKProg=L)

V_{CC} = 4.5 to 5.5 V ; T_j = - 40 °C to + 150 °C ; V_B = 6V to 16V ; Reset = H ; V_{DO} = V_{CC} (unless otherwise specified)

No.	Parameter	Sym-bol	Condition	Value			Unit	Pin / Comment
				min	typ	max		
4	**Digital Outputs**							
4.1	SO Low State Output Voltage	V_{SOL}	I_{SOL}=2.5mA			0.4	V	SO
4.2	SO High State Output Voltage	V_{SOH}	I_{SOH}=-2mA	V_{DO}-0.4V			V	SO
4.3	DIAG Low State Output Voltage		I_{DIAGL}= 50µA			0.4	V	DIAG1-6
4.4	DIAG High State Output Voltage		I_{DIAGH}= -50µA	V_{DO}-0.4V			V	DIAG1-6
4.5	Fault Low Output Voltage	V_{ol}	I_{out}= 1mA			0.4	V	Fault
4.6	Fault Output leak Current	I_{oh}	Output :OFF $V_{(fault)}$ =5V			1	µA	Fault
5	**Diagnostic Functions**							
5.1	Open Load Detection Voltage	$V_{DS(OL)}$	lowside con-figuration, Vbat=12V		5.5		V	
5.2	Open Load Detection Voltage	$V_{DS(OL)}$	highside configura-tion, Vbat=12V		4.5		V	
5.3	Output Open Load diag-nosis Current	$I_{d(OL)}$	Vbat=Vout= 12V	20	100	500	µA	
5.4	Fault Filter Time	$t_{f(fault)}$		50	100	200	µs	
5.5	Switch Bypass Detec-tion Current	$I_{d(SB)}$				250	µA	
5.6	Overload Detection Threshold (Channel 1-3)	$I_{Dd(lim1-3)}$		4		6	A	
5.7	Overload Detection Threshold (Channel 4-6)	$I_{Dd(lim 4-6)}$		3		6	A	

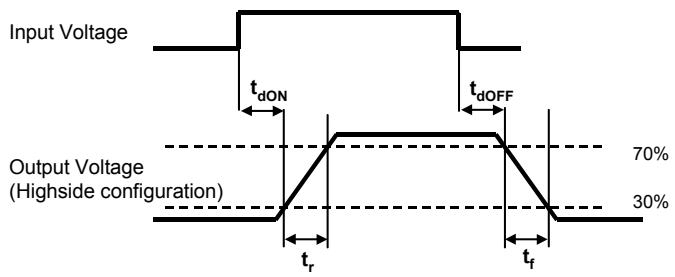


Fig.3 : Turn on/off timings with resistive load

V_{CC} = 4.5 to 5.5 V ; T_j = - 40 °C to + 150 °C ; V_B = 6V to 16V ; Reset = H ; V_{DO} = V_{CC} (unless otherwise specified)

No.	Parameter	Symbol	Condition	Value			Unit	Pin / Comment
				min	typ	max		
6	**SPI Timing**							
6.1	Serial Clock Frequency (depending on SO load)	f_{SCK}		DC	--	5	MHz	
6.2	Serial Clock Period (1/fclk)	$t_{p(SCK)}$		200	--	--	ns	
6.3	Serial Clock High Time	t_{SCKH}		50	--	--	ns	
6.4	Serial Clock Low Time	t_{SCKL}		50	--	--	ns	
6.5	Enable Lead Time (falling edge of $\overline{CS}$ to falling edge of SCLK)	t_{leadL}	CLKProg=L	200	--	--	ns	
	Enable Lead Time (falling edge of $\overline{CS}$ to rising edge of SCLK)	t_{leadH}	CLKProg=H	200	--	--	ns	
6.6	Enable Lag Time (rising edge of SCLK to rising edge of $\overline{CS}$)	t_{lagL}	CLKProg=L	200	---	--	ns	
	Enable Lag Time (falling edge of SCLK to rising edge of $\overline{CS}$)	t_{lagH}	CLKProg=H	200	---	--	ns	
6.7	Data Setup Time (required time SI to rising of SCLK)	t_{SUL}	CLKProg=L	20	--	--	ns	
	Data Setup Time (required time SI to falling of SCLK)	t_{SUH}	CLKProg=H	20	--	--	ns	
6.8	Data Hold Time (rising edge of SCLK to SI)	t_{HL}	CLKProg=L	20	--	--	ns	
	Data Hold Time (falling edge of SCLK to SI)	t_{HH}	CLKProg=H	20	--	--	ns	
6.9	Disable Time	t_{DIS}			--	200	ns	
6.10	Transfer Delay Time[2] ($\overline{CS}$ high time between two accesses)	t_{dt}		200	--	--	ns	
6.11	Data Valid Time C_L = 50 pF to 100pF C_L = 220 pF	t_{valid}		 -- --	 -- --	 120 150	ns	

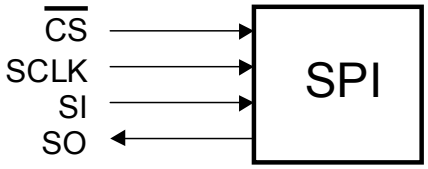
[1)] To get the correct diagnostic information, the transfer delay time has to be extended to the maximum fault delay time $t_{f(fault)max}$ = 200µs.

7 Diagnostics

detailled description of the diagnosis will be added

8 SPI

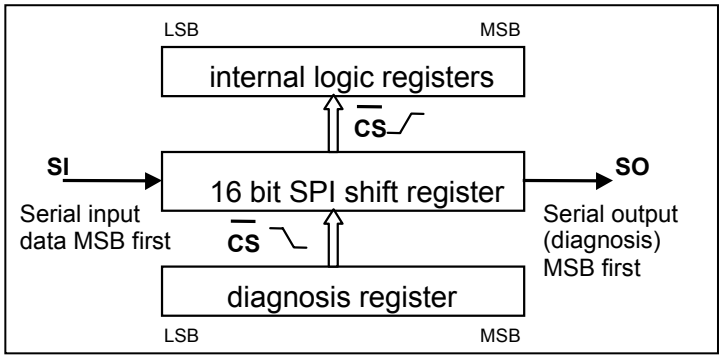
The SPI is a **S**erial **P**eripheral **I**nterface with 4 digital pins and an 16 bit shift register. The SPI is used to configure and program the device, turn on and off channels and to read detailled diagnostic information.



8.1 SPI Signal Description:

$\overline{CS}$ - Chip Select. The system microcontroller selects the TLE 6288 R by means of the $\overline{CS}$ pin. Whenever the pin is in a logic low state, data can be transferred from the µC and vice versa.

$\overline{CS}$ = H : Any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.



$\overline{CS}$ = H→L :

- diagnostic information is transferred from the diagnosis register into the SPI shift register.
- serial input data can be clocked into the SPI shift register from then on
- SO changes from high impedance state to logic high or low state corresponding to the SO bits

$\overline{CS}$ = L : SPI is working like a shift register. With each clock signal the state of the SI is read into the SPI shift-register and one diagnosis bit is written out of SO.

$\overline{CS}$ = L→H:

- transfer of SI bits from SPI shift register into the internal logic registers
- reset of diagnosis register if sent command was valid

To avoid any false clocking the serial clock input pin SCLK should be logic high state (if CKLProg=L; low state if CLKProg=H) during high to low transition of $\overline{CS}$.

SCLK - Serial Clock. The serial clock pin clocks the internal SPI shift register of the TLE 6288 R. The serial input (SI) accepts data into the input SPI shift register on the rising edge of SCLK (if CKLProg=L; falling edge if CLKProg=H) while the serial output (SO) shifts diagnostic information out of the SPI shift register on the falling edge (if CKLProg=L; rising edge if CLKProg=H) of serial clock. It is essential that the SCLK pin is in a logic high state (if CKLProg=L; low state if CLKProg=H) whenever chip select $\overline{CS}$ makes any transition.

SI - Serial Input. Serial data bits are shifted in at this pin, the most significant bit (MSB) first. SI information is read in on the rising edge of SCLK (if CKLProg=L; falling edge if CLKProg=H). Input data is latched in the SPI shift register and then transferred to the internal registers of the logic.

The input data consist of 16 bit, made up of 4 control bits and 12 data bits. The control word is used to program the device, to operate it in a certain mode as well as providing diagnostic information (see SPI Commands).

SO - Serial Output. Diagnostic data bits are shifted out serially at this pin, the most significant bit (MSB) first. SO is in a high impedance state until the $\overline{CS}$ pin goes to a logic low state. New diagnostic data will appear at the SO pin following the falling edge of SCLK (if CKLProg=L; rising edge if CLKProg=H).

8.2 SPI Diagnostics:

As soon as a fault occurs for longer than the fault filtering time, the fault information is latched into the diagnosis register (and the Fault pin will change from high to low state). A new error on the same channel will over-write the old error report. Serial data out pin (SO) is in a high impedance state when $\overline{CS}$ is high. If $\overline{CS}$ receives a LOW signal, all diagnosis bits can be shifted out serially. If the sent command was valid the rising edge of $\overline{CS}$ will reset the diagnosis registers (except the channel OT flag) and restart the fault filtering time. In case of an invalid command the device will ignore the data bits and the diagnosis register will not be reset at the rising $\overline{CS}$ edge.

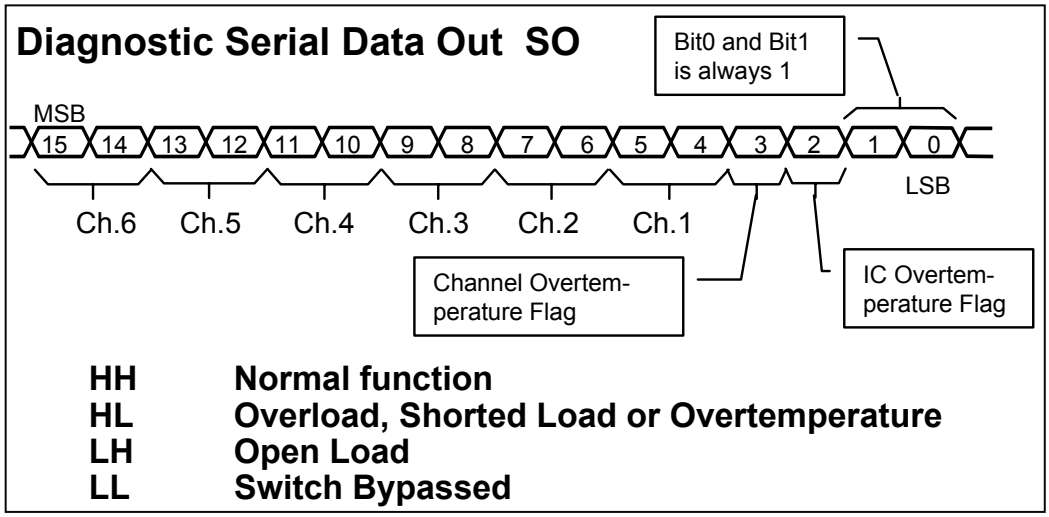


Figure 1: Two bits per channel diagnostic feedback plus two overtemperature flags

For Full Diagnosis there are two diagnostic bits per channel configured as shown in Figure 1. Diagnosis bit0 and bit1 are always set to 1.

Normal function: The bit combination **HH** indicates that there is no fault condition, i.e. normal function.

Overload, Shorted Load or Overtemperature: HL is set when the current limitation gets active, i.e. there is a overload, short to supply or overtemperature condition. The second reason for this bit combination is overtemperature of the corresponding channel.

Open load: LH is set when open load is detected (in off state of the channel)

Switch Bypassed:

Short to GND : in lowside configuration LL is set when this condition is detected

Short to Battery : in highside configuration LL is set when this condition is detected

Channel Overtemperature Flag: In case of overtemperature in any output channel in on state the overtemperature Flag in the SPI diagnosis register is set (change bit 3 from 0 to 1). This Bit can be used to distinguish between Overload and Overtemperature (both HL combination) and is reset by switching OFF/ON the affected channel.
In addition the DIAG6 / Ovtertemp pin is set low (if configured as Overtemp.Flag).

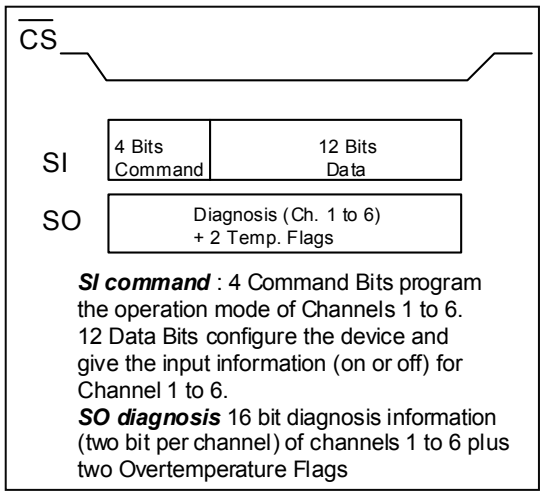
IC Overtemperature Flag: When the IC logic tremperature exceeds typ.170° the non-latching IC Overtemperature Flag will be set in the SPI diagnosis register(change bit 2 from 0 to 1).

In addition the DIAG6 / Ovtertemp pin is set low (if configured as Overtemp.Flag).

8.3 SPI Commands, Values and Parameters:

The 16 bit SPI is used to program different IC functions and values, turn on and off the channels and to get detailled diagnosis information. Therefore 4 command bits and 12 data bits are used.

The following parameters and functional behavior can be programmed by SPI:



SI command : 4 Command Bits program the operation mode of Channels 1 to 6. 12 Data Bits configure the device and give the input information (on or off) for Channel 1 to 6.
SO diagnosis 16 bit diagnosis information (two bit per channel) of channels 1 to 6 plus two Overtemperature Flags

Current regulation Mode (mode) : for each of the three highside channels individually the operation mode can be set.
a) "no current regulation
b) Current regulation "hold only
c) Current regulation "peak & hold with minimum peak time
d) Current regulation "peak & hold with programmed peak time".

Peak Current (I_{pk}) : for each of the three highside channels individually the peak current value for P&H current regulation can be programmed. The current range is 1.2A to 3.6A.

Fixed off time of the current regulator (t_{fo}) : for each of the three highside channels (Ch1 - Ch3) individually the fixed off time for all modes with current regulation can be programmed from 100µs to 400µs.

Hold Current (I_{hd}) : for each of the three highside channels(Ch1 - Ch3) individually the hold current value for P&H and hold only current regulation can be programmed. The current range is 0.7A to 2.0A

Peak Time (t_p) : for each of the three highside channels(Ch1 - Ch3) individually the peak time value for P&H current regulation can be programmed. The time range is 0.8ms to 3.6ms.

Highside / Lowside Configuration (H/L) : Each of the three configurable channels (Ch4 – Ch6) can be programmed for use as Highside Switch or Lowside Switch.

Open load and switch bypassed detection activated or deactivated (OL+SB) : For each of the three configurable channels(Ch4 – Ch6) the open load and switch bypassed diagnosis can be deactivated. In lowside configuration the open load and the short to GND detection can be deactivated, in highside configuration the open load and short to battery detection.

Boolean Operation (OR / AND) : For all channels generally the Boolean operation of the parallel input signal and the SPI bit of the corresponding channel can be defined.

Overtemperature Behavior (R/L) **:** The overtemperature behavior of the channels can be programmed by SPI. Autorestart or latching overtemperature shutdown can be selected (for all channels the same behavior).

DIAG6 or Overtemperature Flag (D/F) : With this SPI bit the function of the DIAG6/Overtemp pin is defined. This output can work as diagnosis output of channel 6 or as Overtemperature Flag.

8.4 SPI Commands

Command Table

No	Command	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
1	Config. Regulator 1	1	0	0	1	Mode		I_{pk}		t_{fo}		I_{hd}		t_p			X
2	Config. Regulator 2	1	0	1	0	Mode		I_{pk}		t_{fo}		I_{hd}		t_p			X
3	Config. Regulator 3	1	0	1	1	Mode		I_{pk}		t_{fo}		I_{hd}		t_p			X
						Ch. 6		Ch. 5		Ch 4		all	all	DIAG 6			
4	Config. Ch1 - Ch6	1	1	0	0	H/L	OL+ SB	H/L	OL+ SB	H/L	OL+ SB	OR/ AND	R/L	D/F	X	X	X
5	Set all to Default	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
6	Diagnosis only	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X
7	Channels on / off	1	1	0	1	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	X	X	X	X	X	X

Legend of SPI Command Table:
Mode: Operation mode of the current regulator:
- a) no regulation
- b) hold only
- c) peak&hold with minimum peak time
- d) peak&hold with programmed peak time

I_{pk} : Peak current values 1.2A - 3.6A
I_{hd} : Hold current values 0.7A - 2A
t_p : Peak time value 0.8ms – 3.6ms
t_{fo} : Fixed off time value 100µs – 400µs
H/L : Channel 1-3 in highside or lowside configuration
OL+SB : open load detection and switch bypassed detection activated or deactivated
OR / AND : Boolean Operation (parallel input and corresponding SPI Bit)
R/L : Autorestart or Latching overtemperature behaviour
D/F : DIAG6/Overtemp pin set as Diagnosis output of channel 6 or as Overtemperature Flag
Ch1-Ch6 : On / Off information of the output drivers (high active)

Command description:
Config. Regulator 1-3: With this command the values for for the current regulation and the functional mode of the channel is written into the internal logic registers.
Config. Ch1- Ch6 : This command writes the configuration data of the three configurable channels (4-6) and sets the Boolean operation and overtemperature behavior of all channels. It also and sets the DIAG6/Overtemp. pin to Diagnosis of channel 6 or Overtemperature Flag.
Set all to default : This command sets all internal logic registers back to default settings.
Diagnosis only : When this command is sent the 12 data bits are ignored. The internal logic registers are not changed.
Channels on/off : With this command the SPI bits for the ON/OFF information of the 6 Channels are set

Note: Specified control words (valid commands) are executed and the diagnosis register is reset after the rising $\overline{CS}$ edge.
Not specified control words are not executed (cause no function) and the diagnosis register is not reset after the $\overline{CS}$ = L→H signal.

8.5 Default settings for the internal logic registers:

Mode	:no regulation
Peak Current (Ipeak)	:2.4A
Hold Current (Ihold)	:1A
Fixed off Time (toff)	:200µs
Peak Time (tpeak)	:2.8ms
AND / OR	:OR
Autorestart / Latch	:Restart
Diag6 / Temp. Fault	:Diagnosis channel 6
Highside / Lowside (4-6)	:Highside
Open load & SB Yes/No (4-6)	:Yes (diagnosis active)
Channels 1-6 (ON / OFF)	:OFF
SPI	:all 0

8.6 Bit Assignment:

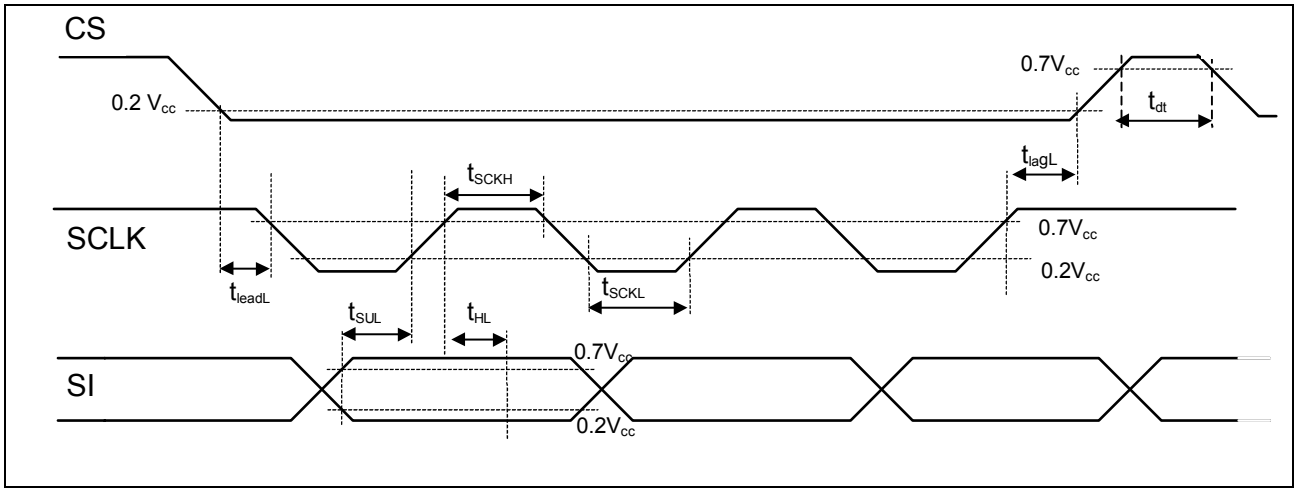
Mode	**00**	**no current regulation**
	01	hold only
	10	P&H minimum peak time
	11	P&H with programmed times

Peak Current (I_{pk})::	: 1.2A	1.8A	**2.4A**	3.6A				
2 Bits	: 0 0	0 1	**1 0**	1 1				
Hold Current (I_{hd})	: 0.7A	**1A**	1.4A	2A				
2 Bits	: 0 0	**0 1**	1 0	1 1				
Fixed off Time (t_{fo})	: 100µs	**200µs**	300µs	400µs				
2 Bits	: 0 0	**0 1**	1 0	1 1				
Peak Time (t_p)	: 0.8	1.2	1.6	2	2.4	**2.8**	3.2	3.6 [ms]
3 Bits	: 000	001	010	011	100	**101**	110	111
Boolean operation	: **OR**		AND					
1 Bit	: **0**		1					
Overtemp. behavior	: **Restart**		Latch					
1 Bit	: **0**		1					
Diag6 / Overtemp	:**Diag6**		Overtemp. Flag					
1 Bit	:**0**		1					
Highside/Lowside	:**Highside**		Lowside					
1 Bit	:**0**		1					
Open Load & SB (4-6)	:**Yes**		No					
1 Bit	:**0**		1					

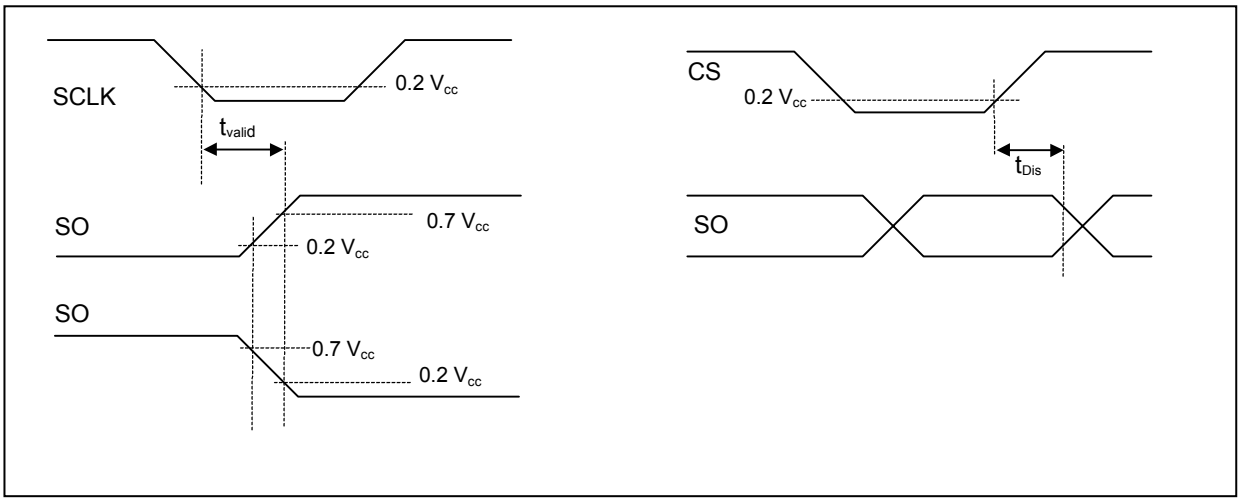
Default settings are pin **bold print.**

8.7 SPI Timing Diagrams :

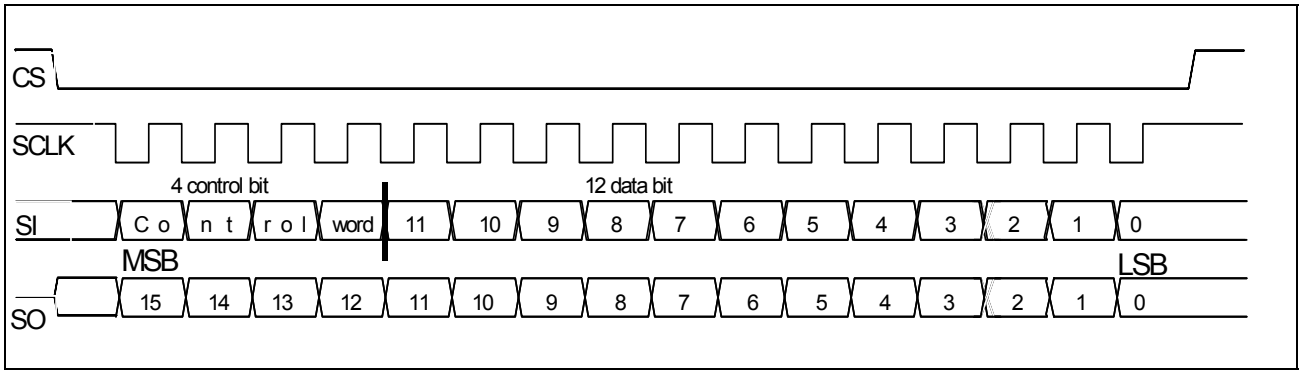
Input Timing Diagram (CLKProg = L)



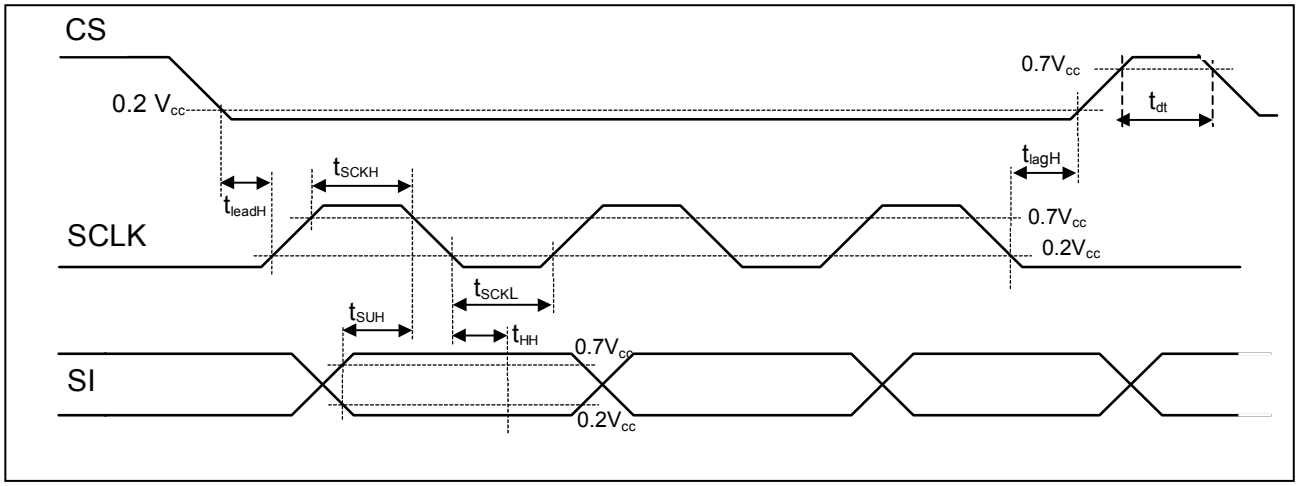
SO Valid Time Waveforms (CLKProg = L)



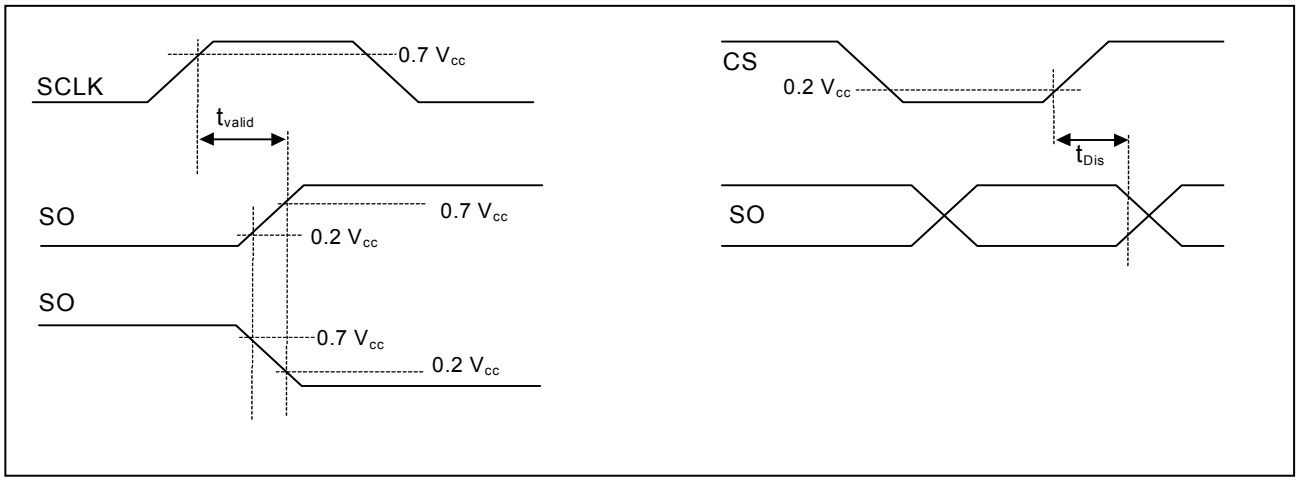
Enable and Disable Time Waveforms



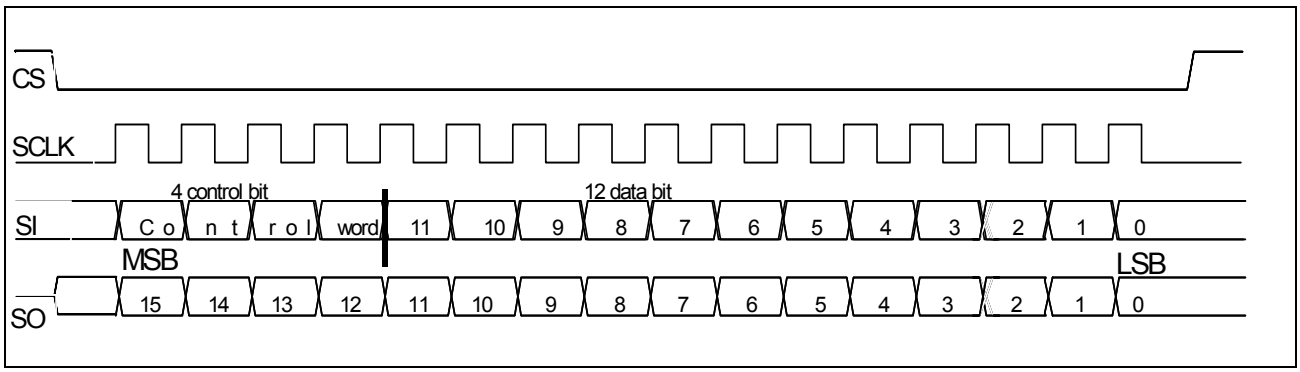
Input Timing Diagram (CLKProg = H)



SO Valid Time Waveforms (CLKProg = H)

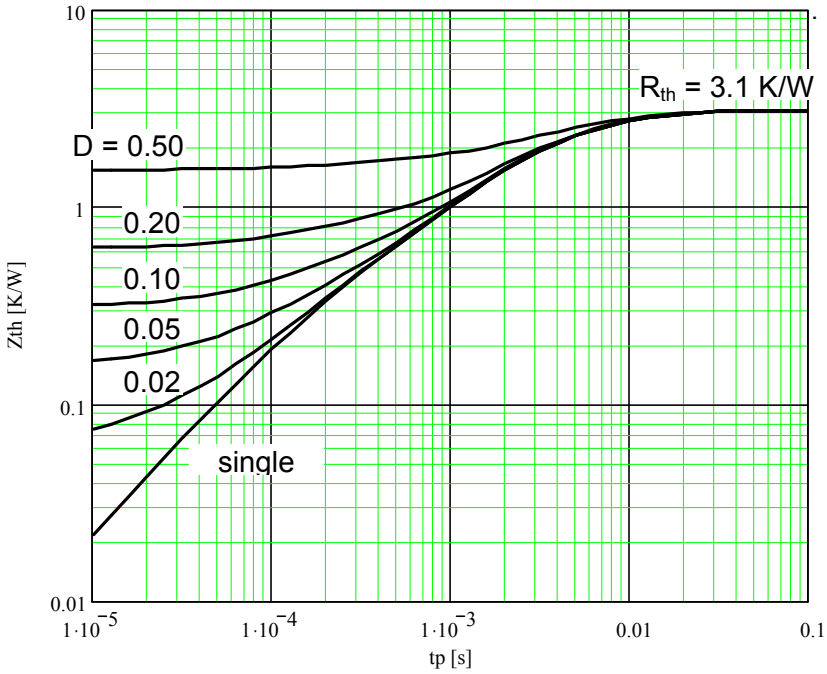


Enable and Disable Time Waveforms



9 Typicel Characteristics

9.1 Zth Diagramm



Conditions:

T_{case} = 125°C

Single Channel Operation

Parameters:

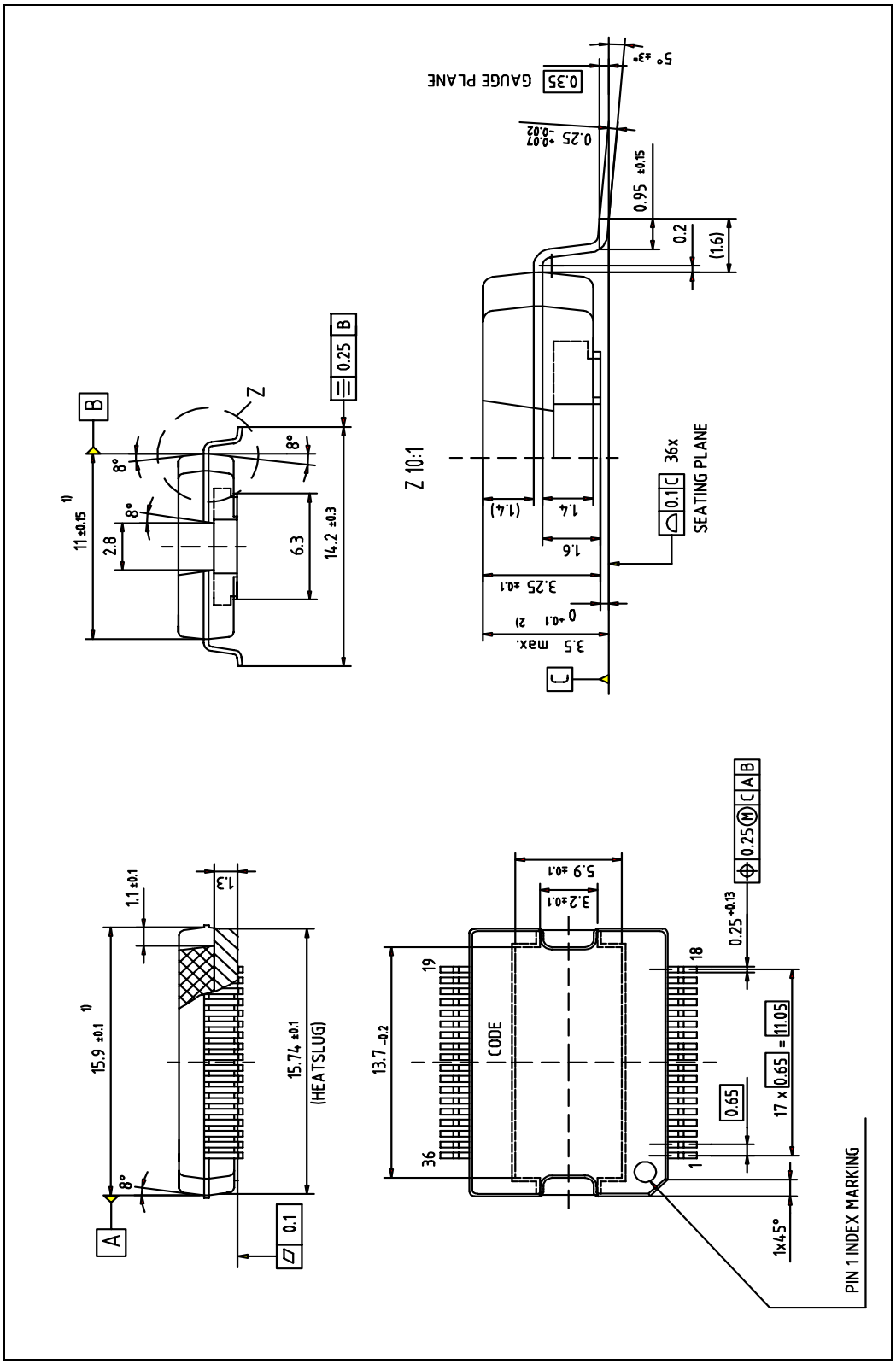
tp ..... Pulse Width

D ..... Duty Cycle

10 Package

(all dimensions in mm)

P-DSO 36-12



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