Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics

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Virtex-7 FPGA Electrical Characteristics

Virtex-7 FPGAs are available in -3, -2, -1, and -1L speed grades, with -3 having the highest performance. Virtex-7 FPGA DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Virtex-7 FPGA data sheet, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at www.xilinx.com/7.

All specifications are subject to change without notice.

Virtex-7 FPGA DC Characteristics

Table 1: **Absolute Maximum Ratings** (1)

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.1	V
	For -1L devices: Internal supply voltage relative to GND	–0.5 to 1.0	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 2.0	V
V_{CCAUX_IO}	Auxiliary supply voltage relative to GND	–0.5 to 2.06	V
V_{CCO}	Output drivers supply voltage relative to GND for 3.3V HR banks	–0.5 to 3.6	V
	Output drivers supply voltage relative to GND for 1.8V HP banks	–0.5 to 2.0	V
V_{CCBRAM}	Supply voltage for the block RAM memories	–0.5 to 1.1	V
V_{CCADC}	XADC supply relative to GNDADC	–0.5 to 2.0	V
V_{CCBATT}	Key memory battery backup supply	–0.5 to 2.0	V
V_{REF}	Input reference voltage	–0.5 to 2.0	V
V_{REFP}	XADC reference input relative to GNDADC	–0.5 to 2.0	V
V_{IN} (2)	3.3V or below I/O input voltage relative to GND (3) (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
	1.8V or below I/O input voltage relative to GND (3) (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state 1.8V or below output (3) (user and dedicated I/Os)	–0.5 to V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to 150	°C
T_{SOL}	Maximum soldering temperature (4)	+220	°C
T_j	Maximum junction temperature (4)	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The 3.3V and 1.8V I/O absolute maximum limit applied to DC and AC signals.
3. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide*.
4. For soldering guidelines and thermal considerations, see *7 Series FPGA Packaging and Pinout Specification*.

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Table 2: **Recommended Operating Conditions (1)**

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_j = 0°C to +85°C	0.97	1.03	V
	For -1L devices: internal supply voltage relative to GND, T_j = 0°C to +85°C	0.87	0.93	V
V_{CCAUX}	Auxiliary supply voltage relative to GND, T_j = 0°C to +85°C	1.71	1.89	V
V_{CCAUX_IO}	Auxiliary supply voltage relative to GND	1.71	2.06	V
V_{CCO}(2)(4)(5)	Supply voltage for 3.3V HR I/O banks relative to GND, T_j = 0°C to +85°C	1.11	3.45	V
	Supply voltage for 1.8V HP I/O banks relative to GND, T_j = 0°C to +85°C	1.11	1.89	V
V_{CCBRAM}	Block RAM supply voltage	0.97	1.03	V
V_{CCBATT}(3)	Battery voltage relative to GND, T_j = 0°C to +85°C	1.0	1.98	V
V_{IN}	I/O input voltage relative to GND, T_j = 0°C to +85°C	GND – 0.20	V_{CCO} + 0.2	V
I_{IN}(6)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	10	mA

Notes:

1. All voltages are relative to ground.
2. Configuration data is retained even if V_{CCO} drops to 0V.
3. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
4. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0}.
6. A total of 100 mA per bank should not be exceeded.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ(1)	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)				V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)				V
I_{REF}	V_{REF} leakage current per pin				µA
I_L	Input or output leakage current per pin (sample-tested)				µA
C_{IN}(2)	Die input capacitance at the pad				pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V				µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V				µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V				µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V				µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V				µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V				µA
	Pad pull-down (when selected) @ V_{IN} = 1.8V				µA
I_{BATT}(3)	Battery supply current				nA
n	Temperature diode ideality factor				n
r	Series resistance				Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.

Important Note

Typical values for quiescent supply current are specified at nominal voltage, 85°C junction temperatures (T_j). Xilinx recommends analyzing static power consumption at T_j = 85°C because the majority of designs operate near the high end of the commercial temperature range. Quiescent supply current is specified by speed grade for Virtex-7 devices. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified in Table 4.

Table 4: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed and Temperature Grade				Units
			-3	-2	-1	-1L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC7V285T					mA
		XC7V450T					mA
		XC7V585T					mA
		XC7V855T					mA
		XC7V1500T	N/A				mA
		XC7V2000T	N/A				mA
		XC7VX485T				N/A	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC7V285T					mA
		XC7V450T					mA
		XC7V585T					mA
		XC7V855T					mA
		XC7V1500T	N/A				mA
		XC7V2000T	N/A				mA
		XC7VX485T				N/A	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7V285T					mA
		XC7V450T					mA
		XC7V585T					mA
		XC7V855T					mA
		XC7V1500T	N/A				mA
		XC7V2000T	N/A				mA
		XC7VX485T				N/A	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j).
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

The recommended power-on and reverse power-off sequence for Virtex-7 devices is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure I/Os are 3-stated at power-up. In cases where the recommended sequence cannot be met, the following rules ensure that the I/Os remain 3-stated and no device damage will occur. V_{CCINT} and V_{CCBRAM} can be powered on or off at any time as long as the following rules are met:

- V_{CCAUX} and V_{CCAUX_IO} must be powered prior to V_{CCO}. The sequencing of V_{CCAUX} and V_{CCAUX_IO} relative to each other does not matter.
- V_{CCAUX} and V_{CCO} can be powered by the same supply.
- V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} can ramp simultaneously.
- During operation, the V_{CCAUX},V_{CCAUX_IO}, and V_{CCINT} voltages must stay within their specifications (see Table 2).

When powering down, the reverse power-up sequencing rules are recommended for the same reasons given during power up. V_{CCO} must be powered down prior to V_{CCAUX} and V_{CCAUX_IO}, or if powered by the same supply, V_{CCO} can be powered down simultaneously.

In -3, -2, and -1 devices, if V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels, then both can be powered by the same supply. Both V_{CCINT} and V_{CCBRAM} can be powered up or down any time during the recommended sequence.

Table 5 shows the minimum current, in addition to I_{CCQ}, that are required by Virtex-7 devices for proper power-on and configuration. If the current minimums shown in Table 4 and Table 5 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 5: **Power-On Current for Virtex-7 Devices**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	Units
	Typ(1)	Typ(1)	Typ(1)	
XC7V285T				mA
XC7V450T				mA
XC7V585T				mA
XC7V855T				mA
XC7V1500T				mA
XC7V2000T				mA
XC7VX485T				mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.

Table 6: **Power Supply Ramp Time**

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms
V_{CCBRAM}	Block RAM supply voltage relative to GND	0.20 to 50.0	ms

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 7: **SelectIO DC Input and Output Levels** (1)(2)

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL	–0.3	0.8	2.0	3.45	0.4	2.4	Note 3	Note 3
LVCMOS33	–0.3	0.8	2.0	3.45	0.4	V_{CCO} – 0.4	Note 4	Note 4
LVCMOS25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note 4	Note 4
LVCMOS18, LVDCI18	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.45	V_{CCO} – 0.45	Note 5	Note 5
LVCMOS15, LVDCI15	–0.3	30% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note 6	Note 6
LVCMOS12	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note 7	Note 7
PCI33_3	–0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
HSTL I_12	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I(8)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II(8)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
DIFF HSTL I(8)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
DIFF HSTL II(8)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
SSTL135	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3				
DIFF SSTL135	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3				
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	8	–8
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 I	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.608	V_{TT} + 0.608	–	–
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
SSTL15	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	V_{TT} – 0.175	V_{TT} + 0.175	17.8	17.8

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 4, 8, 12, 16, or 24 mA
4. Supported drive strengths of 4, 8, 12, or 16 mA
5. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, or 16 mA in HR I/O banks.
7. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks and 4, 8, or 12 mA in HR I/O banks.
8. Applies to both 1.5V and 1.8V HSTL.
9. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide*.

LVDS DC Specifications (LVDS_25)

Table 8: **LVDS_25 DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage					V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals				V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals				V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals				mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals				V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High					mV
V_{ICM}	Input Common-Mode Voltage					V

LVDS DC Specifications (LVDS)

Table 9: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage					V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals				V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals				V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals				mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals				V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V				mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV				V

eFUSE Read Endurance and Programming Conditions

Table 10 lists the maximum number of read cycle operations expected. Table 11 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide*.

Table 10: **eFUSE Read Endurance**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.					Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.					Read Cycles

Table 11: **eFUSE Programming Conditions**

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	40	mA
t_j	Temperature range	15	–	85	°C

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 12: **Recommended Operating Conditions for GTX Transceivers (1)(2)**

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	0.97	1.0	1.03	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	1.17	1.2	1.23	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.17	1.2	1.23	V
MGTVCCAUX	Auxiliary analog Quad PLL (QPLL) voltage supply for the transceivers	1.75	1.80	1.85	V

Notes:

1. Each voltage listed requires the filter circuit described in *7 Series FPGAs Transceiver User Guide*.
2. Voltages are specified for the temperature range of T_j = 0°C to +85°C.

GTX Transceiver DC Input and Output Levels

Table 13 summarizes the DC output specifications of the GTX transceivers in Virtex-7 FPGAs. Consult the *7 Series FPGAs Transceiver User Guide* for further details.

Table 13: **GTX Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled		–	2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTT = 1.2V	–400	–	MGTAVTT	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTT = 1.2V	–	2/3 MGTAVTT	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage (1)	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage.	Equation based	MGTAVTT – DV_{PPOUT}/4			mV
R_{IN}	Differential input resistance			100		Ω
R_{OUT}	Differential output resistance			100		Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–		10	ps
C_{EXT}	Recommended external AC coupling capacitor (2)		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs Transceiver User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

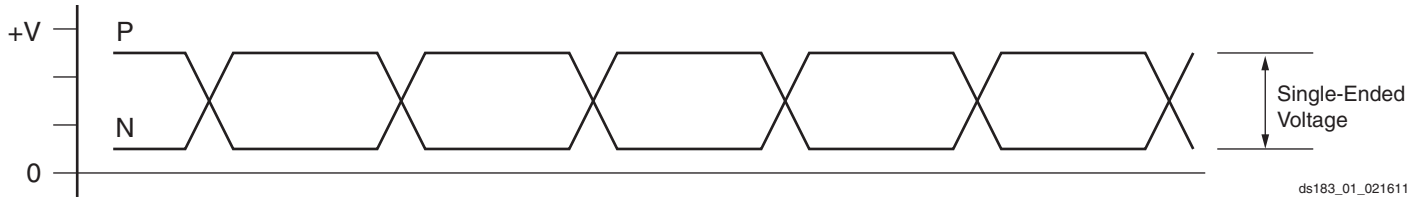

Figure 1: **Single-Ended Peak-to-Peak Voltage**

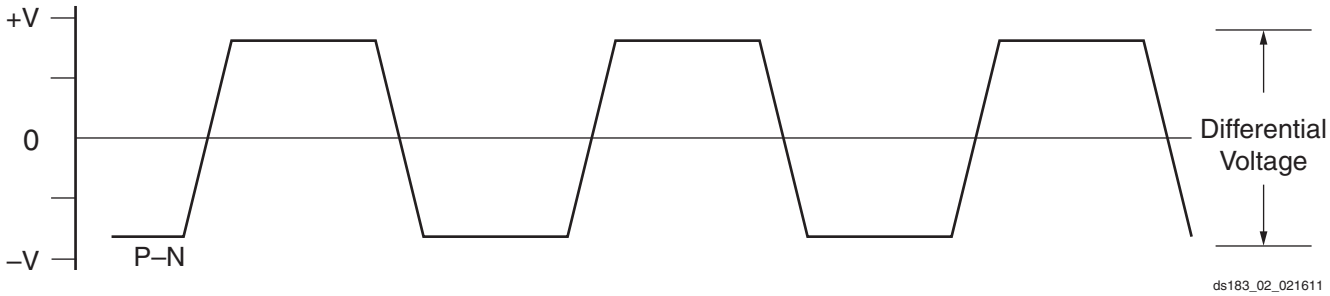

Figure 2: **Differential Peak-to-Peak Voltage**

Table 14 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *7 Series FPGAs Transceiver User Guide* for further details.

Table 14: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250		2000	mV
R_{IN}	Differential input resistance		100		Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult *7 Series FPGAs Transceiver User Guide* for further information.

Table 15: **GTX Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade				Units
			-3	-2	-1	-1L(1)	
F_{GTXMAX}(2)	Maximum GTX transceiver data rate		12.5	10.3125	6.6	6.6	Gb/s
F_{GTXMIN}(2)	Minimum GTX transceiver data rate		0.500	0.500	0.500	0.500	Gb/s
$F_{GTXCRANGE}$	CPLL line rate range	1	3.2–6.6				Gb/s
		2	1.6–3.3				Gb/s
		4	0.8–1.65				Gb/s
		8	0.5–0.825				Gb/s
		16	N/A				Gb/s
$F_{GTXQRANGE1}$	QPLL line rate range 1	1	5.93–8.0	5.93–8.0	5.93–6.6	5.93–6.6	Gb/s
		2	2.965–4.0	2.965–4.0	2.965–3.3	2.965–3.3	Gb/s
		4	1.4825–2.0	1.4825–2.0	1.4825–1.65	1.4825–1.65	Gb/s
		8	0.74125–1.0	0.74125–1.0	0.74125–0.825	0.74125–0.825	Gb/s
		16	N/A	N/A	N/A	N/A	Gb/s
$F_{GTXQRANGE2}$	QPLL line rate range 2	1	9.8–12.5	9.8–10.3125	N/A	N/A	Gb/s
		2	4.9–6.25	4.9–5.15625	N/A	N/A	Gb/s
		4	2.45–3.125	2.45–2.578125	N/A	N/A	Gb/s
		8	1.225–1.5625	1.225–1.2890625	N/A	N/A	Gb/s
		16	0.6125–0.78125	0.6125–0.64453125	N/A	N/A	Gb/s
$F_{GCPLLRANGE}$	GTX transceiver CPLL frequency range		1.6–3.3	1.6–3.3	1.6–3.3	1.6–3.3	GHz
$F_{GCPLLRANGE1}$	GTX transceiver QPLL frequency range 1		5.93–8.0	5.93–8.0	5.93–6.6	5.93–6.6	GHz
$F_{GCPLLRANGE2}$	GTX transceiver QPLL frequency range 2		9.8–12.5	9.8–10.3125	N/A	N/A	GHz

Notes:

1. The -1L speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s.
2. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.

Table 16: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	150	150	125	125	MHz

Table 17: **GTX Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	650	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–		ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–		µs

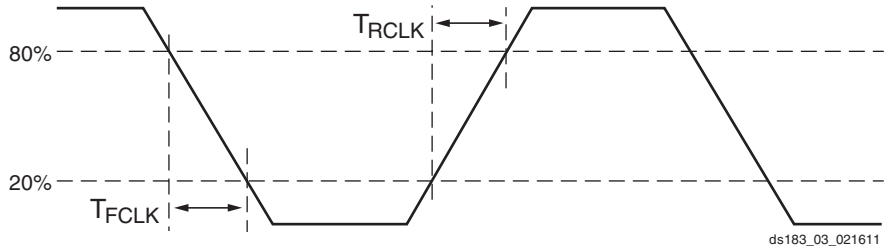

Figure 3: **Reference Clock Timing Parameters**

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 18: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$F_{PIPECLK}$	Pipe clock maximum frequency	250	250	250	250	MHz
$F_{USERCLK}$	User clock maximum frequency	500	500	250	250	MHz
$F_{USERCLK2}$	User clock 2 maximum frequency	250	250	250	250	MHz
F_{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

XADC Specifications

Table 19: **XADC Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 26 MHz, T_j = –40°C to 100°C, Typical values at T_j=+40°C						
ADC Accuracy(1)						
Resolution			12	–	–	Bits
Integral Nonlinearity	INL		–	–	±2	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Calibrated	–	–	±4	LSBs
Gain Error		Calibrated	–	–	±0.4	%
Channel Matching		Based on two individual ADC instances with calibration enabled	–	–	10	LSBs
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio	SNR	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion	THD	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	75	–	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs(2)						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T_j = –40°C to 100°C.	–	–	±4	°C
		T_j = –55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –40°C to +100°C	–	–	±1	%
		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –55°C to +125°C	–	–	±2	%
Conversion Rate(3)						
Conversion Time - Continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	cycle
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	cycle
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%

Table 19: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
XADC Reference(4)						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V
Power Requirements						
Analog Power Supply	V_{CCADC}		1.71	1.8	1.89	V
Analog Supply Current	I_{CCADC}	Analog circuits in powered up state	–	–	20	mA

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature.
2. See the ADC chapter in the *7 Series FPGAs XADC User Guide* for a detailed description.
3. See the Timing chapter in the *7 Series FPGAs XADC User Guide* for a detailed description.
4. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics, page 13. In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 20: **Networking Applications Interface Performances**

Description	I/O Bank Type	Speed Grade				Units
		-3	-2	-1	-1L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625		Mb/s
	HP	710	710	625		Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 10)	HR	1055	800	667		Mb/s
	HP	1600	1400	1250		Mb/s
SDR LVDS receiver (SFI-4.1)(1)	HR	710	710	625		Mb/s
	HP	710	710	625		Mb/s
DDR LVDS receiver (SPI-4.2)(1)	HR	1055	800	667		Mb/s
	HP	1600	1400	1250		Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 21: **Maximum Physical Interface (PHY) Rate for Memory Interfaces[1]**

Memory Standard	I/O Bank Type	V_{CCAUX_IO}	Speed Grade				Units
			-3	-2	-1	-1L	
DDR3	HP	2.0V	1866		1600		Mb/s
	HP	1.8V	1600	1333	1066		Mb/s
	HR	N/A	1066	1066	800		Mb/s
DDR3L	HP	2.0V			1333		Mb/s
	HP	1.8V	1333	1066	800		Mb/s
	HR	N/A	800	800	667		Mb/s
DDR2	HP	2.0V	800	800	800		Mb/s
	HP	1.8V					
	HR	N/A					
QDR II+	HP	2.0V	550	500	450		MHz
	HP	1.8V					
	HR	N/A	500	450	400		MHz
RLDRAM II	HP	2.0V	533	500	450		MHz
	HP	1.8V					
	HR	N/A					
RLDRAM III	HP	2.0V					MHz
	HP	1.8V					MHz
	HR	N/A	N/A				
LPDDR2	HP	2.0V					Mb/s
	HP	1.8V					Mb/s
	HR	N/A					Mb/s

Notes:

1. Advance performance numbers pending characterization on Xilinx memory platforms designed according to the guidelines in the *7 Series FPGAs Memory Interface Solutions User Guide*.

Switching Characteristics

All values represented in this data sheet are based on the advance speed specifications in ISE® software.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production
These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 22 correlates the current status of each Virtex-7 device on a per speed grade basis.

Table 22: **Virtex-7 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7V285T	-1L, -1, -2, -3		
XC7V450T	-1L, -1, -2, -3		
XC7V585T	-1L, -1, -2, -3		
XC7V855T	-1L, -1, -2, -3		
XC7V1500T	-1L, -1, -2		
XC7V2000T	-1L, -1, -2		
XC7VX485T	-1, -2, -3		

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-7 devices.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 23 lists the production released Virtex-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 23: **Virtex-7 Device Production Software and Speed Specification Release**

Device	Speed Grade Designations			
	-3	-2	-1	-1L
XC7V285T				
XC7V450T				
XC7V585T				
XC7V855T				
XC7V1500T	N/A			
XC7V2000T	N/A			
XC7VX485T				N/A

Notes:
1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

IOB Pad Input/Output/3-State Switching Characteristics

Table 24 (3.3V high-range IOB (HR)) and Table 25 (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 26 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 24: **3.3V IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDS_25(1)	0.61	0.66	0.74		1.19	1.27	1.40		1.19	1.27	1.40		ns
MINI_LVDS_25	0.61	0.65	0.72		1.19	1.27	1.40		1.19	1.27	1.40		ns
BLVDS_25(1)	0.61	0.67	0.76		1.64	1.80	2.04		1.64	1.80	2.04		ns
RSDS_25 (point to point)(1)	0.61	0.66	0.75		1.19	1.27	1.40		1.19	1.27	1.40		ns
PPDS_25(1)	0.63	0.68	0.76		1.17	1.27	1.42		1.17	1.27	1.42		ns
TMDS_33(1)	0.72	0.79	0.90		1.25	1.33	1.45		1.25	1.33	1.45		ns
PCI33_3(1)	1.32	1.44	1.62		2.52	2.78	3.18		2.52	2.78	3.18		ns
HSUL_12	0.56	0.60	0.65		1.99	2.25	2.66		1.99	2.25	2.66		ns
DIFF_HSUL_12	0.54	0.58	0.64		1.66	1.86	2.15		1.66	1.86	2.15		ns
HSTL_I_S	0.57	0.61	0.67		1.30	1.41	1.58		1.30	1.41	1.58		ns
HSTL_II_S	0.57	0.61	0.67		0.96	1.03	1.14		0.96	1.03	1.14		ns
HSTL_I_18_S	0.58	0.61	0.67		1.12	1.21	1.35		1.12	1.21	1.35		ns
HSTL_II_18_S	0.58	0.61	0.67		1.01	1.09	1.21		1.01	1.09	1.21		ns
DIFF_HSTL_I_S	0.61	0.65	0.70		1.21	1.30	1.45		1.21	1.30	1.44		ns
DIFF_HSTL_II_S	0.61	0.65	0.70		0.94	1.00	1.10		1.20	1.30	1.46		ns
DIFF_HSTL_I_18_S	0.62	0.66	0.73		1.07	1.15	1.27		1.23	1.32	1.46		ns
DIFF_HSTL_II_18_S	0.62	0.66	0.73		0.93	1.00	1.10		1.25	1.36	1.51		ns
HSTL_I_F	0.57	0.61	0.67		0.93	1.01	1.13		0.93	1.01	1.13		ns
HSTL_II_F	0.57	0.61	0.67		0.84	0.92	1.02		0.84	0.92	1.02		ns
HSTL_I_18_F	0.58	0.61	0.67		0.91	0.99	1.10		0.91	0.99	1.10		ns
HSTL_II_18_F	0.58	0.61	0.67		0.85	0.92	1.03		0.85	0.92	1.03		ns
DIFF_HSTL_I_F	0.61	0.65	0.70		0.88	0.96	1.06		1.21	1.30	1.44		ns
DIFF_HSTL_II_F	0.61	0.65	0.70		0.82	0.89	1.00		1.20	1.30	1.46		ns
DIFF_HSTL_I_18_F	0.62	0.66	0.73		0.88	0.95	1.06		1.23	1.32	1.46		ns
DIFF_HSTL_II_18_F	0.62	0.66	0.73		0.81	0.88	0.98		1.25	1.36	1.51		ns

Table 24: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVCMOS33, Slow, 4 mA	1.52	1.62	1.78		4.81	5.16	5.68		4.81	5.16	5.68		ns
LVCMOS33, Slow, 8 mA	1.52	1.62	1.78		4.08	4.47	5.05		4.08	4.47	5.05		ns
LVCMOS33, Slow, 12 mA	1.52	1.62	1.78		3.29	3.64	4.15		3.29	3.64	4.15		ns
LVCMOS33, Slow, 16 mA	1.52	1.62	1.78		2.82	3.15	3.65		2.82	315	3.65		ns
LVCMOS33, Fast, 4 mA	1.52	1.62	1.78		4.30	4.56	4.96		4.30	4.56	4.96		ns
LVCMOS33, Fast, 8 mA	1.52	1.62	1.78		3.66	3.91	4.29		3.66	3.91	4.29		ns
LVCMOS33, Fast, 12 mA	1.52	1.62	1.78		2.33	2.93	3.83		2.33	2.93	3.83		ns
LVCMOS33, Fast, 16 mA	1.52	1.62	1.78		2.22	2.44	2.79		2.22	2.44	2.79		ns
LVCMOS25, Slow, 4 mA	1.27	1.36	1.48		4.22	4.64	5.26		4.22	4.64	5.26		ns
LVCMOS25, Slow, 8 mA	1.27	1.36	1.48		3.31	3.69	4.25		3.31	3.69	4.25		ns
LVCMOS25, Slow, 12 mA	1.27	1.36	1.48		2.63	3.10	3.81		2.63	3.10	3.81		ns
LVCMOS25, Slow, 16 mA	1.27	1.36	1.48		3.01	3.38	3.94		3.01	3.38	3.94		ns
LVCMOS25, Fast, 4 mA	1.27	1.36	1.48		4.00	4.31	4.77		4.00	4.31	4.77		ns
LVCMOS25, Fast, 8 mA	1.27	1.36	1.48		2.33	2.80	3.51		2.33	2.80	3.51		ns
LVCMOS25, Fast, 12 mA	1.27	1.36	1.48		2.33	2.80	3.51		2.33	2.80	3.51		ns
LVCMOS25, Fast, 16 mA	1.27	1.36	1.48		1.86	2.16	2.60		1.86	2.16	2.60		ns
LVCMOS18, Slow, 4 mA	0.67	0.71	0.77		3.17	3.35	3.63		3.17	3.35	3.63		ns
LVCMOS18, Slow, 8 mA	0.67	0.71	0.77		2.49	2.79	3.25		2.49	2.79	3.25		ns
LVCMOS18, Slow, 12 mA	0.67	0.71	0.77		2.49	2.79	3.25		2.49	2.79	3.25		ns
LVCMOS18, Slow, 16 mA	0.67	0.71	0.77		1.72	1.94	2.25		1.72	1.94	2.25		ns
LVCMOS18, Slow, 24 mA(1)	0.67	0.71	0.77		1.60	1.77	2.01		1.60	1.77	2.01		ns
LVCMOS18, Fast, 4 mA	0.67	0.71	0.77		3.06	3.20	3.41		3.06	3.20	3.41		ns
LVCMOS18, Fast, 8 mA	0.67	0.71	0.77		1.81	2.10	2.53		1.81	2.10	2.53		ns
LVCMOS18, Fast, 12 mA	0.67	0.71	0.77		1.81	2.10	2.53		1.81	2.10	2.53		ns
LVCMOS18, Fast, 16 mA	0.67	0.71	0.77		1.37	1.52	1.74		1.37	1.52	1.74		ns
LVCMOS18, Fast, 24 mA(1)	0.67	0.71	0.77		1.16	1.27	1.43		1.16	1.27	1.43		ns
LVCMOS15, Slow, 4 mA	0.69	0.74	0.81		3.53	3.75	4.07		3.53	3.75	4.07		ns
LVCMOS15, Slow, 8 mA	0.69	0.74	0.81		2.14	2.43	2.87		2.14	2.43	2.87		ns
LVCMOS15, Slow, 12 mA	0.69	0.74	0.81		1.72	1.91	2.20		1.72	1.91	2.20		ns
LVCMOS15, Slow, 16 mA	0.69	0.74	0.81		1.63	1.81	2.07		1.63	1.81	2.07		ns
LVCMOS15, Fast, 4 mA	0.69	0.74	0.81		3.38	3.57	3.86		3.38	3.57	3.86		ns
LVCMOS15, Fast, 8 mA	0.69	0.74	0.81		1.59	1.80	2.12		1.59	1.80	2.12		ns
LVCMOS15, Fast, 12 mA	0.69	0.74	0.81		1.23	1.36	1.54		1.23	1.36	1.54		ns
LVCMOS15, Fast, 16 mA	0.69	0.74	0.81		1.21	1.32	1.50		1.21	1.32	1.50		ns
LVCMOS12, Slow, 4 mA	0.77	0.82	0.89		3.97	431	4.82		3.97	431	4.82		ns
LVCMOS12, Slow, 8 mA	0.77	0.82	0.89		2.71	3.12	3.74		2.71	3.12	3.74		ns
LVCMOS12, Slow, 12 mA(1)	0.77	0.82	0.89		1.99	2.25	2.66		1.99	2.25	2.66		ns
LVCMOS12, Fast, 4 mA	0.77	0.82	0.89		3.51	3.76	4.14		3.51	3.76	4.14		ns

Table 24: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVCMOS12, Fast, 8 mA	0.77	0.82	0.89		1.69	2.22	3.02		1.69	2.22	3.02		ns
LVCMOS12, Fast, 12 mA(1)	0.77	0.82	0.89		1.40	1.57	1.82		1.40	1.57	1.82		ns
SSTL135_S	0.57	0.60	0.64		0.96	1.03	1.14		0.96	1.03	1.14		ns
SSTL15_S	0.58	0.61	0.67		0.96	1.03	1.13		0.96	1.03	1.13		ns
SSTL18_I_S	0.58	0.61	0.67		1.34	1.45	1.62		1.34	1.45	1.62		ns
SSTL18_II_S	0.58	0.61	0.67		0.95	1.02	1.13		0.95	1.02	1.13		ns
DIFF_SSTL135_S	0.56	0.61	0.69		0.96	1.03	1.14		0.96	1.03	1.14		ns
DIFF_SSTL15_S	0.61	0.65	0.70		0.96	1.03	1.13		0.96	1.03	1.13		ns
DIFF_SSTL18_I_S	0.62	0.66	0.73		1.30	1.41	1.57		1.30	1.41	1.57		ns
DIFF_SSTL18_II_S	0.62	0.66	0.73		0.92	0.99	1.09		0.92	0.99	1.09		ns
SSTL135_F	0.57	0.60	0.64		0.85	0.93	1.04		0.85	0.93	1.04		ns
SSTL15_F	0.57	0.61	0.67		0.84	0.92	1.03		0.84	0.92	1.03		ns
SSTL18_I_F	0.58	0.61	0.67		0.93	1.01	1.12		0.93	1.01	1.12		ns
SSTL18_II_F	0.58	0.61	0.67		0.84	0.91	1.01		0.84	0.91	1.01		ns
DIFF_SSTL135_F	0.56	0.61	0.69		0.85	0.93	1.04		0.85	0.93	1.04		ns
DIFF_SSTL15_F	0.61	0.65	0.70		0.84	0.82	1.03		0.84	0.82	1.03		ns
DIFF_SSTL18_I_F	0.62	0.66	0.73		0.90	.097	1.08		0.90	.097	1.08		ns
DIFF_SSTL18_II_F	0.62	0.66	0.73		0.82	0.89	0.99		0.82	0.89	0.99		ns

Notes:

1. This I/O standard is only available in the 3.3V high-range (HR) banks.

Table 25: **1.8V IOB High Performance (HP) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDS	0.77	0.85	0.99		1.21	1.29	1.41		1.21	1.29	1.41		ns
HSUL_12	0.71	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
DIFF_HSUL_12	0.71	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
HSTL_I_S	0.74	0.83	0.96		1.21	1.30	1.44		1.21	1.30	1.44		ns
HSTL_II_S	0.74	0.83	0.96		1.20	1.31	1.46		1.20	1.31	1.46		ns
HSTL_III_S	0.74	0.83	0.96		1.18	1.28	1.43		1.18	1.28	1.43		ns
HSTL_I_18_S	0.74	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
HSTL_II_18_S	0.74	0.83	0.96		1.25	1.36	1.52		1.25	1.36	1.51		ns
HSTL_III_18_S	0.74	0.83	0.96		1.19	1.29	1.43		1.19	1.29	1.43		ns
HSTL_I_12_S	0.74	0.83	0.96		1.23	1.33	1.48		1.23	1.33	1.48		ns
HSTL_I_DCI_S	0.74	0.83	0.96		1.19	1.28	1.41		1.19	1.28	1.41		ns
HSTL_II_DCI_S	0.74	0.83	0.96		1.15	1.25	1.40		1.15	1.25	1.40		ns
HSTL_II_T_DCI_S	0.74	0.83	0.96		1.17	1.26	1.39		1.17	1.26	1.39		ns
HSTL_III_DCI_S	0.74	0.83	0.96		1.12	1.21	1.36		1.12	1.21	1.35		ns
HSTL_I_DCI_18_S	0.74	0.83	0.96		1.19	1.28	1.41		1.19	1.28	1.41		ns
HSTL_II_DCI_18_S	0.74	0.83	0.96		1.13	1.22	1.35		1.13	1.22	1.35		ns
HSTL_II _T_DCI_18_S	0.74	0.83	0.96		1.19	1.28	1.41		1.19	1.28	1.41		ns
HSTL_III_DCI_18_S	0.74	0.83	0.96		1.20	1.28	1.42		1.20	1.28	1.42		ns
DIFF_HSTL_I_S	0.77	0.85	0.99		1.21	1.30	1.44		1.21	1.30	1.44		ns
DIFF_HSTL_II_S	0.77	0.85	0.99		1.20	1.31	1.46		1.20	1.31	1.46		ns
DIFF_HSTL_I_DCI_S	0.77	0.85	0.99		1.17	1.26	1.39		1.17	1.26	1.39		ns
DIFF_HSTL_II_DCI_S	0.77	0.85	0.99		1.15	1.25	1.40		1.15	1.25	1.40		ns
DIFF_HSTL_I_18_S	0.77	0.85	0.99		1.23	1.32	1.46		1.23	1.32	1.46		ns
DIFF_HSTL_II_18_S	0.77	0.85	0.99		1.25	1.36	1.52		1.25	1.36	1.51		ns
DIFF_HSTL_I_DCI_18_S	0.77	0.85	0.99		1.19	1.28	1.41		1.19	1.28	1.41		ns
DIFF_HSTL_II_DCI_18_S	0.77	0.85	0.99		1.13	1.22	1.35		1.13	1.22	1.35		ns
DIFF_HSTL_II _T_DCI_18_S	0.77	0.85	0.99		1.19	1.28	1.41		1.19	1.28	1.41		ns
HSTL_I_F	0.74	0.83	0.96		1.21	1.30	1.44		1.21	1.30	1.44		ns
HSTL_II_F	0.74	0.83	0.96		1.20	1.31	1.46		1.20	1.30	1.46		ns
HSTL_III_F	0.74	0.83	0.96		1.18	1.28	1.43		1.18	1.28	1.43		ns
HSTL_I_18_F	0.74	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
HSTL_II_18_F	0.74	0.83	0.96		1.25	1.36	1.52		1.25	1.36	1.51		ns
HSTL_III_18_F	0.74	0.83	0.96		1.19	1.29	1.43		1.19	1.29	1.43		ns
HSTL_I_12_F	0.74	0.83	0.96		1.23	1.33	1.48		1.23	1.33	1.48		ns
HSTL_I_DCI_F	0.74	0.83	0.96		1.19	1.28	1.41		1.19	1.28	1.41		ns
HSTL_II_DCI_F	0.74	0.83	0.96		1.15	1.25	1.40		1.15	1.25	1.40		ns
HSTL_II_T_DCI_F	0.74	0.83	0.96		1.17	1.26	1.39		1.17	1.26	1.39		ns
HSTL_III_DCI_F	0.74	0.83	0.96		1.12	1.21	1.36		1.12	1.21	1.35		ns

Table 25: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
HSTL_I_DCI_18_F	0.74	0.83	0.96		1.19	1.28	1.41		1.19	1.28	1.41		ns
HSTL_II_DCI_18_F	0.74	0.83	0.96		1.13	1.22	1.35		1.13	1.22	1.35		ns
HSTL_II _T_DCI_18_F	0.74	0.83	0.96		1.19	1.28	1.41		1.19	1.28	1.41		ns
HSTL_III_DCI_18_F	0.74	0.83	0.96		1.20	1.28	1.42		1.20	1.28	1.42		ns
DIFF_HSTL_I_F	0.77	0.85	0.99		1.21	1.30	1.44		1.21	1.30	1.44		ns
DIFF_HSTL_II_F	0.77	0.85	0.99		1.20	1.31	1.46		1.20	1.31	1.46		ns
DIFF_HSTL_I_DCI_F	0.77	0.85	0.99		1.17	1.26	1.39		1.17	1.26	1.39		ns
DIFF_HSTL_II_DCI_F	0.77	0.85	0.99		1.15	1.25	1.40		1.15	1.25	1.40		ns
DIFF_HSTL_I_18_F	0.77	0.85	0.99		1.23	1.32	1.46		1.23	1.32	1.46		ns
DIFF_HSTL_II_18_F	0.77	0.85	0.99		1.25	1.36	1.52		1.25	1.36	1.51		ns
DIFF_HSTL_I_DCI_18_F	0.77	0.85	0.99		1.19	1.28	1.41		1.19	1.28	1.41		ns
DIFF_HSTL_II_DCI_18_F	0.77	0.85	0.99		1.13	1.22	1.35		1.13	1.22	1.35		ns
DIFF_HSTL_II _T_DCI_18_F	0.77	0.85	0.99		1.19	1.28	1.41		1.19	1.28	1.41		ns
LVCMOS18, Slow, 2 mA	0.50	0.56	0.65		3.52	3.74	4.07		3.52	3.74	4.07		ns
LVCMOS18, Slow, 4 mA	0.50	0.56	0.65		2.33	2.41	2.68		2.33	2.41	2.68		ns
LVCMOS18, Slow, 6 mA	0.50	0.56	0.65		1.92	2.04	2.20		1.92	2.03	2.20		ns
LVCMOS18, Slow, 8 mA	0.50	0.56	0.65		1.68	1.77	1.90		1.68	1.77	1.90		ns
LVCMOS18, Slow, 12 mA	0.50	0.56	0.65		1.57	1.66	1.79		1.57	1.66	1.79		ns
LVCMOS18, Slow, 16 mA	0.50	0.56	0.65		1.53	1.63	1.77		1.53	1.63	1.77		ns
LVCMOS18, Fast, 2 mA	0.50	0.56	0.65		3.34	3.53	3.82		3.34	3.53	3.82		ns
LVCMOS18, Fast, 4 mA	0.50	0.56	0.65		2.19	2.31	2.49		2.19	2.31	2.49		ns
LVCMOS18, Fast, 6 mA	0.50	0.56	0.65		1.80	1.90	2.06		1.80	1.90	2.06		ns
LVCMOS18, Fast, 8 mA	0.50	0.56	0.65		1.58	1.66	1.78		1.58	1.66	1.78		ns
LVCMOS18, Fast, 12 mA	0.50	0.56	0.65		1.41	1.51	1.65		1.41	1.51	1.65		ns
LVCMOS18, Fast, 16 mA	0.50	0.56	0.65		1.37	1.46	1.59		1.37	1.46	1.59		ns
LVCMOS15, Slow, 2 mA	0.58	0.66	0.77		2.86	3.16	3.59		2.86	3.16	3.59		ns
LVCMOS15, Slow, 4 mA	0.58	0.66	0.77		2.15	2.33	2.59		2.15	2.33	2.59		ns
LVCMOS15, Slow, 6 mA	0.58	0.66	0.77		1.74	1.94	2.24		1.74	1.94	2.24		ns
LVCMOS15, Slow, 8 mA	0.58	0.66	0.77		1.52	1.66	1.87		1.51	1.66	1.87		ns
LVCMOS15, Slow, 12 mA	0.58	0.66	0.77		1.47	1.60	1.79		1.47	1.60	1.79		ns
LVCMOS15, Slow, 16 mA	0.58	0.66	0.77		1.41	1.53	1.71		1.41	1.53	1.70		ns
LVCMOS15, Fast, 2 mA	0.58	0.66	0.77		2.87	3.16	3.58		2.87	3.16	3.58		ns
LVCMOS15, Fast, 4 mA	0.58	0.66	0.77		1.98	2.12	2.32		1.98	2.12	2.32		ns
LVCMOS15, Fast, 6 mA	0.58	0.66	0.77		1.51	1.71	2.02		1.51	1.71	2.02		ns
LVCMOS15, Fast, 8 mA	0.58	0.66	0.77		1.47	1.59	1.76		1.47	1.59	1.76		ns
LVCMOS15, Fast, 12 mA	0.58	0.66	0.77		1.37	1.48	1.64		1.37	1.48	1.64		ns
LVCMOS15, Fast, 16 mA	0.58	0.66	0.77		1.36	1.47	1.64		1.35	1.47	1.64		ns
LVCMOS12, Slow, 2 mA	0.66	0.73	0.84		2.63	2.83	3.13		2.63	2.83	3.13		ns

Table 25: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVCMOS12, Slow, 4 mA	0.66	0.73	0.84		2.03	2.20	2.45		2.03	2.20	2.45		ns
LVCMOS12, Slow, 6 mA	0.66	0.73	0.84		1.60	1.77	2.01		1.60	1.76	2.01		ns
LVCMOS12, Slow, 8 mA	0.66	0.73	0.84		1.56	1.69	1.88		1.56	1.69	1.88		ns
LVCMOS12, Fast, 2 mA	0.66	0.73	0.84		2.26	2.49	2.83		2.26	2.49	2.83		ns
LVCMOS12, Fast, 4 mA	0.66	0.73	0.84		1.61	1.81	2.10		1.61	1.81	2.10		ns
LVCMOS12, Fast, 6 mA	0.66	0.73	0.84		1.47	1.58	1.76		1.47	1.58	1.76		ns
LVCMOS12, Fast, 8 mA	0.66	0.73	0.84		1.41	1.52	1.69		1.41	1.52	1.69		ns
LVDCI_18	0.50	0.56	0.65		1.73	1.87	2.07		1.73	1.87	2.07		ns
LVDCI_15	0.58	0.66	0.77		1.55	1.68	1.87		1.55	1.68	1.87		ns
LVDCI_DV2_18	0.50	0.56	0.65		1.41	1.52	1.67		1.41	1.52	1.67		ns
LVDCI_DV2_15	0.58	0.66	0.77		1.40	1.48	1.59		1.40	1.48	1.59		ns
HSLVDCI_18	0.74	0.83	0.96		1.73	1.87	2.07		1.73	1.87	2.07		ns
HSLVDCI_15	0.74	0.83	0.96		1.55	1.68	1.87		1.55	1.68	1.87		ns
SSTL18_I_S	0.74	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
SSTL18_II_S	0.74	0.83	0.96		1.16	1.26	1.40		1.16	1.25	1.40		ns
SSTL18_I_DCI_S	0.74	0.83	0.96		1.17	1.26	1.39		1.17	1.26	1.39		ns
SSTL18_II_DCI_S	0.74	0.83	0.96		1.14	1.23	1.36		1.14	1.23	1.36		ns
SSTL18_II_T_DCI_S	0.74	0.83	0.96		1.17	1.26	1.39		1.17	1.26	1.39		ns
SSTL15_S	0.74	0.83	0.96		1.19	1.28	1.43		1.19	1.28	1.43		ns
SSTL15_DCI_S	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns
SSTL15_T_DCI_S	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns
SSTL135_S	0.74	0.83	0.96		1.19	1.28	1.43		1.19	1.28	1.43		ns
SSTL135_DCI_S	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns
SSTL135_T_DCI_S	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns
SSTL12_S	0.74	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
SSTL12_DCI_S	0.74	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
SSTL12_T_DCI_S	0.74	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
DIFF_SSTL18_I_S	0.77	0.85	0.99		1.23	1.32	1.46		1.23	1.32	1.46		ns
DIFF_SSTL18_II_S	0.77	0.85	0.99		1.16	1.26	1.40		1.16	1.26	1.40		ns
DIFF_SSTL18_I_DCI_S	0.77	0.85	0.99		1.17	1.26	1.39		1.17	1.26	1.39		ns
DIFF_SSTL18_II_DCI_S	0.77	0.85	0.99		1.14	1.23	1.36		1.14	1.23	1.36		ns
DIFF_SSTL18_II_T_DCI_S	0.77	0.85	0.99		1.17	1.26	1.39		1.17	1.26	1.39		ns
DIFF_SSTL15_S	0.74	0.83	0.96		1.19	1.28	1.43		1.19	1.28	1.43		ns
DIFF_SSTL15_DCI_S	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns
DIFF_SSTL15_T_DCI_S	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns
DIFF_SSTL135_S	0.74	0.83	0.96		1.19	1.28	1.43		1.19	1.28	1.43		ns
DIFF_SSTL135_DCI_S	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns
DIFF_SSTL135_T_DCI_S	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns

Table 25: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
DIFF_SSTL12_S	0.71	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
DIFF_SSTL12_DCI_S	0.71	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
DIFF_SSTL12_T_DCI_S	0.71	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
SSTL18_I_F	0.74	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
SSTL18_II_F	0.74	0.83	0.96		1.16	1.26	1.40		1.16	1.26	1.40		ns
SSTL18_I_DCI_F	0.74	0.83	0.96		1.17	1.26	1.39		1.17	1.26	1.39		ns
SSTL18_II_DCI_F	0.74	0.83	0.96		1.14	1.23	1.36		1.14	1.23	1.36		ns
SSTL18_II_T_DCI_F	0.74	0.83	0.96		1.17	1.26	1.39		1.17	1.26	1.39		ns
SSTL15_F	0.74	0.83	0.96		1.19	1.28	1.43		1.19	1.28	1.43		ns
SSTL15_DCI_F	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns
SSTL15_T_DCI_F	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns
SSTL135_F	0.74	0.83	0.96		1.19	1.28	1.43		1.19	1.28	1.43		ns
SSTL135_DCI_F	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns
SSTL135_T_DCI_F	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns
SSTL12_F	0.71	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
SSTL12_DCI_F	0.71	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
SSTL12_T_DCI_F	0.71	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
DIFF_SSTL18_I_F	0.77	0.85	0.99		1.23	1.32	1.46		1.23	1.32	1.46		ns
DIFF_SSTL18_II_F	0.77	0.85	0.99		1.16	1.26	1.40		1.16	1.25	1.40		ns
DIFF_SSTL18_I_DCI_F	0.77	0.85	0.99		1.17	1.26	1.39		1.17	1.26	1.39		ns
DIFF_SSTL18_II_DCI_F	0.77	0.85	0.99		1.14	1.23	1.36		1.14	1.23	1.36		ns
DIFF_SSTL18_II_T_DCI_F	0.77	0.85	0.99		1.17	1.26	1.39		1.17	1.26	1.39		ns
DIFF_SSTL15_F	0.74	0.83	0.96		1.19	1.28	1.43		1.19	1.28	1.43		ns
DIFF_SSTL15_DCI_F	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns
DIFF_SSTL15_T_DCI_F	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns
DIFF_SSTL135_F	0.74	0.83	0.96		1.19	1.28	1.43		1.19	1.28	1.43		ns
DIFF_SSTL135_DCI_F	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns
DIFF_SSTL135_T_DCI_F	0.74	0.83	0.96		1.18	1.27	1.40		1.18	1.27	1.40		ns
DIFF_SSTL12_F	0.71	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
DIFF_SSTL12_DCI_F	0.71	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns
DIFF_SSTL12_T_DCI_F	0.71	0.83	0.96		1.23	1.32	1.46		1.23	1.32	1.46		ns

Notes:

1. This I/O standard is only available in the 1.8V high-performance (HP) banks.

Table 26: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{IOTPHZ}	T input to Pad high-impedance	2.03	2.17	2.38		ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 27 shows the test setup parameters used for measuring input delay.

Table 27: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(5)	V_{REF} (1)(3)(5)
LVTTL	LVTTL	0	3.3	1.65	–
LVCMOS, 3.3V	LVCMOS33	0	3.3	1.65	–
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
SSTL (Stub Terminated Transceiver Logic), 1.5V and 1.35V	SSTL15, SSTL135	V_{REF} – 1.00	V_{REF} + 1.00	V_{REF}	0.75, 0.675
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), HR I/O Banks	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
LVDS (Low-Voltage Differential Signaling), HP I/O Banks	LVDS	1.2 – 0.125	1.2 + 0.125	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 4.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 4 and Figure 5.

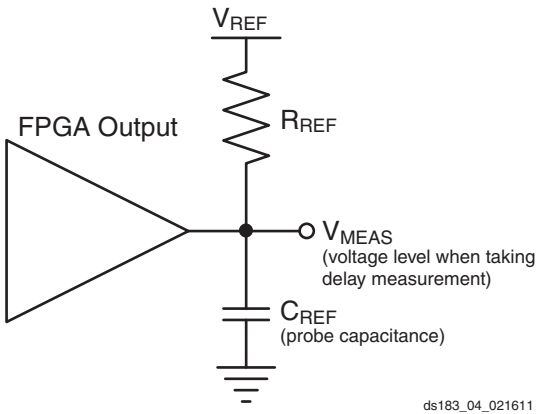

Figure 4: **Single Ended Test Setup**

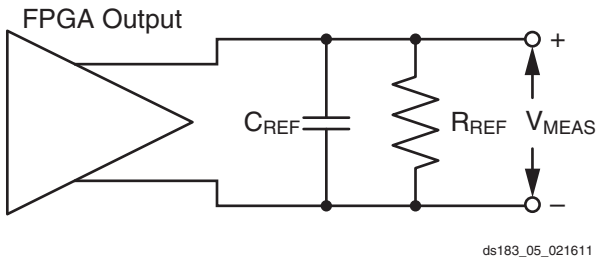

Figure 5: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 28.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 28: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL15	SSTL15	50	0	V_{REF}	0.75
SSTL135	SSTL135	50	0	V_{REF}	0.675
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	100	0	0[2]	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0

Table 28: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL15, with DCI	SSTL15_DCI	50	0	V_{REF}	0.675
SSTL135, with DCI	SSTL135_DCI	50	0	V_{REF}	0.75

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 29: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold						
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.31/ 0.05	0.36/ 0.06	0.44/ 0.07		ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	1.00/ –0.14	1.15/ –0.14	1.39/ –0.14		ns
$T_{IDOCKE2}/T_{IOCKDE2}$	D pin Setup/Hold with respect to CLK without Delay (HP I/O banks only)	0.11/ 0.38	0.13/ 0.42	0.15/ 0.49		ns
$T_{IDOCKDE2}/T_{IOCKDDE2}$	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HP I/O banks only)	0.14/ 0.29	0.17/ 0.32	0.20/ 0.37		ns
$T_{IDOCKE3}/T_{IOCKDE3}$	D pin Setup/Hold with respect to CLK without Delay (HR I/O banks only)	0.11/ 0.38	0.13/ 0.42	0.15/ 0.49		ns
$T_{IDOCKDE3}/T_{IOCKDDE3}$	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HR I/O banks only)	0.14/ 0.29	0.17/ 0.32	0.20/ 0.37		ns
Combinatorial						
T_{IDIE2}	D pin to O pin propagation delay, no Delay (HP I/O banks only)	0.19	0.21	0.24		ns
T_{IDIDE2}	DDLY pin to O pin propagation delay (using IDELAY) (HP I/O banks only)	0.22	0.24	0.28		ns
T_{IDIE3}	D pin to O pin propagation delay, no Delay (HR I/O banks only)	0.19	0.21	0.24		ns
T_{IDIDE3}	DDLY pin to O pin propagation delay (using IDELAY) (HR I/O banks only)	0.22	0.24	0.28		ns
Sequential Delays						
T_{IDLOE2}	D pin to Q1 pin using flip-flop as a latch without Delay (HP I/O banks only)	0.48	0.54	0.62		ns
$T_{IDLODE2}$	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only)	0.51	0.57	0.66		ns
T_{IDLOE3}	D pin to Q1 pin using flip-flop as a latch without Delay (HR I/O banks only)	0.48	0.54	0.62		ns
$T_{IDLODE3}$	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only)	0.51	0.57	0.66		ns
T_{ICKQ}	CLK to Q outputs	0.55	0.61	0.70		ns

Table 29: **ILOGIC Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{RQ\_ILOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	1.12	1.29	1.54		ns
$T_{GSRQ\_ILOGICE2}$	Global Set/Reset to Q outputs (HP I/O banks only)	7.67	7.67	10.61		ns
$T_{RQ\_ILOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	1.12	1.29	1.54		ns
$T_{GSRQ\_ILOGICE3}$	Global Set/Reset to Q outputs (HR I/O banks only)	7.67	7.67	10.61		ns
Set/Reset						
$T_{RPW\_ILOGICE2}$	Minimum Pulse Width, SR inputs (HP I/O banks only)	0.63	0.66	0.71		ns, Min
$T_{RPW\_ILOGICE3}$	Minimum Pulse Width, SR inputs (HR I/O banks only)	0.82	1.00	1.26		ns, Min

Table 30: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold						
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.55/ –0.22	0.61/ –0.22	0.71/ –0.22		ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.13/ –0.06	0.15/ –0.06	0.18/ –0.06		ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.54/ –0.20	0.64/ –0.20	0.79/ –0.20		ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.53/ –0.21	0.59/ –0.21	0.69/ –0.21		ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.12/ –0.05	0.14/ –0.05	0.17/ –0.05		ns
Combinatorial						
T_{ODQ}	D1 to OQ out or T1 to TQ out	0.78	0.88	1.03		ns
Sequential Delays						
T_{OCKQ}	CLK to OQ/TQ out	0.31	0.35	0.41		ns
$T_{RQ\_OLOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	0.56	0.64	0.76		ns
$T_{GSRQ\_OLOGICE2}$	Global Set/Reset to Q outputs (HP I/O banks only)	7.67	7.67	10.61		ns
$T_{RQ\_OLOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	0.56	0.64	0.76		ns
$T_{GSRQ\_OLOGICE3}$	Global Set/Reset to Q outputs (HR I/O banks only)	7.67	7.67	10.61		ns
Set/Reset						
$T_{RPW\_OLOGICE2}$	Minimum Pulse Width, SR inputs (HP I/O banks only)	0.63	0.66	0.71		ns, Min
$T_{RPW\_OLOGICE3}$	Minimum Pulse Width, SR inputs (HR I/O banks only)	0.82	1.00	1.26		ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 31: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold for Control Lines						
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.13/ 0.11	0.15/ 0.12	0.18/ 0.15		ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin Setup/Hold with respect to CLK (for CE1)	0.22/ –0.04	0.26/ –0.04	0.32/ –0.04		ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)	0.06/ 0.14	0.06/ 0.15	0.07/ 0.18		ns
Setup/Hold for Data Lines						
T_{ISDCK_D} /T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.02/ 0.12	0.03/ 0.14	0.03/ 0.17		ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IDELAY)(1)	0.05/ 0.09	0.06/ 0.10	0.08/ 0.12		ns
$T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	0.02/ 0.12	0.03/ 0.14	0.03/ 0.17		ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IDELAY)(1)	0.05/ 0.09	0.06/ 0.10	0.08/ 0.12		ns
Sequential Delays						
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.59	0.66	0.76		ns
Propagation Delays						
T_{ISDO_DO}	D input to DO output pin	0.22	0.24	0.28		ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 32: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.48/ –0.21	0.54/ –0.21	0.63/ –0.21		ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	0.53/ –0.22	0.59/ –0.22	0.69/ –0.22		ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input Setup/Hold with respect to CLKDIV	0.48/ –0.22	0.56/ –0.22	0.68/ –0.22		ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input Setup/Hold with respect to CLK	0.13/ –0.06	0.15/ –0.06	0.18/ –0.06		ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.72	0.82	0.98		ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input Setup/Hold with respect to CLK	0.12/ –0.05	0.14/ –0.05	0.17/ –0.05		ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.28	0.32	0.37		ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.28	0.32	0.37		ns
Combinatorial						
T_{OSDO_TTQ}	T input to TQ Out	0.78	0.88	1.03		ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Input/Output Delay Switching Characteristics

Table 33: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
IDELAYCTRL						
T_{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.25	3.25	3.25		µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.0(1)	200	200	200		MHz
	Attribute REFCLK frequency = 300.0(1)	300	300	N/A		MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10		MHz
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width	52.5	52.5	52.5		ns
IDELAY/ODELAY						
$T_{IDELAYRESOLUTION}$	IDELAY/ODELAY chain delay resolution	1/(32 x 2 x F_{REF})				ps
$T_{IDELAYPAT\_JIT\_CLOCK}$	Pattern dependent period jitter in delay chain for clock pattern. (HP I/O banks only)(2)	0	0	0		ps per tap
$T_{IDELAYPAT\_JIT\_DATA}$	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) (HP I/O banks only)(2)	±5	±5	±5		ps per tap
$T_{IDELAYPAT\_JIT\_CLOCK}$	Pattern dependent period jitter in delay chain for clock pattern. (HR I/O banks only)(2)	0	0	0		ps per tap
$T_{IDELAYPAT\_JIT\_DATA}$	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) (HR I/O banks only)(2)	±9	±9	±9		ps per tap
$T_{IDELAY\_CLK\_MAX}$/ $T_{ODELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY/ODELAY	920	920	816.5		MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin Setup/Hold with respect to C for IDELAY	–0.02/ 0.21	–0.02/ 0.24	–0.02/ 0.30		ns
T_{ODCCK_CE} / T_{ODCKC_CE}	CE pin Setup/Hold with respect to C for ODELAY	–0.02/ 0.21	–0.02/ 0.25	–0.02/ 0.30		ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin Setup/Hold with respect to C for IDELAY	0.10/ 0.24	0.11/ 0.28	0.12/ 0.34		ns
T_{ODCCK_INC}/ T_{ODCKC_INC}	INC pin Setup/Hold with respect to C for ODELAY	0.11/ 0.24	0.11/ 0.28	0.12/ 0.34		ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin Setup/Hold with respect to C for IDELAY	0.10/ 0.26	0.12/ 0.31	0.14/ 0.38		ns
T_{ODCCK_RST}/ T_{ODCKC_RST}	RST pin Setup/Hold with respect to C for ODELAY	0.10/ 0.27	0.12/ 0.32	0.15/ 0.38		ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY	Note 2	Note 2	Note 2		ps
$T_{ODDO\_ODATAIN}$	Propagation delay through ODELAY	Note 2	Note 2	Note 2		ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. Delay depends on IDELAY/ODELAY tap setting. See TRACE report for actual values.

CLB Switching Characteristics

Table 34: **CLB Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Combinatorial Delays						
T_{ILO}	An – Dn LUT address to A	0.05	0.06	0.07		ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.17	0.19	0.23		ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A	0.25	0.28	0.35		ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.57	0.65	0.80		ns, Max
T_{AXA}	AX inputs to AMUX output	0.32	0.37	0.46		ns, Max
T_{AXB}	AX inputs to BMUX output	0.35	0.40	0.50		ns, Max
T_{AXC}	AX inputs to CMUX output	0.35	0.40	0.50		ns, Max
T_{AXD}	AX inputs to DMUX output	0.40	0.45	0.54		ns, Max
T_{BXB}	BX inputs to BMUX output	0.29	0.33	0.41		ns, Max
T_{BXD}	BX inputs to DMUX output	0.37	0.41	0.49		ns, Max
T_{CXC}	CX inputs to CMUX output	0.24	0.26	0.31		ns, Max
T_{CXD}	CX inputs to DMUX output	0.32	0.35	0.42		ns, Max
T_{DXD}	DX inputs to DMUX output	0.30	0.34	0.41		ns, Max
T_{OPCYA}	An input to COUT output	0.31	0.35	0.43		ns, Max
T_{OPCYB}	Bn input to COUT output	0.31	0.35	0.44		ns, Max
T_{OPCYC}	Cn input to COUT output	0.24	0.27	0.33		ns, Max
T_{OPCYD}	Dn input to COUT output	0.22	0.26	0.32		ns, Max
T_{AXCY}	AX input to COUT output	0.26	0.29	0.34		ns, Max
T_{BXCY}	BX input to COUT output	0.22	0.25	0.30		ns, Max
T_{CXCY}	CX input to COUT output	0.17	0.19	0.22		ns, Max
T_{DXCY}	DX input to COUT output	0.16	0.18	0.22		ns, Max
T_{BYP}	CIN input to COUT output	0.06	0.06	0.07		ns, Max
T_{CINA}	CIN input to AMUX output	0.22	0.25	0.30		ns, Max
T_{CINB}	CIN input to BMUX output	0.23	0.26	0.32		ns, Max
T_{CINC}	CIN input to CMUX output	0.22	0.24	0.29		ns, Max
T_{CIND}	CIN input to DMUX output	0.24	0.27	0.33		ns, Max
Sequential Delays						
T_{CKO}	Clock to AQ – DQ outputs	0.27	0.30	0.36		ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.31	0.35	0.42		ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{DICK}/T_{CKDI}	A – D input to CLK on A – D Flip Flops	0.35/ 0.14	0.40/ 0.15	0.51/ 0.19		ns, Min
T_{CECK_CLB}/ T_{CKCE_CLB}	CE input to CLK on A – D Flip Flops	0.12/ 0.00	0.14/ 0.00	0.16/ 0.00		ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D Flip Flops	0.32/ 0.02	0.37/ 0.02	0.44/ 0.03		ns, Min
T_{CINCK}/T_{CKCIN}	CIN input to CLK on A – D Flip Flops	0.15/ 0.14	0.18/ 0.15	0.24/ 0.19		ns, Min

Table 34: **CLB Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Set/Reset						
T_{SRMIN}	SR input minimum pulse width	0.50	0.75	1.00		ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.40	0.45	0.53		ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.37	0.41	0.50		ns, Max
F_{TOG}	Toggle frequency (for export control)	1412	1286	1098		MHz

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 35: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Sequential Delays						
T_{SHCKO}	Clock to A – B outputs	0.72	0.81	0.99		ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	0.97	1.09	1.33		ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS_LRAM}/T_{DH_LRAM}	A – D inputs to CLK	0.47/ 0.24	0.52/ 0.26	0.62/ 0.30		ns, Min
T_{AS_LRAM}/T_{AH_LRAM}	Address An inputs to clock	0.15/ 0.51	0.17/ 0.55	0.22/ 0.62		ns, Min
T_{WS_LRAM}/T_{WH_LRAM}	WE input to clock	0.32/ 0.08	0.36/ 0.08	0.45/ 0.09		ns, Min
T_{CECK_LRAM}/ T_{CKCE_LRAM}	CE input to CLK	0.33/ 0.08	0.37/ 0.08	0.46/ 0.09		ns, Min
Clock CLK						
T_{MPW_LRAM}	Minimum pulse width	0.73	0.86	1.09		ns, Min
T_{MCP}	Minimum clock period	1.46	1.71	2.18		ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 36: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	0.92	1.03	1.26		ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.18	1.32	1.61		ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	0.82	0.92	1.13		ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS_SHFREG}/ T_{WH_SHFREG}	WE input	0.29/ 0.08	0.33/ 0.08	0.41/ 0.09		ns, Min
T_{CECK_SHFREG}/ T_{CKCE_SHFREG}	CE input to CLK	0.30/ 0.08	0.34/ 0.08	0.42/ 0.09		ns, Min
T_{DS_SHFREG}/ T_{DH_SHFREG}	A – D inputs to CLK	0.29/ 0.28	0.32/ 0.30	0.39/ 0.35		ns, Min
Clock CLK						
T_{MPW_SHFREG}	Minimum pulse width	0.63	0.73	0.93		ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Block RAM and FIFO Switching Characteristics

Table 37: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$ (1)	Clock CLK to DOUT output (without output register) (2)(3)	1.83	2.03	2.34		ns, Max
	Clock CLK to DOUT output (with output register) (4)(5)	0.56	0.62	0.71		ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register) (2)(3)	2.38	2.74	3.27		ns, Max
	Clock CLK to DOUT output with ECC (with output register) (4)(5)	0.58	0.65	0.76		ns, Max
$T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$	Clock CLK to DOUT output with Cascade (without output register) (2)	2.18	2.46	2.88		ns, Max
	Clock CLK to DOUT output with Cascade (with output register) (4)	1.01	1.12	1.29		ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs (6)	0.69	0.75	0.84		ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs (7)	0.79	0.86	0.97		ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.66	0.72	0.81		ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (without output register)	2.20	2.53	3.03		ns, Max
	Clock CLK to BITERR (with output register)	0.54	0.60	0.70		ns, Max

Table 37: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.64	0.70	0.80		ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.69	0.77	0.88		ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCCK\_ADDRA}/T_{RCKC\_ADDRA}$	ADDR inputs(8)	0.37/ 0.21	0.40/ 0.23	0.45/ 0.25		ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs(9)	0.87/ 0.22	0.99/ 0.23	1.18/ 0.24		ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode(9)	0.35/ 0.22	0.41/ 0.23	0.52/ 0.24		ns, Min
	DIN inputs with block RAM ECC encode only(9)	0.76/ 0.22	0.88/ 0.23	1.05/ 0.24		ns, Min
	DIN inputs with FIFO ECC in standard mode(9)	0.87/ 0.22	0.99/ 0.23	1.18/ 0.24		ns, Min
$T_{RCCK\_CLK}/T_{RCKC\_CLK}$	Inject single/double bit error in ECC mode	0.51/ 0.17	0.58/ 0.18	0.68/ 0.18		ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	Block RAM Enable (EN) input	0.36/ 0.18	0.39/ 0.19	0.44/ 0.21		ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.32/ 0.05	0.34/ 0.06	0.39/ 0.06		ns, Min
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	Synchronous RSTREG input(10)	0.37/ 0.04	0.40/ 0.04	0.45/ 0.04		ns, Min
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.24/ 0.14	0.25/ 0.15	0.27/ 0.16		ns, Min
$T_{RCCK\_WEA}/T_{RCKC\_WEA}$	Write Enable (WE) input (Block RAM only)	0.39/ 0.15	0.43/ 0.16	0.49/ 0.17		ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.46/ 0.18	0.51/ 0.19	0.59/ 0.21		ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.42/ 0.18	0.49/ 0.19	0.59/ 0.21		ns, Min
Reset Delays (Flags)						
T_{RCO_RST}	Reset RST to FIFO Flags/Pointers(11)	0.76	0.83	0.94		ns, Max
Maximum Frequency						
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (Write first and No change modes) When not in SDP RF mode	601	544	458		MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (Read first, Performance mode) When in SDP RF mode but no address overlap between port A and port B	601	544	458		MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (Read first, Delayed_write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses	541	485	401		MHz

Table 37: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$F_{MAX\_CAS\_WF\_NC}$	Block RAM Cascade (Write first, No change mode) When cascade but not in RF mode	529	475	392		MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM Cascade (Read first, Performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled	529	475	392		MHz
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B	492	437	353		MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	601	544	458		MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	495	427	326		MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
10. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).
11. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.

DSP48E1 Switching Characteristics

Table 38: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed				Units
		-3	-2	-1	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
$T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$	A input to A register CLK	0.31/ 0.10	0.37/ 0.11	0.51/ 0.16		ns
$T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$	B input to B register CLK	0.36/ 0.11	0.42/ 0.12	0.57/ 0.17		ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.24/ 0.15	0.28/ 0.16	0.40/ 0.22		ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.29/ 0.14	0.35/ 0.15	0.50/ 0.20		ns
$T_{DSPDCK\_ACIN\_AREG}$/$T_{DSPCKD\_ACIN\_AREG}$	ACIN input to A register CLK	0.28/ 0.10	0.34/ 0.11	0.47/ 0.16		ns
$T_{DSPDCK\_BCIN\_BREG}$/$T_{DSPCKD\_BCIN\_BREG}$	BCIN input to B register CLK	0.30/ 0.11	0.35/ 0.12	0.48/ 0.17		ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
$T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_B\_MREG\_MULT}$	{A, B,} input to M register CLK using multiplier	2.43/ –0.03	2.81/ –0.03	3.61/ –0.01		ns
$T_{DSPDCK\_\{A, B\}\_ADREG}$/ $T_{DSPCKD\_ D\_ADREG}$	{A, D} input to AD register CLK	1.28/ –0.04	1.46/ –0.04	1.85/ –0.03		ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
$T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\} \_PREG\_MULT}$	{A, B,} input to P register CLK using multiplier	3.97/ –0.16	4.57/ –0.16	5.78/ –0.16		ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK using multiplier	3.87/ –0.56	4.48/ –0.56	5.69/ –0.56		ns
$T_{DSPDCK\_B\_PREG}$/ $T_{DSPCKD\_B\_PREG}$	B input to P register CLK not using multiplier	1.70/ –0.16	1.94/ –0.16	2.45/ –0.16		ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK not using multiplier	1.50/ –0.13	1.72/ –0.13	2.18/ –0.13		ns
$T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$	PCIN input to P register CLK	1.30/ –0.04	1.48/ –0.04	1.87/ –0.03		ns
Setup and Hold Times of the CE Pins						
$T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.38/ 0.08	0.46/ 0.09	0.62/ 0.13		ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.31/ 0.09	0.38/ 0.10	0.51/ 0.14		ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.40/ –0.03	0.47/ –0.03	0.63/ –0.02		ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.31/ 0.06	0.37/ 0.07	0.51/ 0.10		ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.36/ 0.02	0.43/ 0.02	0.58/ 0.05		ns
Setup and Hold Times of the RST Pins						
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.42/ 0.11	0.49/ 0.12	0.63/ 0.16		ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.10/ 0.08	0.12/ 0.09	0.17/ 0.13		ns

Table 38: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed				Units
		-3	-2	-1	-1L	
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.47/ 0.07	0.55/ 0.08	0.71/ 0.12		ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.37/ 0.08	0.43/ 0.09	0.55/ 0.12		ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.26/ 0.02	0.30/ 0.03	0.39/ 0.05		ns
Combinatorial Delays from Input Pins to Output Pins						
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier	3.75	4.32	5.46		ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier	3.67	4.25	5.40		ns
$T_{DSPDO\_B\_P}$	B input to P output not using multiplier	1.50	1.72	2.16		ns
$T_{DSPDO\_C\_P}$	C input to P output	1.30	1.50	1.89		ns
Combinatorial Delays from Input Pins to Cascading Output Pins						
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.54	0.62	0.79		ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier	3.99	4.60	5.81		ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier	3.90	4.51	5.72		ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.72	1.98	2.48		ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output	1.52	1.75	2.21		ns
Combinatorial Delays from Cascading Input Pins to All Output Pins						
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier	3.58	4.13	5.23		ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier	1.31	1.51	1.91		ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output	0.35	0.41	0.53		ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier	3.81	4.39	5.55		ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier	1.54	1.77	2.23		ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output	1.10	1.26	1.57		ns
$T_{DSPDO\_PCIN\_CARRYCASCOUT}$	PCIN input to CARRYCASCOUT output	1.32	1.51	1.90		ns
Clock to Outs from Output Register Clock to Output Pins						
$T_{DSPCKO\_P\_PREG}$	CLK (PREG) to P output	0.29	0.33	0.42		ns
$T_{DSPCKO\_CARRYCASCOUT\_PREG}$	CLK (PREG) to CARRYCASCOUT output	0.48	0.54	0.68		ns
Clock to Outs from Pipeline Register Clock to Output Pins						
$T_{DSPCKO\_P\_MREG}$	CLK (MREG) to P output	1.58	1.82	2.30		ns
$T_{DSPCKO\_CARRYCASCOUT\_MREG}$	CLK (MREG) to CARRYCASCOUT output	1.80	2.07	2.62		ns
$T_{DSPCKO\_P\_ADREG\_MULT}$	CLK (ADREG) to P output using multiplier	2.68	3.09	3.91		ns
$T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$	CLK (ADREG) to CARRYCASCOUT output using multiplier	2.91	3.35	4.23		ns

Table 38: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed				Units
		-3	-2	-1	-1L	
Clock to Outs from Input Register Clock to Output Pins						
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK (AREG) to P output using multiplier	3.87	4.46	5.63		ns
$T_{DSPCKO\_P\_BREG}$	CLK (BREG) to P output not using multiplier	1.58	1.81	2.26		ns
$T_{DSPCKO\_P\_CREG}$	CLK (CREG) to P output not using multiplier	1.62	1.85	2.32		ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK (DREG) to P output using multiplier	3.84	4.45	5.64		ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
$T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.61	0.70	0.89		ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	4.10	4.72	5.95		ns
$T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$	CLK (BREG) to CARRYCASCOUT output not using multiplier	1.80	2.06	2.59		ns
$T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$	CLK (DREG) to CARRYCASCOUT output using multiplier	4.07	4.70	5.97		ns
$T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$	CLK (CREG) to CARRYCASCOUT output	1.84	2.11	2.64		ns
Maximum Frequency						
F_{MAX}	With all registers used	617	533	419		MHz
F_{MAX_PATDET}	With pattern detector	533	461	363		MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	350	304	241		MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	321	279	221		MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	399	345	272		MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	399	345	272		MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	263	228	181		MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	246	214	169		MHz

Configuration Switching Characteristics

Table 39: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Power-up Timing Characteristics						
T_{PL}[1]	Program Latency					ms, Max
T_{POR}[1]	Power-on-Reset			50		ms, Max
T_{ICCK}	CCLK (output) delay					ns, Min
$T_{PROGRAM}$	Program Pulse Width			250		ns, Min
Master/Slave Serial Mode Programming Switching						
T_{DCCK}/T_{CCKD}	DIN Setup/Hold, slave mode			5.0/0.0		ns, Min
T_{DSCCK}/T_{SCCKD}	DIN Setup/Hold, master mode			5.0/0.0		ns, Min
T_{CCO}	DOUT at 3.3V					ns, Max
	DOUT at 2.5V					ns, Max
	DOUT at 1.8V					ns, Max
F_{MCCK}	Maximum Frequency, master mode with respect to nominal CCLK.			100		MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode with respect to nominal CCLK.			±55		%
F_{MSCCK}	Slave mode external CCLK			100		MHz
SelectMAP Mode Programming Switching						
T_{SMDCCK}/T_{SMCCKD}	SelectMAP Data Setup/Hold			5.0/0.0		ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold					ns, Min
T_{SMCCKW}/T_{SMWCCK}	RDWR_B Setup/Hold					ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)					ns, Max
T_{SMCO}	CCLK to DATA out in readback at 3.3V					ns, Max
	CCLK to DATA out in readback at 2.5V					ns, Max
	CCLK to DATA out in readback at 1.8V					ns, Max
F_{SMCCK}	Maximum Frequency with respect to nominal CCLK.			100		MHz, Max
F_{RBCCK}	Maximum Readback Frequency with respect to nominal CCLK			70		MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance with respect to nominal CCLK.			±55		%
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI Setup time before TCK/ Hold time after TCK					ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid at 3.3V					ns, Max
	TCK falling edge to TDO output valid at 2.5V					ns, Max
	TCK falling edge to TDO output valid at 1.8V					ns, Max
F_{TCK}	Maximum configuration TCK clock frequency			20		MHz, Max
F_{TCKB}	Maximum boundary-scan TCK clock frequency			20		MHz, Max

Table 39: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
BPI Master Flash Mode Programming Switching						
T_{BPICCO}[2]	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B outputs valid after CCLK rising edge at 3.3V					ns
	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B outputs valid after CCLK rising edge at 2.5V					ns
	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B outputs valid after CCLK rising edge at 1.8V					ns
T_{BPIDCC}/T_{BPICCD}	Setup/Hold on D[15:00] data input pins			5.0/0.0		ns
SPI Master Flash Mode Programming Switching						
$T_{SPIDCC}/T_{SPIDCCD}$	DIN Setup/Hold before/after the rising CCLK edge			5.0/0.0		ns
T_{SPICCM}	MOSI clock to out at 3.3V					ns
	MOSI clock to out at 2.5V					ns
	MOSI clock to out at 1.8V					ns
$T_{SPICCFC}$	FCS_B clock to out at 3.3V					ns
	FCS_B clock to out at 2.5V					ns
	FCS_B clock to out at 1.8V					ns
CCLK Output (Master Modes)						
F_{MCCK_START}	Master CCLK frequency at start of configuration			2		MHz, Typ
T_{MCCKL}	Master CCLK clock Low time duty cycle					%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle					%, Min/Max
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time					ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time					ns, Min
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
F_{DCK}	Maximum frequency for DCLK	200	200	200		MHz
$T_{MMCMDCK\_DADDR}/T_{MMCMCKD\_DADDR}$	DADDR Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00		ns
$T_{MMCMDCK\_DI}/T_{MMCMCKD\_DI}$	DI Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00		ns
$T_{MMCMDCK\_DEN}/T_{MMCMCKD\_DEN}$	DEN Setup/Hold time	1.76/ 0.00	1.97/ 0.00	2.29/ 0.00		ns
$T_{MMCMDCK\_DWE}/T_{MMCMCKD\_DWE}$	DWE Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00		ns
$T_{MMCMCKO\_DO}$	CLK to out of DO[3]	3.10	3.61	4.37		ns
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.43	0.49	0.58		ns

Notes:

1. To support longer delays in configuration, use the design solutions described in *7 Series FPGA Configuration User Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Clock Buffers and Networks

Table 40: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins Setup/Hold	0.10/ 0.04	0.12/ 0.05	0.15/ 0.05		ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold	0.10/ 0.04	0.12/ 0.05	0.15/ 0.05		ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.08	0.09	0.11		ns
Maximum Frequency0.08						
F_{MAX_BUFG}	Global clock tree (BUFG)	710	710	625		MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 41: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BIOCKO_O}	Clock to out delay from I to O	1.14	1.29	1.52		ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	800	800	710		MHz

Table 42: **Regional Clock Buffer Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BRCKO_O}	Clock to out delay from I to O	0.77	0.87	1.03		ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.39	0.44	0.53		ns
T_{BRDO_O}	Propagation delay from CLR to O	0.67	0.76	0.89		ns
Maximum Frequency						
F_{MAX_BUFR}(1)	Regional clock tree (BUFR)	575	484	345		MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 43: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BHCKO_O}	BUFH delay from I to O	0.09	0.10	0.12		ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin Setup and Hold	0.09/ 0.05	0.11/ 0.05	0.14/ 0.06		ns
Maximum Frequency						
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	710	710	625		MHz

MMCM Switching Characteristics

Table 44: **MMCM Specification**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
MMCM_F_{INMAX}	Maximum Input Clock Frequency	1066	933	800		MHz
MMCM_F_{INMIN}	Minimum Input Clock Frequency	10	10	10		MHz
MMCM_F_{INDUTY}	Allowable Input Duty Cycle: 19—49 MHz	25	25	25		%
	Allowable Input Duty Cycle: 50—199 MHz	30	30	30		%
	Allowable Input Duty Cycle: 200—399 MHz	35	35	35		%
	Allowable Input Duty Cycle: 400—499 MHz	40	40	40		%
	Allowable Input Duty Cycle: >500 MHz	45	45	45		%
MMCM_F_{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01		MHz
MMCM_F_{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	550	500	450		MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO Frequency	600	600	600		MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO Frequency	1600	1440	1200		MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical(1)	1.22	1.22	1.22		MHz
	High MMCM Bandwidth at Typical(1)	4.88	4.88	4.88		MHz
MMCM_$T_{STATPHAOFFSET}$	Static Phase Offset of the MMCM Outputs(2)	0.12	0.12	0.12		ns
MMCM_$T_{OUTDUTY}$	MMCM Output Clock Duty Cycle Precision(3)	0.19	0.25	0.25		ns
MMCM_$T_{LOCKMAX}$	MMCM Maximum Lock Time	122	122	122		µs
MMCM_F_{OUTMAX}	MMCM Maximum Output Frequency	1066	933	800		MHz
MMCM_F_{OUTMIN}	MMCM Minimum Output Frequency(4)(5)	4.69	4.69	4.69		MHz
MMCM_$RST_{MINPULSE}$	Minimum Reset Pulse Width	5.00	5.00	5.00		ns
MMCM_F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550	500	450		MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	550	500	450		MHz
MMCM_F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	10	10	10		MHz
MMCM Switching Characteristics Setup and Hold						
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and Hold of Phase Shift Enable	1.04/ 0.00	1.04/ 0.00	1.04/ 0.00		ns
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and Hold of Phase Shift Increment/Decrement	1.04/ 0.00	1.04/ 0.00	1.04/ 0.00		ns
$T_{MMCMCKO\_PSDONE}$	Phase Shift Clock-to-Out of PSDONE	0.62	0.70	0.84		ns

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Includes global clock buffer.
4. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
5. When CASCADE4_OUT = TRUE, F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 45: **PLL Specification**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F_{INMAX}	Maximum Input Clock Frequency	1066	933	800		MHz
F_{INMIN}	Minimum Input Clock Frequency	19	19	19		MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
F_{INDUTY}	Allowable Input Duty Cycle: 19—49 MHz	25	25	25		%
	Allowable Input Duty Cycle: 50—199 MHz	30	30	30		%
	Allowable Input Duty Cycle: 200—399 MHz	35	35	35		%
	Allowable Input Duty Cycle: 400—499 MHz	40	40	40		%
	Allowable Input Duty Cycle: >500 MHz	45	45	45		%
F_{VCOMIN}	Minimum PLL VCO Frequency	800	800	800		MHz
F_{VCOMAX}	Maximum PLL VCO Frequency	2133	1866	1600		MHz
$F_{BANDWIDTH}$	Low PLL Bandwidth at Typical(1)	1.00	1.00	1.00		MHz
	High PLL Bandwidth at Typical(1)	4.00	4.00	4.00		MHz
$T_{STATPHAOFFSET}$	Static Phase Offset of the PLL Outputs(2)	0.12	0.12	0.12		ns
$T_{OUTJITTER}$	PLL Output Jitter(3)	Note 1				
$T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision(4)	0.15	0.20	0.20		ns
$T_{LOCKMAX}$	PLL Maximum Lock Time	100	100	100		µs
F_{OUTMAX}	PLL Maximum Output Frequency	1066	933	800		MHz
F_{OUTMIN}	PLL Minimum Output Frequency(5)(6)	6.25	6.25	6.25		MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				
$RST_{MINPULSE}$	Minimum Reset Pulse Width	5.00	5.00	5.00		ns
F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550	500	450		MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	550	500	450		MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	19	19	19		MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				

Table 45: **PLL Specification *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
PLL Switching Characteristics Setup and Hold						
T_{PLLCCK_DEN}/ T_{PLLCKC_DEN}	Setup and Hold of D enable	1.76/ 0.00	1.97/ 0.00	2.29/ 0.00		ns
T_{PLLCCK_DADDR}/ T_{PLLCKC_DADDR}	Setup and Hold of D address	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00		ns
T_{PLLCCK_DI}/ T_{PLLCKC_DI}	Setup and Hold of D input	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00		ns
T_{PLLCCK_DWE}/ T_{PLLCKC_DWE}	Setup and Hold of D write enable	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00		ns

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Architecture Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When CASCADE4_OUT = TRUE, F_{OUTMIN} is 0.036 MHz.

Virtex-7 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 46. Values are expressed in nanoseconds unless otherwise noted.

Table 46: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS Clock-Capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* MMCM/PLL.							
T_{ICKOF}	Clock-capable clock input and OUTFF *without* MMCM/PLL (near clock region)	XC7V285T	6.69	7.39	8.46		ns
		XC7V450T	6.94	7.66	8.76		ns
		XC7V585T	6.97	7.70	8.81		ns
		XC7V855T	7.12	7.86	8.99		ns
		XC7V1500T	N/A				ns
		XC7V2000T	N/A				ns
		XC7VX485T	5.45	6.03	6.92	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 47: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS Clock-Capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* MMCM/PLL.							
T_{ICKOF_FAR}	Clock-capable clock input and OUTFF *without* MMCM/PLL (far clock region)	XC7V285T	7.45	8.22	9.39		ns
		XC7V450T	7.17	7.92	9.05		ns
		XC7V585T	7.98	8.79	10.04		ns
		XC7V855T	8.14	8.97	10.24		ns
		XC7V1500T	N/A				ns
		XC7V2000T	N/A				ns
		XC7VX485T	6.22	6.86	7.86	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 48: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS Clock-Capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM	XC7V285T	2.32	2.40	2.47		ns
		XC7V450T	2.20	2.26	2.31		ns
		XC7V585T	2.31	2.38	2.45		ns
		XC7V855T	2.31	2.38	2.45		ns
		XC7V1500T	N/A				ns
		XC7V2000T	N/A				ns
		XC7VX485T	0.94	0.88	0.74	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 49: **Clock-Capable Clock Input to Output Delay With PLL**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS Clock-Capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* PLL.							
$T_{ICKOF\_PLL\_CC}$	Clock-capable clock input and OUTFF *with* PLL	XC7V285T	2.32	2.40	2.47		ns
		XC7V450T	2.20	2.26	2.31		ns
		XC7V585T	2.31	2.38	2.45		ns
		XC7V855T	2.31	2.38	2.45		ns
		XC7V1500T	N/A				ns
		XC7V2000T	N/A				ns
		XC7VX485T	0.94	0.88	0.74	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Virtex-7 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 50. Values are expressed in nanoseconds unless otherwise noted.

Table 50: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS Standard.(1)							
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks	XC7V285T	–1.13/ 3.38	–1.13/ 3.76	–1.13/ 4.35		ns
		XC7V450T	–0.98/ 3.12	–0.98/ 3.47	–0.98/ 4.03		ns
		XC7V585T	–1.46/ 3.92	–1.46/ 4.35	–1.46/ 5.02		ns
		XC7V855T	–1.55/ 4.08	–1.55/ 4.51	–1.55/ 5.20		ns
		XC7V1500T	N/A				ns
		XC7V2000T	N/A				ns
		XC7VX485T	–0.76/ 3.11	–0.76/ 3.47	–0.76/ 4.03	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 51: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS Standard.(1)							
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No Delay clock-capable clock input and IFF(2) with MMCM	XC7V285T	1.82/ –0.58	2.03/ –0.58	2.32/ –0.58		ns
		XC7V450T	1.71/ –0.58	1.91/ –0.58	2.19/ –0.58		ns
		XC7V585T	1.91/ –0.61	2.13/ –0.61	2.44/ –0.61		ns
		XC7V855T	1.91/ –0.61	2.13/ –0.61	2.44/ –0.61		ns
		XC7V1500T	N/A				ns
		XC7V2000T	N/A				ns
		XC7VX485T	1.82/ –0.58	2.03/ –0.58	2.32/ –0.58	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 52: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for LVCMOS Standard.(1)							
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No Delay clock-capable clock input and IFF(2) with PLL	XC7V285T	1.82/ –0.58	2.03/ –0.58	2.32/ –0.58		ns
		XC7V450T	1.71/ –0.58	1.91/ –0.58	2.19/ –0.58		ns
		XC7V585T	1.91/ –0.61	2.13/ –0.61	2.44/ –0.61		ns
		XC7V855T	1.91/ –0.61	2.13/ –0.61	2.44/ –0.61		ns
		XC7V1500T	N/A				ns
		XC7V2000T	N/A				ns
		XC7VX485T	1.82/ –0.58	2.03/ –0.58	2.32/ –0.58	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-7 FPGA clock transmitter and receiver data-valid windows.

Table 53: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion(1)	All	0.12	0.12	0.12		ns
T_{CKSKEW}	Global Clock Tree Skew(2)	XC7V285T	0.48	0.53	0.61		ns
		XC7V450T	0.33	0.36	0.41		ns
		XC7V585T	0.62	0.68	0.78		ns
		XC7V855T	0.62	0.69	0.78		ns
		XC7V1500T	N/A				ns
		XC7V2000T	N/A				ns
		XC7VX485T	0.47	0.52	0.59	N/A	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	0.08		ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.04	0.04	0.04		ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15		ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 54: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC7V285T	FFG484		ps
			FFG784		ps
			FFG1157		ps
			FFG1761		ps
		XC7V450T	FFG784		ps
			FFG1157		ps
			FFG1761		ps
		XC7V585T	FFG1157		ps
			FFG1761		ps
		XC7V855T	FFG1157		ps
			FFG1761		ps
		XC7V1500T	FHG1157		ps
			FFG1761		ps
		XC7V2000T	FHG1761		ps
			FFG1925		ps
		XC7VX485T	FFG1157		ps
			FFG1158		ps
			FFG1761		ps
			FFG1929		ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 55: **Sample Window**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{SAMP}	Sampling Error at Receiver Pins(1)	0.51	0.56	0.61		ps
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	0.30	0.35	0.40		ps

Notes:

1. This parameter indicates the total sampling error of the Virtex-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Virtex-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 56: **Pin-to-Pin Setup/Hold and Clock-to-Out**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO						
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock	–0.20/ 1.79	–0.20/ 2.01	–0.20/ 2.33		ns
Pin-to-Pin Clock-to-Out Using BUFIO						
$T_{ICKOFCS}$	Clock-to-Out of I/O clock	5.48	6.05	6.92		ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description
03/01/11	1.0	Initial Xilinx release.

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