

**FEATURES**

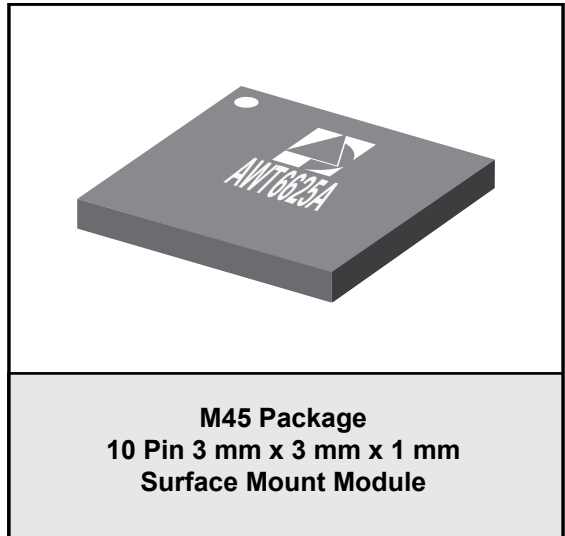
- Multimode (HSPA, EVDO Compliant)
- 4th Generation HELP™ technology
- High Efficiency (R99):
  - 41 % @ P<sub>OUT</sub> = +28.6 dBm
  - 27 % @ P<sub>OUT</sub> = +17 dBm
  - 17 % @ P<sub>OUT</sub> = +13.5 dBm
  - 18 % @ P<sub>OUT</sub> = +7 dBm
  - 11 % @ P<sub>OUT</sub> = +3.5 dBm
- Low Quiescent Current: <3 mA
- Low Leakage Current in Shutdown Mode: <5 μA
- Internal Voltage Regulator
- Integrated “daisy chainable” directional coupler with CPL<sub>IN</sub> and CPL<sub>OUT</sub> port.
- Internal DC Blocks on all RF ports
- Optimized for a 50 Ω System
- 1.8V Control Logic
- RoHS Compliant Package, 260 °C MSL-3

**APPLICATIONS**

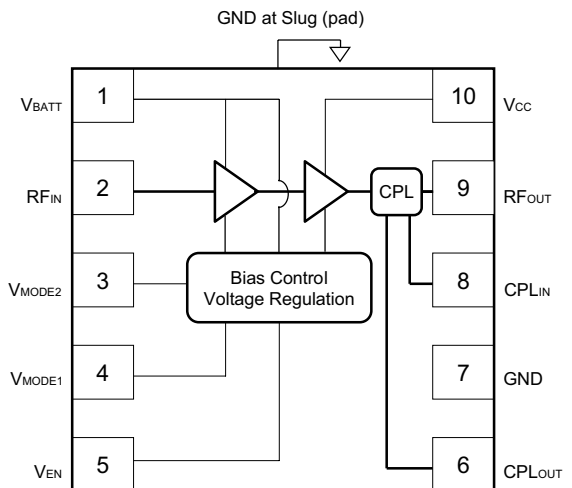
- Band 5
- Band Classes 0 & 10 CDMA/EVDO Wireless Devices

**PRODUCT DESCRIPTION**

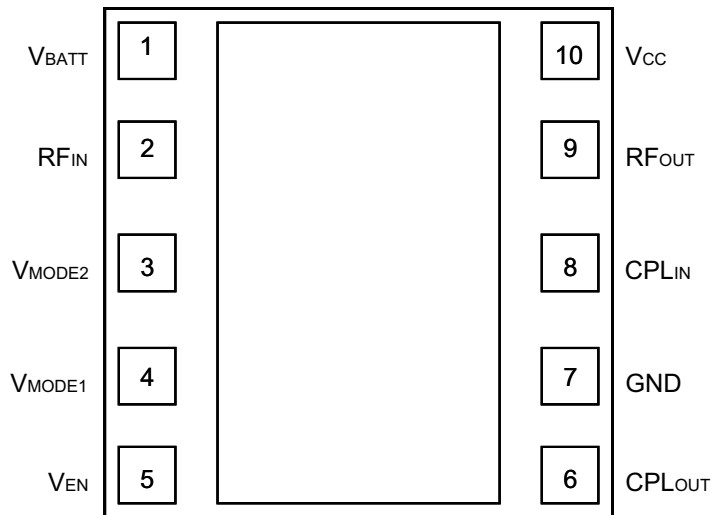
The AWT6625A HELP4™ PA is the 4th generation HELP™ product for WCDMA devices operating in UMTS800 (Band 5) and for CDMA devices operating in Cell-band. This PA incorporates ANADIGICS’ HELP4™ technology to deliver exceptional efficiency at low power levels and low quiescent current without the need for external voltage regulators or converters. The device is manufactured using advanced InGaP-Plus™ HBT technology offering state-of-the-art reliability, temperature stability, and ruggedness. Three selectable bias modes that optimize efficiency for different output power levels and a shutdown mode with low leakage current increase handset



talk and standby time. A “daisy chainable” directional coupler is integrated in the module thus eliminating the need of an external coupler. The self-contained 3 mm x 3 mm x 1 mm surface mount package incorporates matching networks optimized for output power, efficiency, and linearity in a 50 Ω system.



**Figure 1: Block Diagram**



**Figure 2: Pinout (X-ray Top View)**

**Table 1: Pin Description**

PIN	NAME	DESCRIPTION
1	V <sub>BATT</sub>	Battery Voltage
2	RF <sub>IN</sub>	RF Input
3	V <sub>MODE2</sub>	Mode Control Voltage 2
4	V <sub>MODE1</sub>	Mode Control Voltage 1
5	V <sub>EN</sub>	PA Enable Voltage
6	CPL <sub>OUT</sub>	Coupler Output
7	GND	Ground
8	CPL <sub>IN</sub>	Coupler Input
9	RF <sub>OUT</sub>	RF Output
10	V <sub>CC</sub>	Supply Voltage

## ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage ( $V_{CC}$ )	0	+5	V
Battery Voltage ( $V_{BATT}$ )	0	+6	V
Control Voltages ( $V_{MODE1}$ , $V_{MODE2}$ , $V_{EN}$ )	0	+3.5	V
RF Input Power ( $P_{IN}$ )	-	+10	dBm
Storage Temperature ( $T_{STG}$ )	-40	+150	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (f)	814	-	849	MHz	
Supply Voltage ( $V_{CC}$ )	+3.2	+3.4	+4.35	V	$P_{OUT} \leq +28.6$ dBm
Enable Voltage ( $V_{EN}$ )	+1.35 0	+1.8 -	+3.1 +0.5	V	PA "on" PA "shut down"
Mode Control Voltage ( $V_{MODE1}$ , $V_{MODE2}$ )	+1.35 0	+1.8 -	+3.1 +0.5	V	Low Bias Mode High Bias Mode
UMTS Output Power R99, HPM HSPA (MPR = 0), HPM R99, MPM HSPA (MPR = 0), MPM R99, LPM HSPA (MPR = 0), LPM	28.1 <sup>(1)</sup> 27.1 <sup>(1)</sup> 16.5 15.5 - -	28.6 27.6 17.0 16.0 7 6.0	- - - - - -	dBm	3GPP TS 34.121-1, Rel 8 Table C.11.1.3 for WCDMA SUBTEST 1
CDMA Output Power HPM MPM LPM	27.2 <sup>(1)</sup> - -	27.7 16.0 6.5	- - -	dBm	CDMA 2000, RC1
Case Temperature ( $T_c$ )	-30	-	+90	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Note:

(1) For operation at 3.2 V,  $P_{OUT}$  is derated by 0.5 dB.

**Table 4: Electrical Specifications - WCDMA Operation (R99 Modulation)**  
**(T<sub>C</sub> = +25 °C, V<sub>CC</sub> = +3.4 V, V<sub>BATT</sub> = +3.4 V, V<sub>EN</sub> = +1.8 V, 50 Ω system)**

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P <sub>OUT</sub>	V <sub>MODE1</sub>	V <sub>MODE2</sub>
Gain	26 16 10	28.5 19 13.5	31.5 21.5 16	dB	P <sub>OUT</sub> = +28.6 dBm P <sub>OUT</sub> = +17 dBm P <sub>OUT</sub> = +7 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR1 at 5 MHz offset <sup>(1)</sup>	- - -	-42 -42 -41	-37 -36.5 -36.5	dBc	P <sub>OUT</sub> = +28.6 dBm P <sub>OUT</sub> = +17 dBm P <sub>OUT</sub> = +7 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
ACLR2 at 10 MHz offset	- - -	-57 -59 -60	-48 -48 -48	dBc	P <sub>OUT</sub> = +28.6 dBm P <sub>OUT</sub> = +17 dBm P <sub>OUT</sub> = +7 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Power-Added Efficiency <sup>(1)</sup>	37 23 15 -	41.5 27 17 18 11	- - - -	%	P <sub>OUT</sub> = +28.6 dBm P <sub>OUT</sub> = +17 dBm P <sub>OUT</sub> = +13.5 dBm P <sub>OUT</sub> = +7 dBm P <sub>OUT</sub> = +3.5 dBm	0 V 1.8 V 1.8 V 1.8 V 1.8 V	0 V 0 V 0 V 1.8 V 1.8 V
Quiescent Current (I <sub>q</sub> ) Low Bias Mode	-	3	4.5	mA	through V <sub>CC</sub> pin	1.8 V	1.8 V
Mode Control Current	-	0.06	0.12	mA	through V <sub>MODE</sub> pins, V <sub>MODE</sub> = 1.8 V		
Enable Current	-	0.04	0.1	mA	through V <sub>EN</sub> pin		
BATT Current	-	0.7	1.4	mA	through V <sub>BATT</sub> pin, V <sub>MODE1</sub> = +1.8 V, V <sub>MODE2</sub> = +1.8 V		
Leakage Current	-	<5	10	μA	V <sub>BATT</sub> = +4.2 V, V <sub>CC</sub> = +4.2 V, V <sub>EN</sub> = 0 V, V <sub>MODE</sub> = 0 V, V <sub>MODE1</sub> = 0 V		
Noise in Receive Band	-	-134	-	dBm/Hz	869 MHz to 894 MHz		
Harmonic 2 fo 3 fo, 4 fo	- - -	-46 -50	-35 -42	dBc	P <sub>OUT</sub> ≤ +28.6 dBm		
Coupling Factor	-	20.5	-	dB			
Directivity	-	20	-	dB			
Coupler IN_OUT Daisy Chain Insertion Loss	-	<0.35	-	dB	698 MHz to 2620 MHz Pin 8 - 6, Shutdown Mode		
Spurious Output Level (all spurious outputs)	-	-	-70	dBc	P <sub>OUT</sub> < +28.6 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating conditions		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range		

Notes:

(1) ACLR and Efficiency measured at 836.5 MHz.

**Table 5: Electrical Specifications - CDMA2000 Operation (RC-1 waveform)**  
 (T<sub>C</sub> = +25 °C, V<sub>BATT</sub> = V<sub>CC</sub> = +3.4 V, V<sub>ENABLE</sub> = +1.8 V, 50 Ω system)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P <sub>OUT</sub>	V <sub>MODE1</sub>	V <sub>MODE2</sub>
Gain	26 15 10	29 19 13.5	32 22 16	dB	P <sub>OUT</sub> = +27.7 dBm P <sub>OUT</sub> = +16 dBm P <sub>OUT</sub> = +6.5 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Adjacent Channel Power at ± 885 kHz offset <sup>(1)</sup> Primary Channel BW = 1.23 MHz Adjacent Channel BW = 30 kHz	- - -	-50 -50 -51	-46.5 -46.5 -46.5	dBc	P <sub>OUT</sub> = +27.7 dBm P <sub>OUT</sub> = +16 dBm P <sub>OUT</sub> = +6.5 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Adjacent Channel Power at ± 1.98 MHz offset <sup>(1)</sup> Primary Channel BW = 1.23 MHz Adjacent Channel BW = 30 kHz	- - -	-59 -60 -59	-56 -56 -56	dBc	P <sub>OUT</sub> = +27.7 dBm P <sub>OUT</sub> = +16 dBm P <sub>OUT</sub> = +6.5 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Power-Added Efficiency <sup>(1)</sup>	33 20 13	37 23 16.5	- - -	%	P <sub>OUT</sub> = +27.7 dBm P <sub>OUT</sub> = +16 dBm P <sub>OUT</sub> = +6.5 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Spurious Output Level (all spurious outputs)	-	-	-70	dBc	P <sub>OUT</sub> < +27.7 dBm In-band Load VSWR < 5:1 Out-of-band Load VSWR < 10:1 Applies over all operating conditions		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over all operating conditions		

Notes:

(1) ACLR and Efficiency measured at 836.5 MHz.

**APPLICATION INFORMATION**

To ensure proper performance, refer to all related Application Notes on the ANADIGICS web site: <http://www.anadigics.com>

**Shutdown Mode**

The power amplifier may be placed in a shutdown mode by applying logic low levels (see Operating Ranges table) to the  $V_{EN}$ ,  $V_{MODE1}$  and  $V_{MODE2}$  voltages.

**Bias Modes**

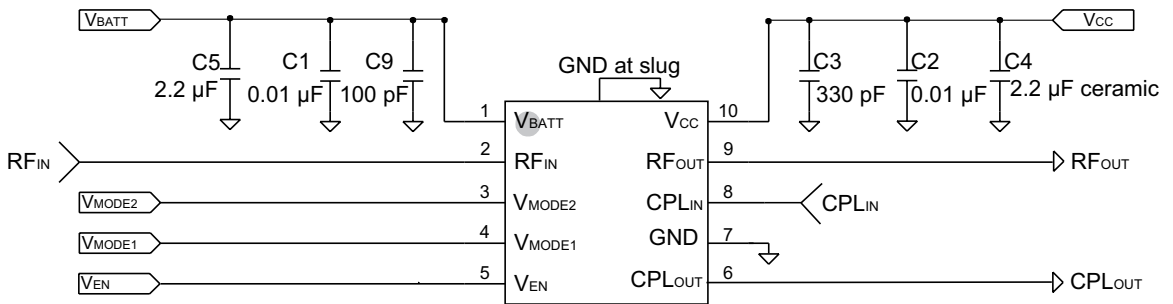
The power amplifier may be placed in either Low, Medium or High Bias modes by applying the appropriate logic level (see Operating Ranges table)

to the  $V_{MODE}$  voltages. The Bias Control table below lists the recommended modes of operation for various applications.

Three operating modes are recommended to optimize current consumption. High Bias/High Power operating mode is for  $P_{OUT}$  levels  $\geq 17$  dBm. At  $\sim 17$  dBm - 7 dBm, the PA should be "Mode Switched" to Medium Power Mode. For  $P_{OUT}$  levels  $\leq \sim 7$  dBm, the PA can be switched to Low Power Mode for even lower quiescent current consumption.

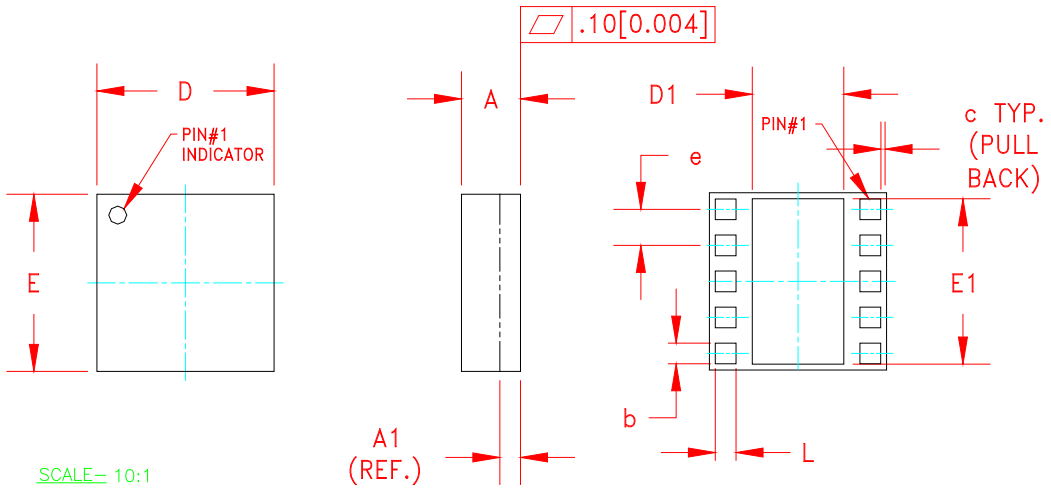
**Table 6: Bias Control**

APPLICATION	$P_{OUT}$ LEVELS	BIAS MODE	$V_{EN}$	$V_{MODE1}$	$V_{MODE2}$	$V_{CC}$	$V_{BATT}$
Low power (Low Bias Mode)	$\leq +7$ dBm	Low	+1.8 V	+1.8 V	+1.8 V	3.2 - 4.35 V	$> 3.2$ V
Med power (Medium Bias Mode)	$> 7$ dBm $\leq +17$ dBm	Low	+1.8 V	+1.8 V	0 V	3.2 - 4.35 V	$> 3.2$ V
High power (High Bias Mode)	$> +17$ dBm	High	+1.8 V	0 V	0 V	3.2 - 4.35 V	$> 3.2$ V
Shutdown	-	Shutdown	0 V	0 V	0 V	3.2 - 4.35 V	$> 3.2$ V



**Figure 3: Evaluation Board Schematic**

PACKAGE OUTLINE



SCALE= 10:1

SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.91	1.03	1.13	0.035	0.041	0.044	-
A1	PLEASE REFER TO LAMINATE CONTROL DRAWING						-
b	0.32	0.35	0.40	0.013	0.014	0.016	3
c	-	0.10	-	-	0.004	-	-
D	2.88	3.00	3.12	0.113	0.118	0.123	-
D1	1.45	1.50	1.57	0.057	0.059	0.062	3
E	2.88	3.00	3.12	0.113	0.118	0.123	-
E1	2.70	2.75	2.85	0.106	0.108	0.112	3
e	0.60			0.024			3
L	0.32	0.35	0.40	0.013	0.014	0.016	3

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL PAD SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO SPECIFIC LAMINATE DESIGN.
4. UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
5. LAMINATE CONTROL DRAWING SPECIFIED BY PART NUMBER.

Figure 4: M45 Package Outline - 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module

TOP BRAND

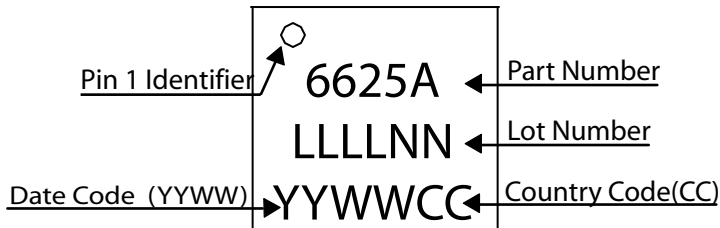
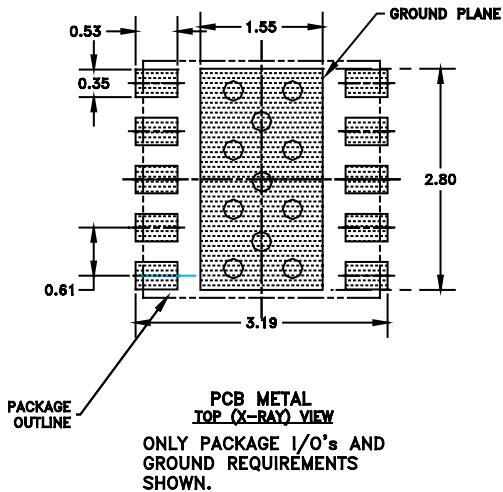


Figure 5: Branding Specification - M45 Package

PCB AND STENCIL DESIGN GUIDELINE



**NOTES:**

- (1) OUTLINE DRAWING REFERENCE: P8002478\_E
- (2) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
- (3) DIMENSIONS IN MILLIMETERS.
- (4) VIAS SHOWN IN PCB METAL VIEW ARE FOR REFERENCE ONLY. NUMBER & SIZE OF THERMAL VIAS REQUIRED DEPENDENT ON HEAT DISSIPATION REQUIREMENT AND THE PCB PROCESS CAPABILITY.
- (5) RECOMMENDED STENCIL THICKNESS: APPROX. 0.150mm (6 Mils)

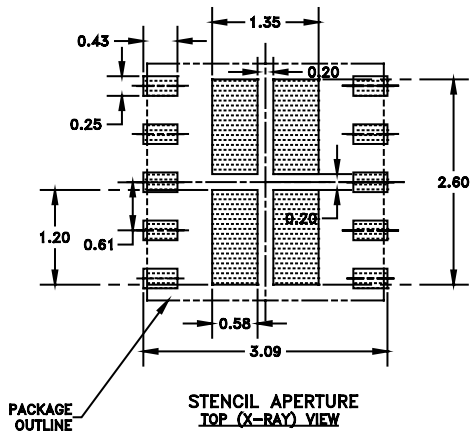
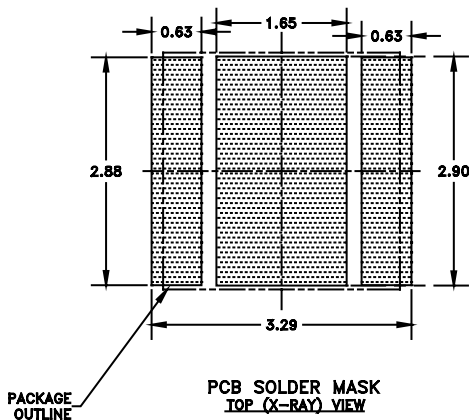
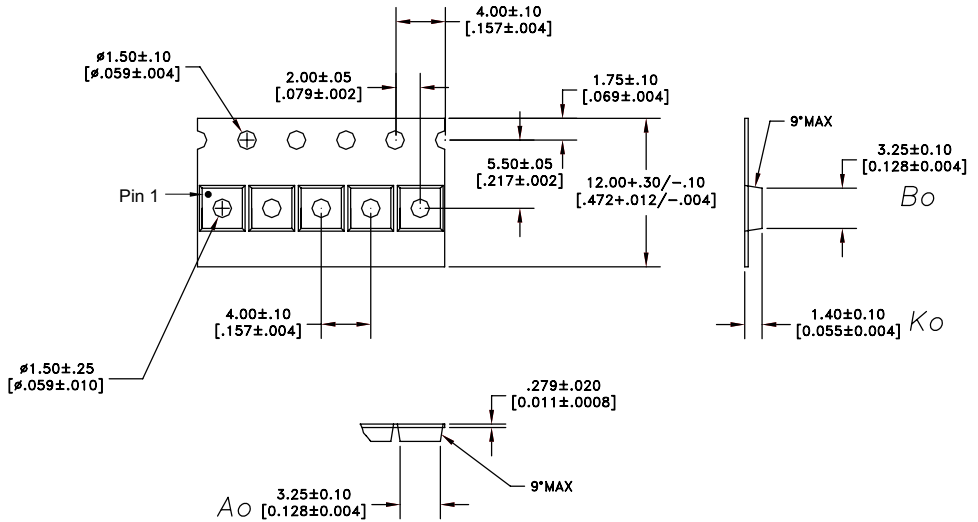


Figure 6: Recommended PCB Layout Information



COMPONENT PACKAGING



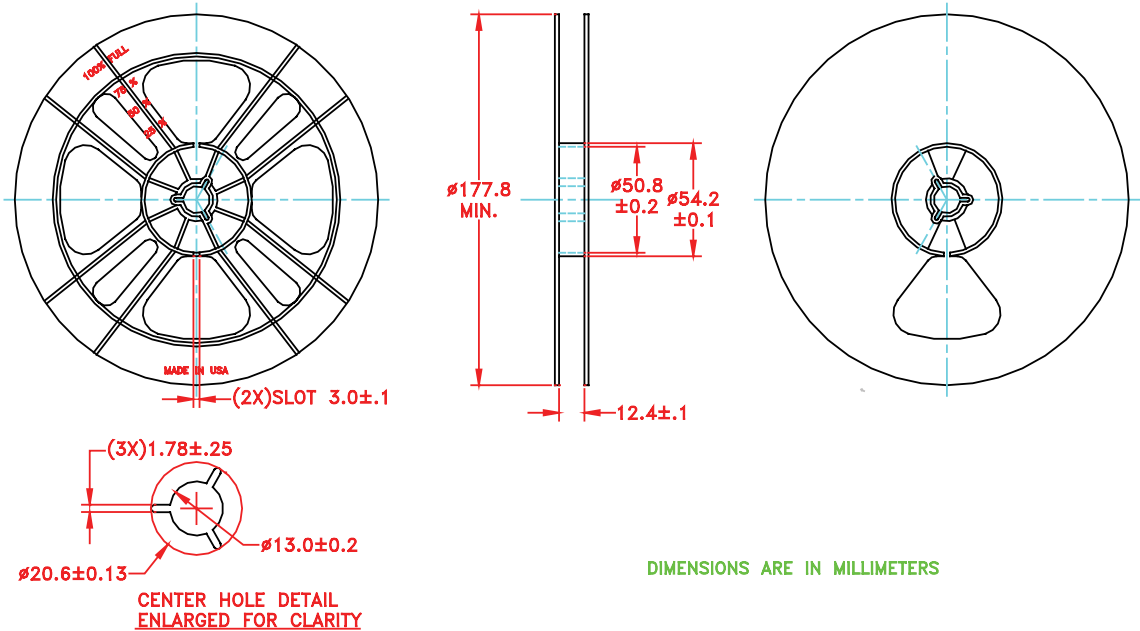
NOTES:

- 1. MATERIAL: 3000 (CARBON FILLED POLYCARBONATE)  
100% RECYCLABLE.

DIMENSIONS ARE IN MILLIMETERS [INCHES]

*DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994*

Figure 7: Carrier Tape



NOTES:

- 1. MATERIAL: BLACK CARBON POLYSTYRENE
- SURFACE RESISTIVITY:  $1 \times 10^4$  TO  $1 \times 10^8$  ohms/square

*DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994*

Figure 8: Reel

**ORDERING INFORMATION**

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
AWT6625ARM45Q7	-30 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module	Tape and Reel, 2500 pieces per Reel
AWT6625ARM45P9	-30 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module	Partial Tape and Reel



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