

524,288 WORDS×36 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM365120BS/BSG/AS/ASG is a 524,288 words by 36 bits dynamic RAM module which assembled 16 pcs of TC514256AJ/BJ and 8 pcs of TC51256T on the printed circuit board. These modules can be as well used as 1,048,576 words by 18 bits dynamic RAM module, by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ..., DQ17 and DQ35, respectively. The These modules are optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

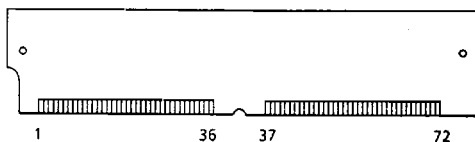
FEATURES

- 524,288 words by 36 bits organization
- Fast access time and cycle time
- Low Power
6,072mW MAX. Operating (THMxxxxxx-60)
5,412mW MAX. Operating (THMxxxxxx-70)
4,752mW MAX. Operating (THMxxxxxx-80)
4,092mW MAX. Operating (THMxxxxxx-10)
132mW MAX. Standby
- Single power supply of 5V±10%
- All inputs and outputs TTL compatible
- 512 refresh cycles/4ms(Burst Refresh)
- 512 refresh cycles/8ms(Distributed Refresh)

	-60	-70	-80	-10
t _{RAC} RAS Access Time	60ns	70ns	80ns	100ns
t _{AA} Column Address Access Time	30ns	35ns	40ns	50ns
t _{CAC} CAS Access Time	20ns	20ns	20ns	25ns
t _{RC} Cycle Time	115ns	130ns	150ns	180ns
t _{PC} Fast Page Mode Cycle Time	40ns	40ns	45ns	55ns

- CAS before RAS refresh, RAS only refresh, Hidden refresh and Fast Page Mode capability
- Package THM365120BS -60 : Tin - Lead Contact
THM365120AS -70,80,10 : Tin - Lead Contact
THM365120BSG -60 : Gold Contact
THM365120ASG -70,80,10 : Gold Contact

PIN CONNECTION (TOP VIEW)



PIN NAMES

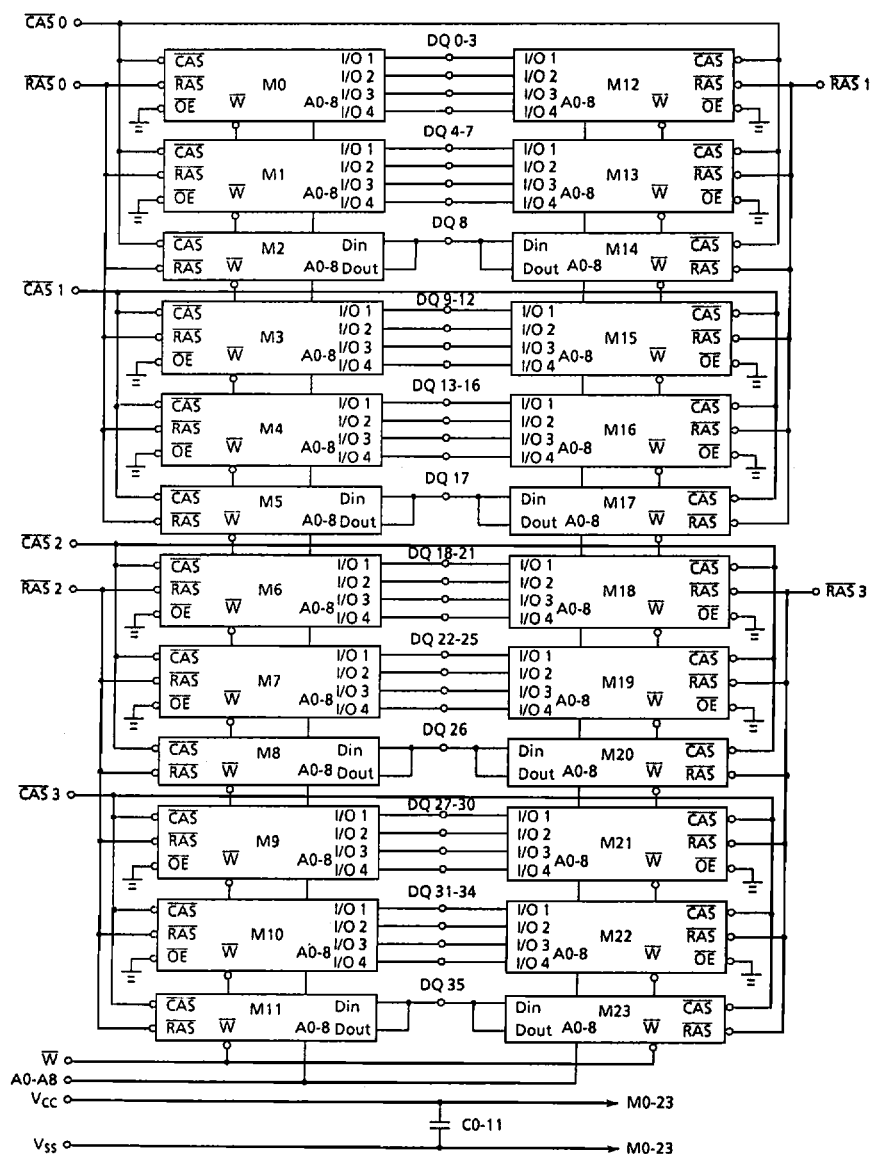
A0~A8	Address Inputs
DQ0~DQ35	Data Input/Outputs
CAS0~CAS3	Column Address Strobe
RAS0~RAS3	Row Address Strobe
W	Read/Write Input
V _{CC}	Power (+5V)
V _{SS}	Ground
PD	Presence Detect Pin

1	V _{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V _{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	CAS0	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	CAS2	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V _{CC}	42	CAS3	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	CAS1	55	DQ12	67	PD0
8	DQ3	20	DQ4	32	NC	44	RAS0	56	DQ30	68	PD1
9	DQ21	21	DQ22	33	RAS3	45	RAS1	57	DQ13	69	PD2
10	V _{CC}	22	DQ5	34	RAS2	46	NC	58	DQ31	70	PD3
11	NC	23	DQ23	35	DQ26	47	W	59	V _{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V _{SS}

	-60	-70	-80	-10
PD0	NC	NC	NC	NC
PD1	V _{SS}	V _{SS}	V _{SS}	V _{SS}
PD2	NC	V _{SS}	NC	V _{SS}
PD3	NC	NC	V _{SS}	V _{SS}

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BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	-1.0~7.0	V	1
Output Voltage	V_{OUT}	-1.0~7.0	V	1
Power Supply Voltage	V_{CC}	-1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	14.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0 \sim 70^{\circ}\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

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DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC} \text{ MIN.}$)	THMxxxxxx-60	–	1104	mA 3, 4 5
		THMxxxxxx-70	–	984	
		THMxxxxxx-80	–	864	
		THMxxxxxx-10	–	744	
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	–	48	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC} \text{ MIN.}$)	THMxxxxxx-60	–	1104	mA 3, 5
		THMxxxxxx-70	–	984	
		THMxxxxxx-80	–	864	
		THMxxxxxx-10	–	744	
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC} = t_{PC} \text{ MIN.}$)	THMxxxxxx-60	–	744	mA 3, 4 5
		THMxxxxxx-70	–	744	
		THMxxxxxx-80	–	624	
		THMxxxxxx-10	–	504	
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)	–	24	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC} \text{ MIN.}$)	THMxxxxxx-60	–	1104	mA 3, 5
		THMxxxxxx-70	–	984	
		THMxxxxxx-80	–	864	
		THMxxxxxx-10	–	744	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = $0V$)	– 240	240	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)	– 20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5mA$)	2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2mA$)	–	0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$) (Notes 6, 7, 8)

SYMBOL	PARAMETER	THMxxxxx-60		THMxxxxx-70		THMxxxxx-80		THMxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	150	—	180	—	ns	
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	50	—	60	—	ns	
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	—	80	—	100	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	20	—	20	—	25	ns	9,14
t_{AA}	Access Time from Column Address	—	30	—	35	—	40	—	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	—	45	—	55	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	—	0	—	0	—	0	—	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	60	—	70	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	20	—	20	—	25	—	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	—	40	—	45	—	55	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	80	—	100	—	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	5	—	5	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	10	—	10	—	ns	
t_{ASR}	Row Address Set-Up Time	0	—	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	10	—	15	—	ns	
t_{ASC}	Column Address Set-Up Time	0	—	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	15	—	20	—	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	—	55	—	60	—	75	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	40	—	50	—	ns	
t_{RCS}	Read Command Set-Up Time	0	—	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time	0	—	0	—	0	—	0	—	ns	11

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	15	–	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	55	–	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	10	–	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	0	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	40	–	40	–	50	–	ns	

CAPACITANCE ($V_{CC} = 5V \pm 10\%$, $f = 1MHz$, $T_a = 0 \sim 70^\circ C$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C11	Input Capacitance (A0~A8)	–	161	pF
C12	Input Capacitance ($\overline{V}$)	–	168	pF
C13	Input Capacitance ($\overline{RAS0} \sim \overline{RAS3}$)	–	42	pF
C14	Input Capacitance ($\overline{CAS0} \sim \overline{CAS3}$)	–	42	pF
CDQ1	I/O Capacitance (DQ0~7, 9~16, 18~25, 27~34)	–	29	pF
CDQ2	I/O Capacitance (DQ8, 17, 26, 35)	–	39	pF

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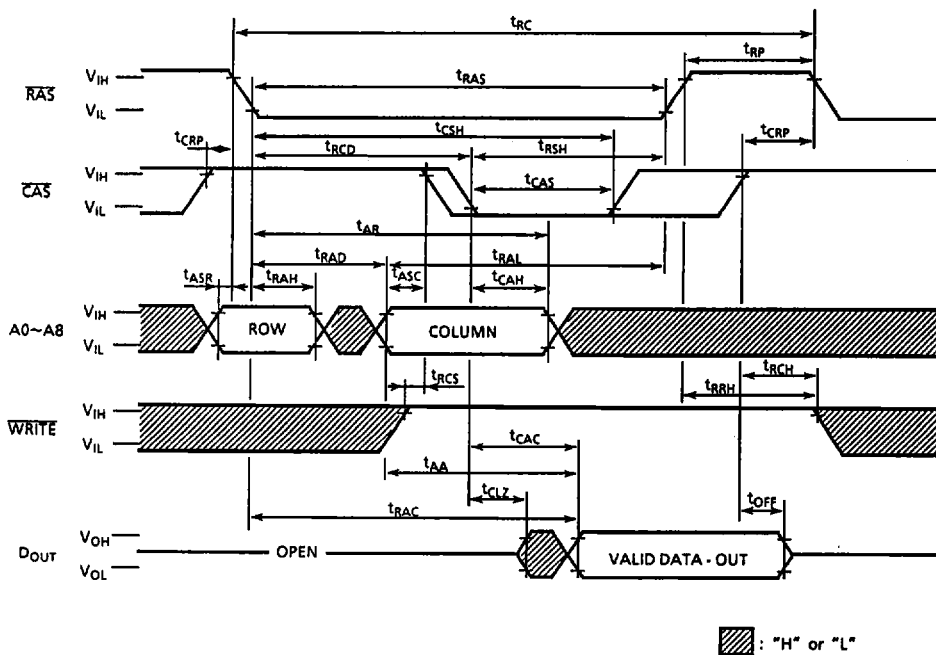
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS} .
3. $ICC1$, $ICC3$, $ICC4$, $ICC6$ depend on cycle rate.
4. $ICC1$, $ICC4$ depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of $200\mu s$ is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_P=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. $twCS$ is not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $twCS \geq twCS$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC} .
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA} .

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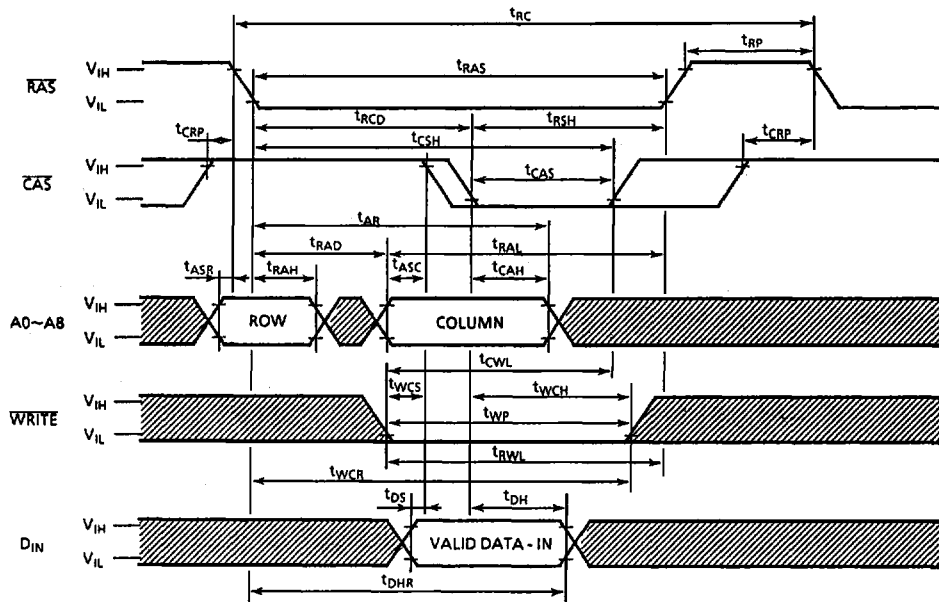
TIMING WAVEFORMS

READ CYCLE



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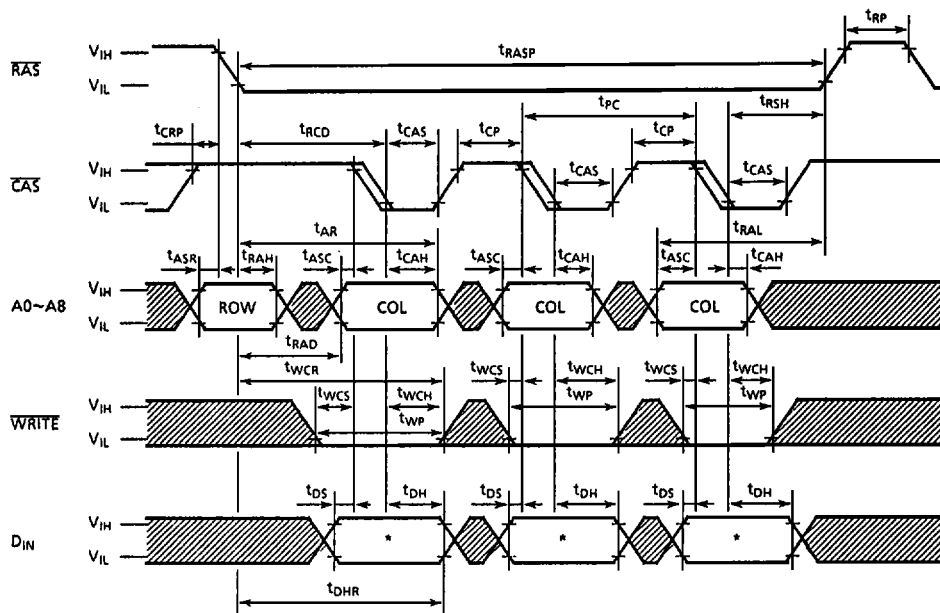
WRITE CYCLE (EARLY WRITE)



▨ : "H" or "L"

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FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

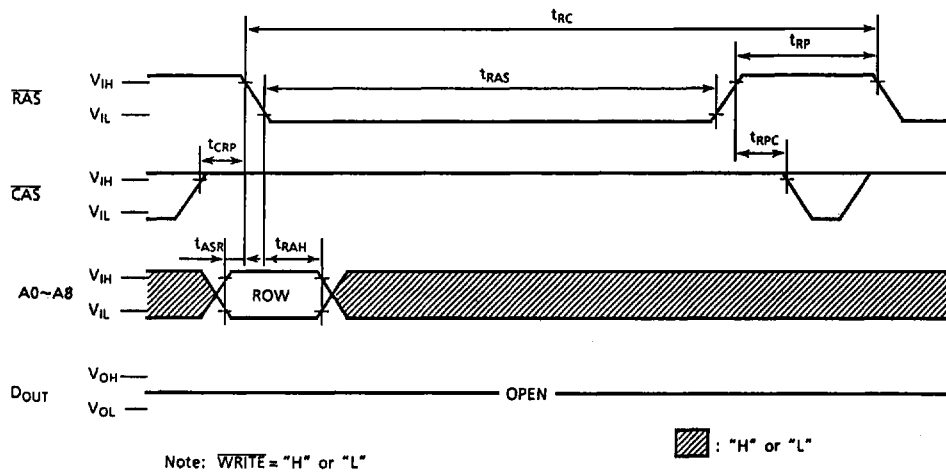


* VALID DATA IN

▨ : "H" or "L"

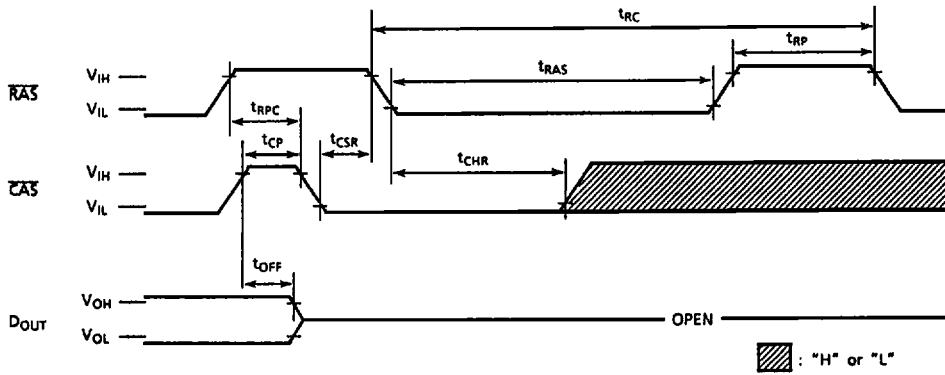
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RAS ONLY REFRESH CYCLE



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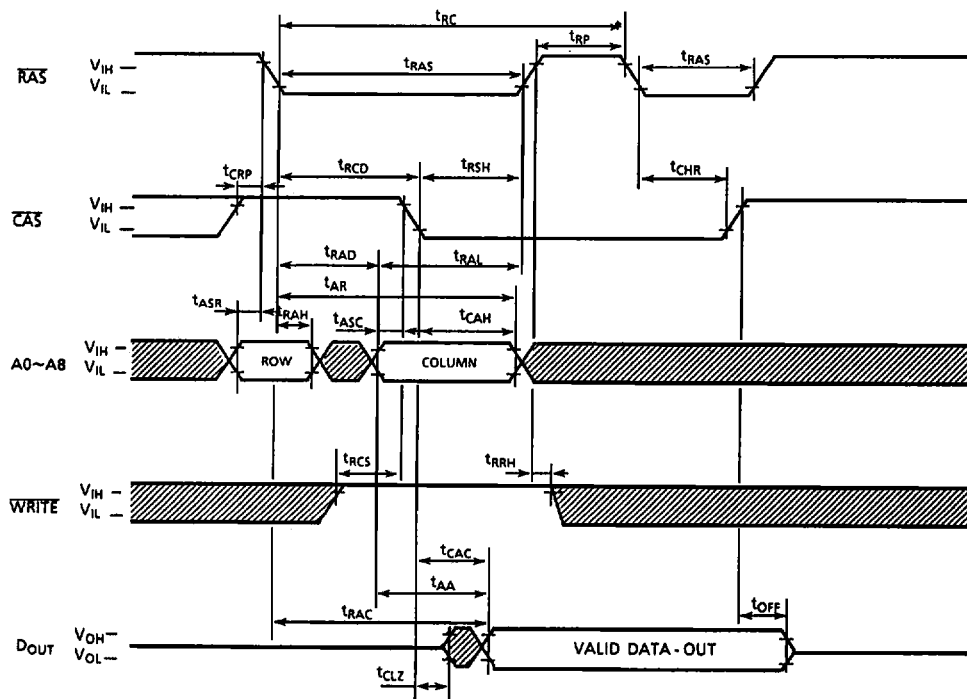
CAS BEFORE RAS REFRESH CYCLE



Note: A0~A8, WRITE = "H" or "L"

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THM365120BSG-60, THM365120ASG-70, 80, 10

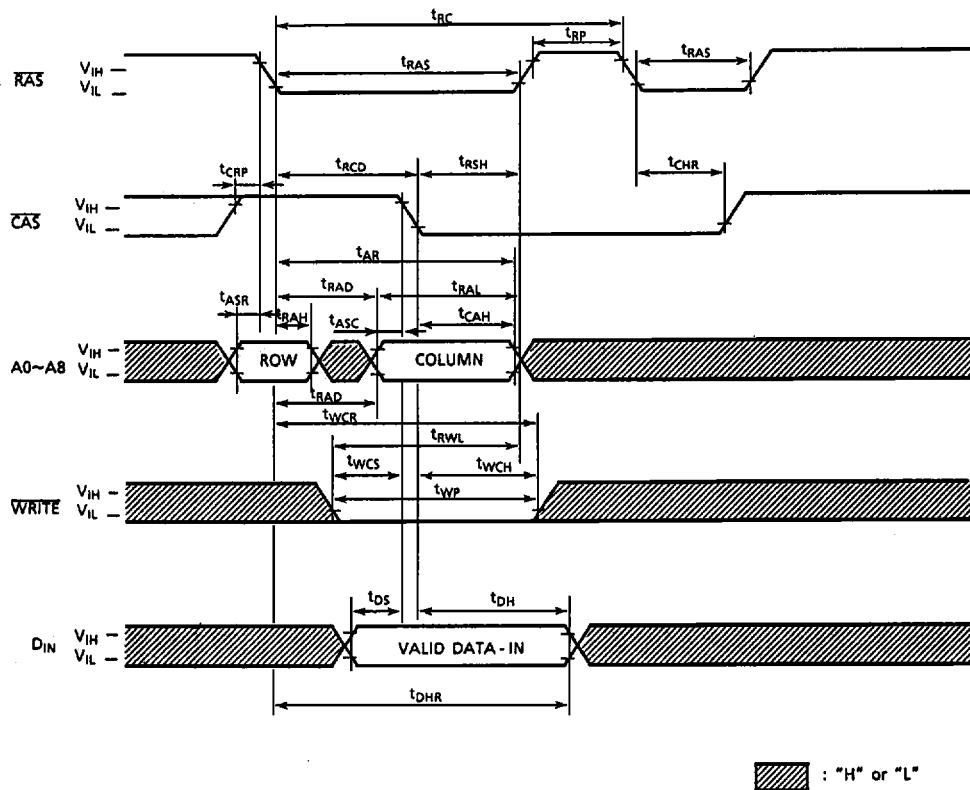
HIDDEN REFRESH CYCLE (READ)



▨ : "H" or "L"

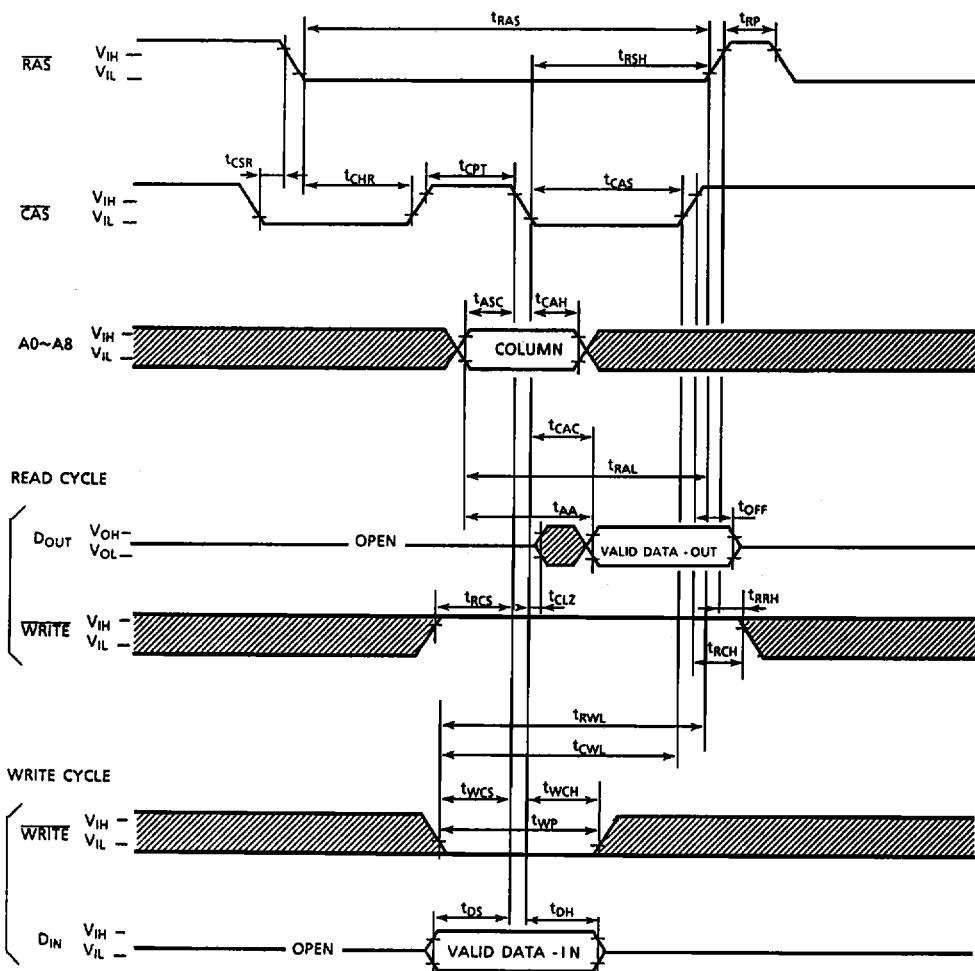
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HIDDEN REFRESH CYCLE (WRITE)



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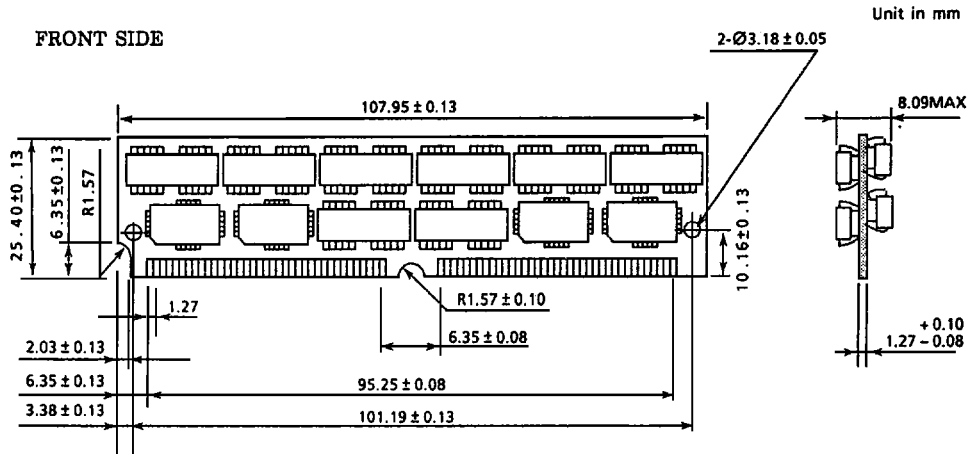
CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



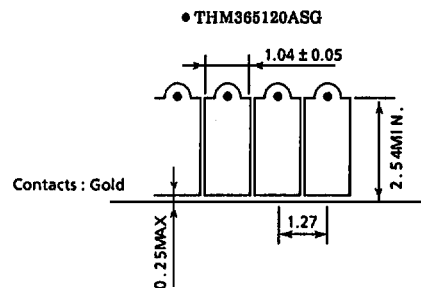
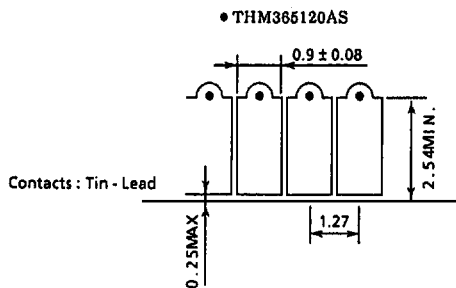
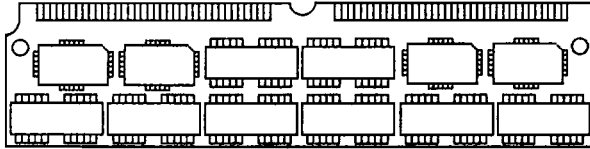
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OUTLINE DRAWINGS

THM365120AS/ASG



BACK SIDE



NOTES