μPD7508A
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTER WITH FIP® DRIVER

Description

The μPD7508A 4-bit, single-chip CMOS microcomputer has advanced fourth-generation architecture. It is identical to the μPD7508 except for a smaller RAM and 16 lines of vacuum fluorescent display FIP drive capability. It contains a 4096 x 8-bit ROM and a 208 x 4-bit RAM.

The μPD7508A contains four 4-bit general purpose registers outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility. The μPD7508A executes 92 instructions of the μPD7500 series instruction set A with a 10-μs cycle time.

The μPD7508A has two external and two internal edge-triggered hardware vectored interrupts. It also contains an 8-bit timer/event counter and an 8-bit serial interface to reduce software requirements. Ports 3-6 can be pulled to −35 V to drive vacuum fluorescent displays. CMOS technology allows the use of a single 2.7 V to 6.0 V power supply with a maximum current consumption of 900 μA. This is even lower in the HALT and STOP standby modes.

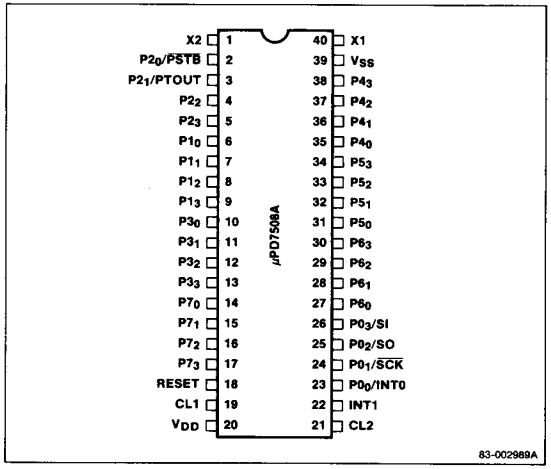
Features

- ☐ Single-chip microcomputer
- ☐ Executes 92 instructions of μPD7500 instruction set A
- ☐ Instruction cycle:
  - — 10 μs/200 kHz (5 V internal)
  - — 5 μs/400 kHz (5 V external)
- ☐ 4096 x 8-bit program ROM
- ☐ 208 x 4-bit data RAM
- ☐ Interrupt capabilities
  - — Two external interrupts: INT0, INT1
  - — Two internal interrupts: INTT, INTS
- ☐ 8-bit timer/event counter
- ☐ 8-bit serial interface
- ☐ Two standby modes
- ☐ Data retention mode
- ☐ 32 I/O lines
- ☐ Four high-voltage (40 V) ports
- ☐ Two high-current (8 mA) ports
- ☐ Internal RC oscillation circuitry
- ☐ Crystal oscillation circuitry for count clock
- ☐ Low power consumption
- ☐ Single 2.7 to 6.0 V operating voltage
- ☐ CMOS technology

Ordering Information

Part No.	Package Type	Max Frequency of Operation
μPD7508AC	40-pin plastic DIP	400 kHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1, 40	X2, X1	Crystal clock/external event input port
2-5	$P2_0/\overline{PSTB}$ $P2_1$/PTOUT, $P2_2$, $P2_3$	Output port 2/output strobe pulse, timer out F/F signal
6-9	$P1_0$-$P1_3$	I/O port 1
10-13	$P3_0$-$P3_3$	Output port 3
14-17	$P7_0$-$P7_3$	I/O port 7
18	RESET	RESET input
19, 21	CL1, CL2	System clock inputs
20	V_{DD}	Positive power supply
22	INT1	External interrupt
23-26	$P0_0$/INT0, $P0_1/\overline{SCK}$, $P0_2$/SO $P0_3$/SI	Input port 0/ external interrupt, serial I/O interface
27-30	$P6_0$-$P6_3$	I/O port 6
31-34	$P5_0$-$P5_3$	I/O port 5
35-38	$P4_3$-$P4_0$	I/O port 4
39	V_{SS}	Ground

FIP is the registered trademark for NEC's fluorescent indicator panel (vacuum fluorescent display).

3

Pin Functions

$P0_0$/INT0, $P0_1$/$\overline{SCK}$, [Port 0/External Interrupt, Serial Interface] $P0_2$/SO, $P0_3$/SI

4-bit input port/serial I/O interface. This port can be configured as a 4-bit parallel input port or as the 8-bit serial I/O interface under control of the serial-mode select register. The serial input SI, serial output SO (active low), and the serial clock $\overline{SCK}$ (active low) used for synchronizing data transfer make up the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT0, a rising edge-triggered interrupt. If $P0_0$/INT0 is unused, it should be connected to V_{SS}. If $P0_1$/$\overline{SCK}$, $P0_2$/SO, or $P0_3$/SI are unused, connect them to V_{SS} or V_{DD}.

$P1_0$-$P1_3$ [Port 1]

4-bit input/three-state output port. Data output to port 1 is strobed in synchronization with a $P2_0$/$\overline{PSTB}$ pulse. Connect unused pins to V_{SS} or V_{DD}.

$P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$, $P2_3$ [Port 2]

4-bit latched three-state output port. Line $P2_0$ is shared with $\overline{PSTB}$, the port 1 output strobe pulse. Line $P2_1$ is shared with PTOUT, the timer out F/F signal. Leave unused pins open.

$P3_0$-$P3_3$ [Port 3]

4-bit latched three-state output port. Leave unused pins open.

$P4_0$-$P4_3$ [Port 4]

4-bit latched three-state output port. Can also perform 8-bit parallel I/O with port 5. In input mode, connect unused pins to V_{DD} or GND. In output mode, leave unused pins open.

$P5_3$-$P5_0$ [Port 5]

4-bit input/latched three-state output port. This port also performs 8-bit parallel I/O with port 4. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P6_3$-$P6_0$ [Port 6]

4-bit input/latched three-state output port. The port 6 mode select register configures individual lines as inputs or outputs. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P7_0$-$P7_3$ [Port 7]

4-bit input/latched three-state output port. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

X2, X1 [Crystal Clock/External Event Input]

For crystal clock operation, connect a crystal oscillator circuit to input X1 and output X2. For external event counting, input external event pulses to input X1 while leaving output X2 open. If X1 is not used, leave it open. If X2 is not used, connect it to ground.

CL1, CL2 [System Clock Input]

Connect an 82 kΩ resistor across CL1 and CL2, and connect a 33 pF capacitor from CL1 to V_{SS} (200 kHz). Alternatively, connect an external clock source to CL1 and leave CL2 open. If CL1 is not used, connect it to V_{SS}.

RESET [Reset]

A high level input to this pin initializes the μPD7508A after power up.

INT1 [Interrupt 1]

External rising edge-triggered interrupt. Connect to V_{SS} if unused.

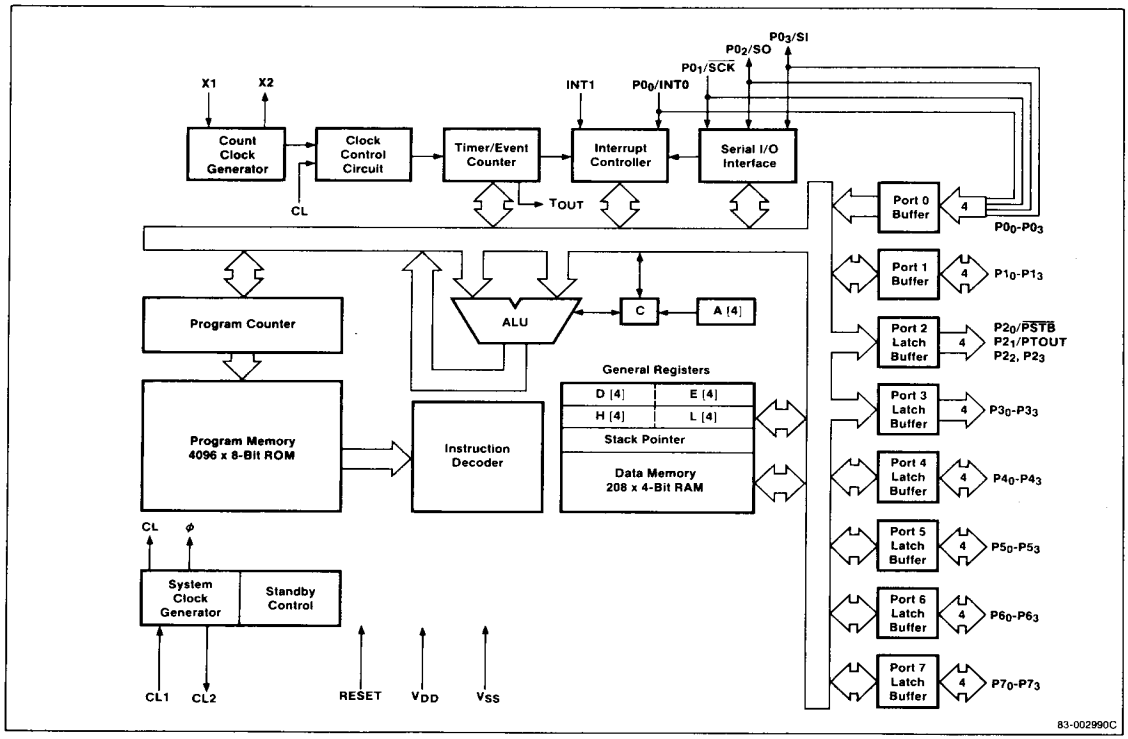
V_{DD} [Power Supply]

Positive power supply. Apply a single voltage in the range 2.7 to 6.0 V for proper operation.

V_{SS} [Ground]

Ground.

Block Diagram

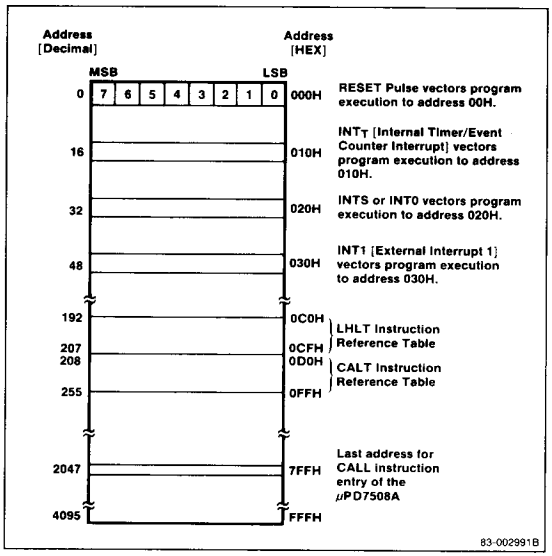


Functional Description

Program Memory

Figure 1 is a map of the 4096 x 8-bit program ROM.

Figure 1. Program Memory Map



Clock Control Circuit

The clock control circuit (figure 2) consists of a 4-bit clock mode register (bits CM_1 and CM_2), prescalers 1, 2, and 3, and a multiplexer. It takes the output of the system clock generator (CL) and count clock generator circuit (I). It also selects the clock source and divides the signal according to the setting in the clock mode register. It outputs the count pulse (CP) to the timer/event counter.

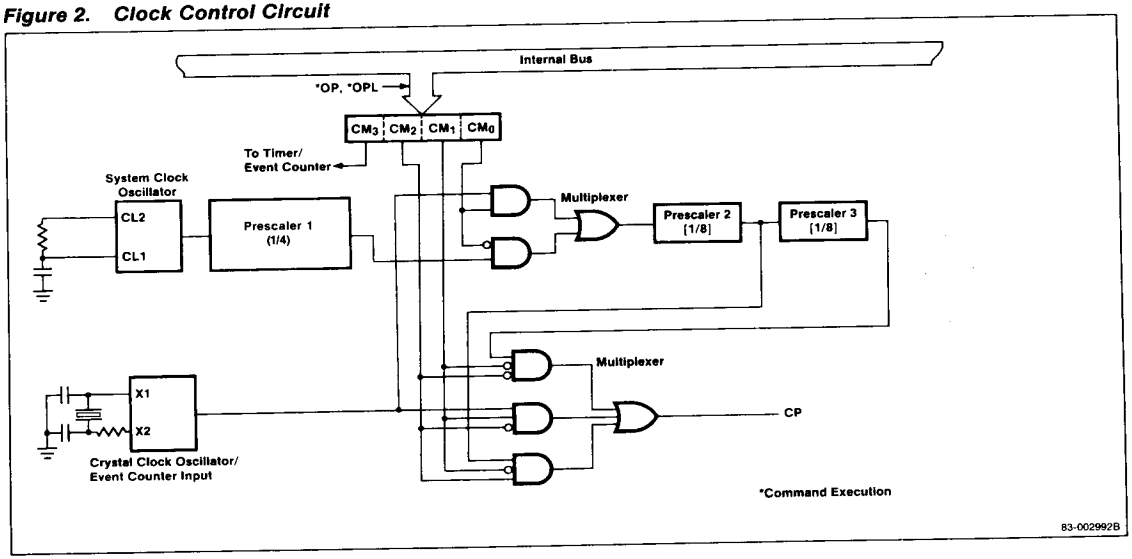
Table 1 lists the codes set in the clock mode register by the OP or OPL instruction to specify the count pulse frequency. Bit CM3 controls the timer out F/F; it is disabled when the bit is 0 and output when the bit is 1. When you set the clock mode register with the OP or OPL instruction, clear the high-order two bits of the accumulator.

Table 1. Selecting the Count Pulse Frequency

CM_2	CM_1	CM_0	Frequency Selected
0	0	0	CL/256
0	0	1	X/64
0	1	0	X
0	1	1	X
1	0	0	CL/32
1	0	1	X/8
1	1	0	Not used
1	1	1	Not used

CM_3	Timer F/F Signal
0	Enabled
1	Disabled

Figure 2. Clock Control Circuit



Timer/Event Counter

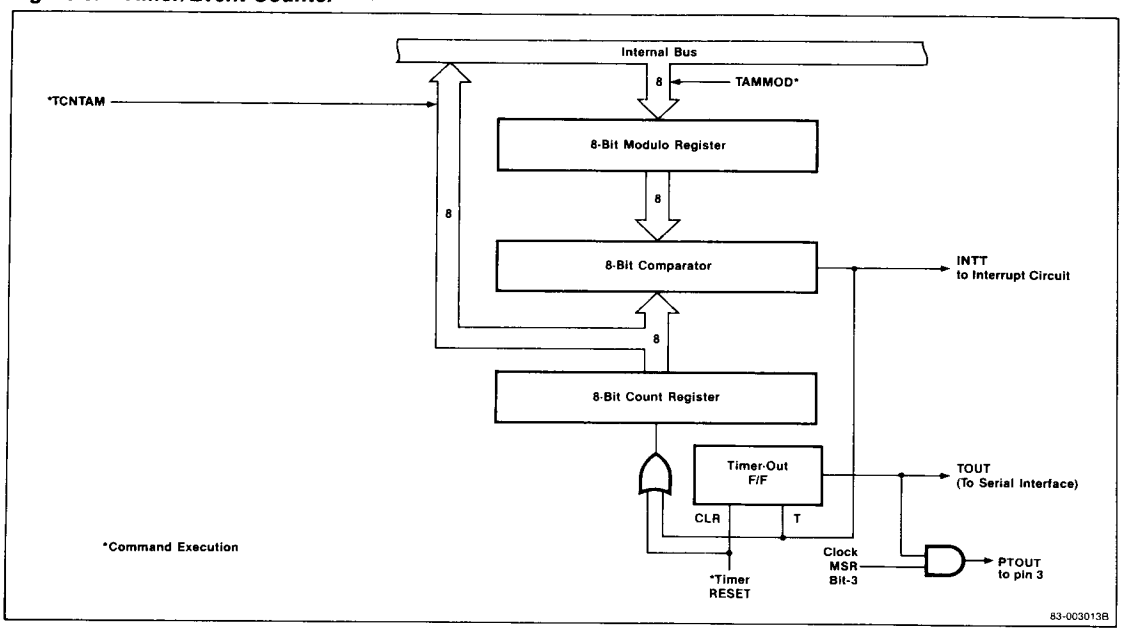
The timer/event counter consists of an 8-bit counter, an 8-bit modulo register, an 8-bit comparator, and a timer out flip flop, as shown in figure 3.

The 8-bit count register is a binary 8-bit up counter which is incremented each time a count pulse is input. The TIMER instruction, a RESET signal, or an INTT coincidence signal clears it to 00H.

The 8-bit modulo register determines the number of counts the count register holds. The TAMMOD instruction loads the contents of the modulo register. RESET sets the modulo register to FFH.

The 8-bit comparator compares the contents of the count register and those of the modulo register and outputs an INTT when they are equal.

Figure 3. Timer/Event Counter

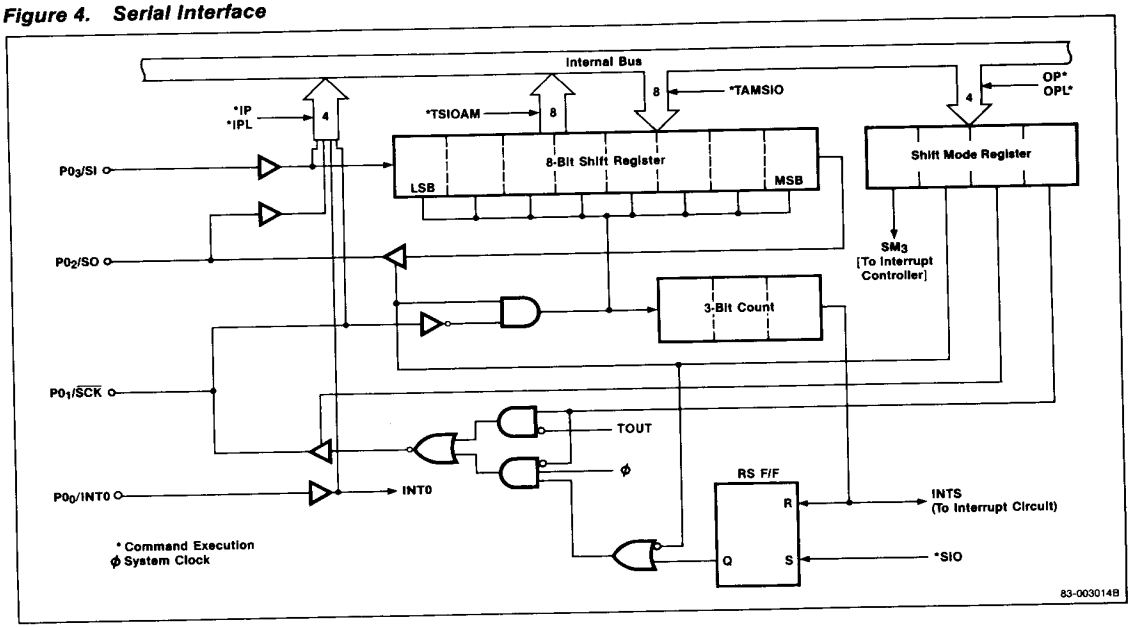


Serial Interface

The 8-bit serial interface allows the μPD7508A to communicate with peripheral devices such as the μPD7001 A/D converter, the μPD7227 dot matrix LCD controller/driver, and other microprocessors or microcomputers. Figure 4 shows the serial interface.

The serial interface consists of an 8-bit shift register, a 3-bit $\overline{SCK}$ pulse counter, the SI input port, the SO output port, the $\overline{SCK}$ serial clock I/O port, and a 4-bit serial mode select register (MSR). The MSR selects serial I/O or port 0 operation.

Figure 4. Serial Interface



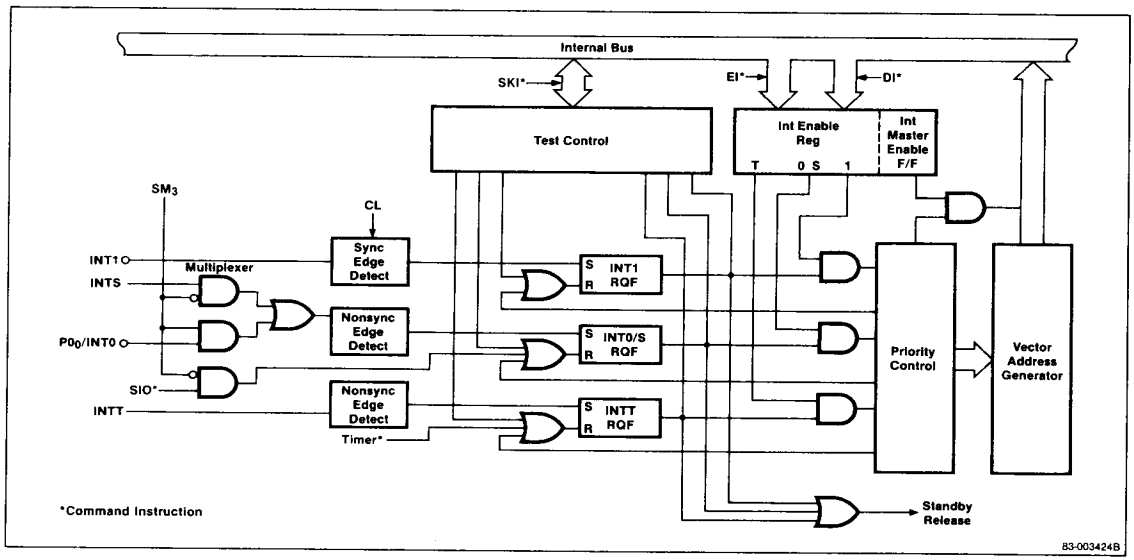
Interrupts

The μPD7508A has four vectored, prioritized interrupts. Two of these interrupts, INTT and INTS, are internally generated from the timer/event counter and serial interface, respectively. INT0 and INT1 are externally generated. Table 2 is a summary of the four interrupts. Figure 5 is a block diagram of the interrupts.

Table 2. μPD7508A Interrupts

Source	Function	Location	Priority	ROM Vector Address
INTT	Coincidence in timer/event counter	Internal	1	10H
INTS	Transfer complete signal from serial interface	Internal	2	20H
INT0	INT0 pin	External	2	20H
INT1	INT1 pin	External	3	30H

Figure 5. Interrupt Block Diagram



System Clock and Timing Circuitry

Timing for the μPD7508A is internally generated except for a frequency reference, which can be an RC circuit or an external clock source. Connect the frequency reference to the on-chip oscillator for the feedback phase shift required for oscillation. Figure 6 shows the connection for an RC circuit. Figures 6 and 7 show the connection for the frequency reference.

The internal oscillator generates a frequency in the range 60 kHz to 300 kHz depending on the frequency reference. For example, at $V_{DD} = 5$ V, an 83 kΩ resistor and a 33 pF capacitor generate a frequency of 200 kHz. The oscillation frequency is fed to the clock control circuit. It is divided by two and the resulting signal is fed to the CPU and serial interface as shown in figure 8.

Table 3 shows the operating status of the various logic blocks under the three power down modes.

Figure 6. RC Circuit Frequency Reference

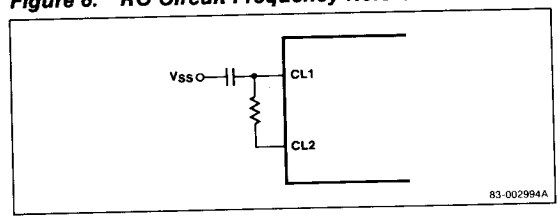


Figure 7. External Clock Frequency Reference

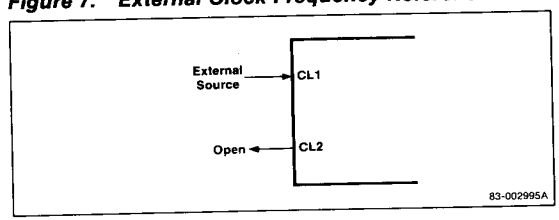


Figure 8. System Clock Circuitry

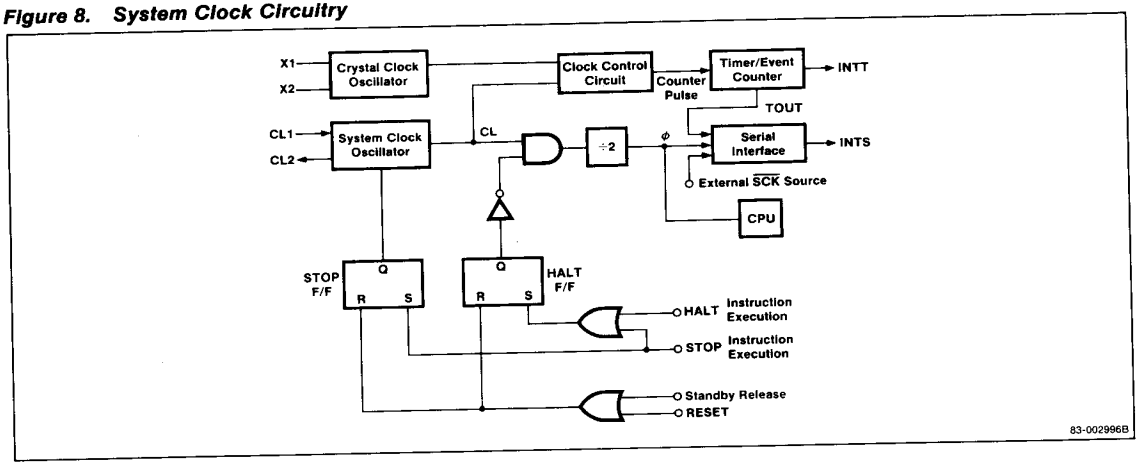


Table 3. Power Down Operating Status

Power Down Mode / Logic Block	HALT	STOP	Data Retention
System clock	(1)	Disabled	Disabled
X2	Normal	Normal	Disabled
CPU	Disabled	Disabled	Disabled
RAM	Data retained	Data retained	Data retained
Internal registers	Data retained	Data retained	Data retained
Timer/event counter	Normal	(3)	Disabled
Serial interface	(2)	(2)	Disabled
INT0	Normal	Normal	Disabled
INT1	Normal	Disabled	Disabled
RESET	Normal	Normal	(4)

Note:

(1) Supplied to timer/event counter but not to CPU or serial interface.

(2) Can function normally if the serial MSR is set to get the $\overline{SCK}$ signal externally or from the TOUT signal.

(3) Can function normally if the clock MSR is set to use X1 as the source for the count pulse.

(4) You must raise RESET while V_{DD} is lowered to enter data retention mode. Raise RESET when V_{DD} is raised, then lower it to end the data retention mode. INTT, INT0, INTS or RESET releases STOP mode. RESET or any interrupt releases HALT mode.

Absolute Maximum Ratings

$T_A = 25°C$

Operating temperature, T_{OPT}	−10 to 70°C
Storage temperature, T_{STG}	−65 to 150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
Input voltage, V_I	
Except ports 4-6	−0.3 to V_{DD} + 0.3 V
Ports 4-6	V_{DD} − 40 to V_{DD} + 0.3 V
Output voltage, V_O	
Except ports 3-6	−0.3 to V_{DD} + 0.3 V
Ports 3-6	V_{DD} − 40 to V_{DD} + 0.3 V
Output current, high, I_{OH}	
Single port, one pin except ports 3-6	−17 mA
Single port, one pin ports 3-6	−30 mA
All port pins	−150 mA
Output current, low, I_{OL}	
One pin	17 mA
All port pins	50 mA

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, $V_{DD} = 0$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	
Output capacitance	C_O			15	pF	Except port 3
	C_O			35	pF	Port 3
I/O capacitance	C_{IO}			15	pF	Except ports 4-6
	C_{IO}			35	pF	Ports 4-6

DC Characteristics

T_A = −10 to +70°C, V_{DD} = 2.7 to 5.5 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CL1, X1, ports 4-6
	V_{IH2}	V_{DD} − 0.5		V_{DD}	V	CL1, X1
	V_{IH3}	0.7 V_{DD}		V_{DD}	V	Ports 4-6; V_{DD} = 4.5 to 5.5 V
	V_{IH3}	V_{DD} − 0.5		V_{DD}	V	Ports 4-6; V_{DD} = 3 to 4.5 V
	V_{IH3}	2.5		V_{DD}	V	Ports 4-6; V_{DD} = 2.7 to 3 V
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.3 V_{DD}	V	Except CL1, X1, ports 4-6
	V_{IL2}	0		0.5	V	CL1, X1
	V_{IL3}	V_{DD} − 35		0.3 V_{DD}	V	Ports 4-6
Output voltage, high	V_{OH}	V_{DD} − 1.0			V	Except ports 3,6; I_{OH} = 1.0 mA, V_{DD} = 4.5 to 5.5 V
	V_{OH}	V_{DD} − 2.0			V	Ports 3, 6; I_{OH} = −8.0 mA; V_{DD} = 4.5 to 5.5 V
	V_{OH}	V_{DD} − 0.5			V	I_{OH} = −100 μA; V_{DD} = 2.7 to 5.5 V
Output voltage, low	V_{OL}			0.4	V	Except ports 3, 6; I_{OL} = 1.6 mA, V_{DD} = 4.5 to 5.5 V
	V_{OL}			0.5	V	Except ports 3, 6; I_{OL} = 400 μA; V_{DD} = 2.7 to 5.5 V
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1, ports 4-6; $V_I = V_{DD}$
	I_{LIH2}			10	μA	CL1, X1; $V_I = V_{DD}$
	I_{LIH3}			60	μA	Ports 4-6; $V_I = V_{DD}$
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1, ports 4-6; V_I = 0 V
	I_{LIL2}			−10	μA	CL1, X1; V_I = 0V
	I_{LIL3}			−30	μA	Ports 4-6; $V_I = V_{DD}$ − 35 V
Output leakage current, high	I_{LOH1}			3	μA	V_O == V_{DD} Except ports 4-6
	I_{LOH2}			30	μA	Ports 4-6; $V_O = V_{DD}$
Output leakage current, low	I_{LOL1}			−3	μA	V_O = 0 V
	I_{LOL2}			−30	μA	Ports 3-6; $V_O = V_{DD}$ − 35 V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode
Supply current	I_{DD1}		300	900	μA	Normal operation, V_{DD} = 5 V ±10%; R = 82 kΩ ±2%, C = 33 pF ±5%
	I_{DD1}		70	300	μA	Normal operation, V_{DD} = 3 V ±10%; R = 160 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		1	20	μA	Stop mode, V_{DD} = 5 V ±10% (1)
	I_{DD2}		0.3	10	μA	Stop mode, V_{DD} = 3 V ±10% (1)
	I_{DDDR}		0.3	10	μA	Data retention mode V_{DDDR} = 2.0 V

Note:

(1) X1 = 0 V; ports 4-6 output disabled or low level input.

AC Characteristics

$T_A = -10$ to 70°C, $V_{DD} = 2.7$ to 5.5 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	150	200	240	kHz	CL1, CL2, RC clock, R = 82 kΩ ±2%; C = 33 pF ±5% V_{DD} = 5 V ±10%, | ΔC/°C | ≤ 60 ppm
	f_{CC}	75	100	120	kHz	CL1, CL2, RC clock, R = 160 kΩ ±2%; C = 33 pF ± 5% V_{DD} = 3 V ±10%, | ΔC/°C | ≤ 60 ppm
	f_{CC}	75		135	kHz	CL1, CL2, RC clock, R = 160 kΩ ±2%; C = 33 pF ±5% | ΔC/°C | ≤ 60 ppm
	f_C	10		410	kHz	CL1, external clock, 50% duty, V_{DD} = 4.5 to 5.5 V
	f_C	10		125	kHz	CL1, external clock, 50% duty, V_{DD} = 2.7 V
System clock rise and fall times	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	1.1		50	μs	CL1, external clock, V_{DD} = 4.5 to 5.5 V
	t_{CH}, t_{CL}	3.5		50	μs	CL1, external clock, V_{DD} = 2.7 V
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		410	kHz	X1, external pulse input 50% duty, V_{DD} = 4.5 to 6.0 V
	f_X	0		135	kHz	X1, external pulse input 50% duty, V_{DD} = 2.7 V
Counter clock rise and fall times	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	1.1			μs	X1, external pulse input, V_{DD} = 4.5 to 5.5 V
	t_{XH}, t_{XL}	3.5			μs	X1, external pulse input, V_{DD} = 2.7 V
Port 1 output setup time to $\overline{PSTB}$ ↑	t_{PST}	(1)			μs	V_{DD} = 4.5 to 5.5 V
	t_{PST}	(2)			μs	
Port 1 output hold time from $\overline{PSTB}$ high	t_{STP}	0.1			μs	V_{DD} = 4.5 to 5.5 V
	t_{STP}	0.1			μs	
$\overline{PSTB}$ low pulse width	t_{STL}	(1)			μs	V_{DD} = 4.5 to 5.5 V
	t_{STL}	(2)			μs	
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	$\overline{SCK}$ as input, V_{DD} = 4.5 to 5.5 V
	t_{KCY}	5.0			μs	$\overline{SCK}$ as output, V_{DD} = 4.5 to 5.5 V
	t_{KCY}	7.0			μs	$\overline{SCK}$ as input
	t_{KCY}	14.0			μs	$\overline{SCK}$ as output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	1.3			μs	$\overline{SCK}$ as input, V_{DD} = 4.5 to 5.5 V
	t_{KH}, t_{KL}	2.2			μs	$\overline{SCK}$ as output, V_{DD} = 4.5 to 5.5 V
	t_{KH}, t_{KL}	3.3			μs	$\overline{SCK}$ as input
	t_{KH}, t_{KL}	6.5			μs	$\overline{SCK}$ as output

AC Characteristics (cont)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
SI setup time to $\overline{SCK}$ high	t_{SIK}	0.3			μs	
SI hold time after $\overline{SCK}$ high	t_{KSI}	0.45			μs	
SO delay time after $\overline{SCK}$ low	t_{SKO}			0.85	μs	V_{DD} = 4.5 to 6.0 V
	t_{SKO}			1.2	μs	
INT0 pulse width	t_{I0H}	10			μs	
	t_{I0L}	10			μs	
INT1 pulse width	t_{I1H}	(3)			μs	
	t_{I1L}	(3)			μs	
RESET pulse width	t_{RSH}	10			μs	
	t_{RSL}	10			μs	
RESET high set up time	t_{SRS}	0			ns	
RESET high hold time	t_{HRS}	0			ns	

Note:

(1) $f_{CC}/2 - 0.8$ or $f_C/2 - 0.8$

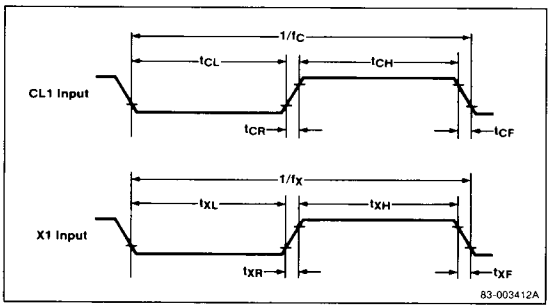
(2) $f_{CC}/2 - 0.3$ or $f_C/2 - 0.2$

(3) $2/f_{CC}$ or $2/f_C$

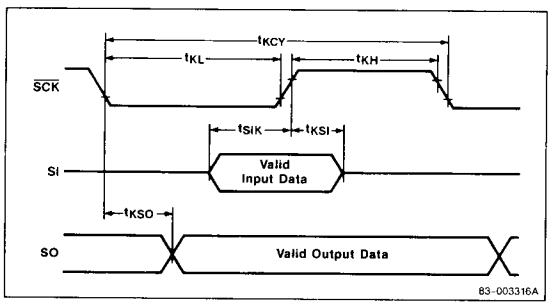
Timing Waveforms

Timing Test Points

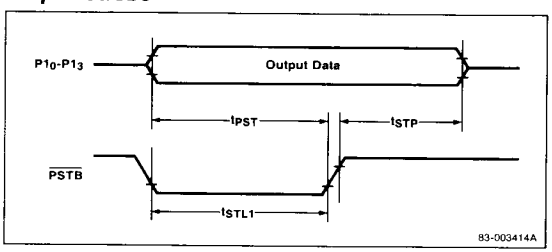
Clocks



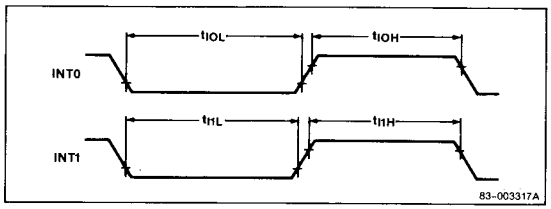
Serial Interface



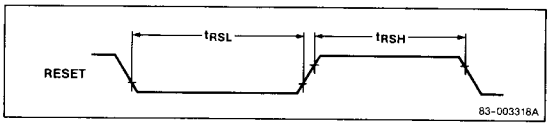
Output Strobe



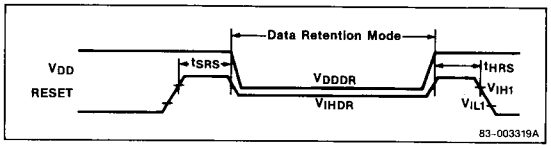
External Interrupts



RESET



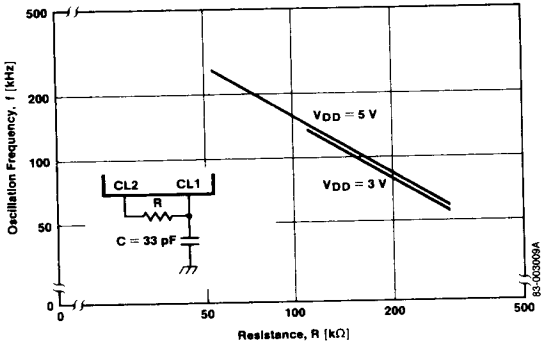
Data Retention Mode



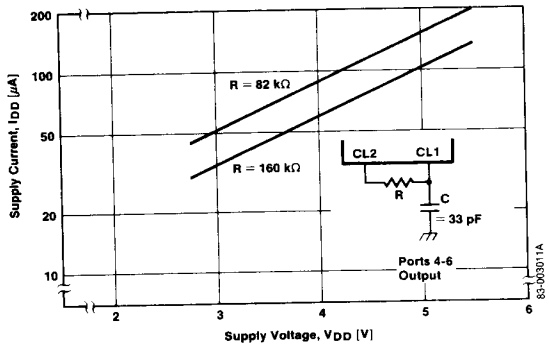
3

Operating Characteristics

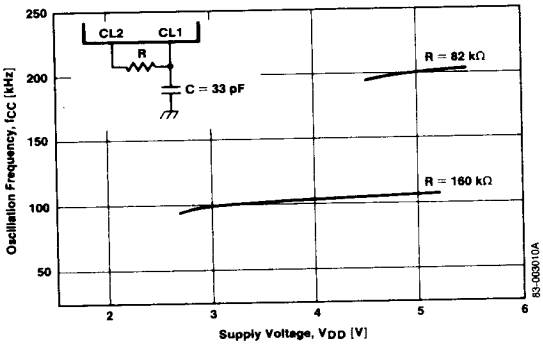
f vs R



IDD vs VDD [HALT Mode]



fCC vs VDD



IDD vs VDD [STOP Mode]