

# DSP56001

## 24-Bit General Purpose Digital Signal Processor

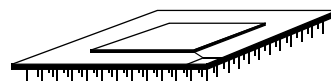
The DSP56001 is a member of Motorola's family of HCMOS, low-power, general purpose Digital Signal Processors. The DSP56001 features 512 words of full speed, on-chip program RAM (PRAM) memory, two 256 word data RAMs, two preprogrammed data ROMs, and special on-chip bootstrap hardware to permit convenient loading of user programs into the program RAM. It is an off-the-shelf part since the program memory is user programmable. The core of the processor consists of three execution units operating in parallel — the data ALU, the address generation unit, and the program controller. The DSP56001 has MCU-style on-chip peripherals, program and data memory, as well as a memory expansion port. The MPU-style programming model and instruction set make writing efficient, compact code, straightforward.

The high throughput of the DSP56001 makes it well-suited for communication, high-speed control, numeric processing, computer and audio applications. The key features which facilitate this throughput are:

- **Speed** At 16.5 million instructions per second (MIPS) with a 33 MHz clock, the DSP56001 can execute a 1024 point complex Fast Fourier Transform in 1.98 milliseconds (66,240 clock cycles).
- **Precision** The data paths are 24 bits wide thereby providing 144 dB of dynamic range; intermediate results held in the 56-bit accumulators can range over 336 dB.
- **Parallelism** The data ALU, address arithmetic units, and program controller operate in parallel so that an instruction prefetch, a 24x24-bit multiplication, a 56-bit addition, two data moves, and two address pointer updates using one of three types of arithmetic (linear, modulo, or reverse carry) can be executed in a single instruction cycle. This parallelism allows a four coefficient Infinite Impulse Response (IIR) filter section to be executed in only four cycles, the theoretical minimum for a single multiplier architecture.
- **Integration** In addition to the three independent execution units, the DSP56001 has six on-chip memories, three on-chip MCU style peripherals (Serial Communication Interface, Synchronous Serial Interface, and Host Interface), a clock generator and seven buses (three address and four data), making the overall system functionally complete and powerful, but also very low cost, low power, and compact.
- **Invisible Pipeline** The three-stage instruction pipeline is essentially invisible to the programmer thus allowing straightforward program development in either assembly language or a high-level language such as ANSI C.
- **Instruction Set** The 62 instruction mnemonics are MCU-like making the transition from programming microprocessors to programming the DSP56001 digital signal processor as easy as possible. The orthogonal syntax supports control of the parallel execution units. This syntax provides 12,808,830 different instruction variations using the 62 instruction mnemonics. The no-overhead DO instruction and the REPEAT (REP) instruction make writing straight-line code obsolete.
- **DSP56000/DSP56001 Compatibility** The DSP56001 is identical to the DSP56000 except that it has 512x24-bits of on-chip program RAM instead of 3.75K of program ROM; a 32x24-bit bootstrap ROM for loading the program RAM from either a byte-wide memory mapped ROM or via the Host Interface; and the on-chip X and Y Data ROMs have been preprogrammed as positive Mu- and A-Law to linear expansion tables and a full, four quadrant sine wave table, respectively.
- **Low Power** As a CMOS part, the DSP56001 is inherently very low power; however, three other features can reduce power consumption to an exceptionally low level.
  - The WAIT instruction shuts off the clock in the central processor portion of the DSP56001.
  - The STOP instruction halts the internal oscillator.
  - Power increases linearly (approximately) with frequency; thus, reducing the clock frequency reduces power consumption.

### Pin Grid Array (PGA)

Available in an 88 pin ceramic through-hole package.



### Ceramic Quad Flat Pack (CQFP)

Available in a 132 pin, small footprint, surface mount package.



### Plastic Quad Flat Pack (PQFP)

Available in a 132 pin, small footprint, surface mount package.



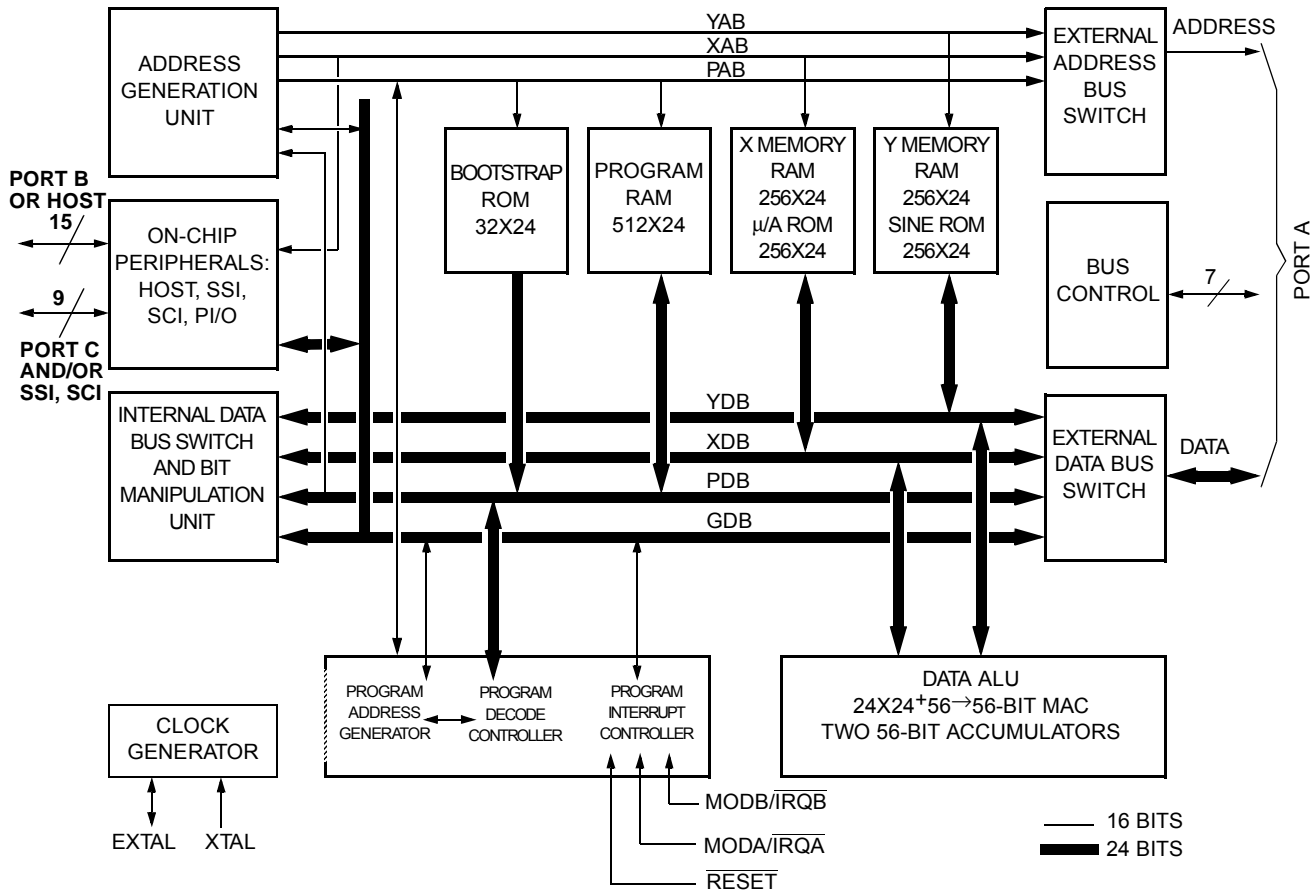


Figure 1. DSP56001 Block Diagram

**In the USA:**

For technical assistance call:  
 DSP Applications Helpline (512) 891-3230

For availability and literature call your local Freescale Sales Office or Authorized Freescale Distributor.

For free application software and information call the Dr. BuB electronic bulletin board:  
 9600/4800/2400/1200/300 baud  
 (512) 891-3771  
 (8 data bits, no parity, 1 stop)

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Contact your regional sales office or Freescale distributor.

## SIGNAL DESCRIPTION

The DSP56001 is available in 132 pin surface mount (CQFP and PQFP) or an 88-pin pin-grid array packaging. Its input and output signals are organized into seven functional groups which are listed below and shown in Figure 1.

- Port A Address and Data Buses
- Port A Bus Control
- Interrupt and Mode Control
- Power and Clock
- Host Interface or Port B I/O
- Serial Communications Interface or Port C I/O
- Synchronous Serial Interface or Port C I/O

## PORT A ADDRESS AND DATA BUS

### Address Bus (A0-A15)

These three-state output pins specify the address for external program and data memory accesses. To minimize power dissipation, A0-A15 do not change state when external memory spaces are not being accessed.

### Data Bus (D0-D23)

These pins provide the bidirectional data bus for external program and data memory accesses. D0-D23 are in the high-impedance state when the bus grant signal is asserted.

## PORT A BUS CONTROL

### Program Memory Select ( $\overline{PS}$ )

This three-state output is asserted only when external program memory is referenced. This pin is three-stated during  $\overline{RESET}$ .

### Data Memory Select ( $\overline{DS}$ )

This three-state output is asserted only when external data memory is referenced. This pin is three-stated during  $\overline{RESET}$ .

### X/Y Select ( $X/\overline{Y}$ )

This three-state output selects which external data memory space (X or Y) is referenced by data memory select ( $\overline{DS}$ ). This pin is three-stated during  $\overline{RESET}$ .

### Read Enable ( $\overline{RD}$ )

This three-state output is asserted to read external memory on the data bus D0-D23. This pin is three-stated during  $\overline{RESET}$ .

### Write Enable ( $\overline{WR}$ )

This three-state output is asserted to write external memory on the data bus D0-D23. This pin is three-stated during  $\overline{RESET}$ .

### Bus Request ( $\overline{BR}/\overline{WT}$ )

The bus request input  $\overline{BR}$  allows another device such as a processor or DMA controller to become the master of external data bus D0-D23 and external address bus A0-A15. When operating mode register (OMR) bit 7 is clear and  $\overline{BR}$  is asserted, the DSP56001 will always release the external data bus D0-D23, address bus A0-A15, and bus control pins  $\overline{PS}$ ,  $\overline{DS}$ ,  $X/\overline{Y}$ ,  $\overline{RD}$ , and  $\overline{WR}$  (i. e., Port A), by placing these pins in the high-impedance state after execution of the current instruction has been completed. **The  $\overline{BR}$  pin should be pulled up when not in use.**

If OMR bit 7 is set, this pin is an input that allows an external device to force wait states during an external Port A operation for as long as  $\overline{WT}$  is asserted.

### Bus Grant ( $\overline{BG}/\overline{BS}$ )

If OMR bit 7 is clear, this output is asserted to acknowledge an external bus request after Port A has been released. If OMR bit 7 is set, this pin is bus strobe and is asserted when the DSP accesses Port A. This pin is three-stated during  $\overline{RESET}$ .

## INTERRUPT AND MODE CONTROL

### Mode Select A/External Interrupt Request A ( $\overline{MODA}/\overline{IRQA}$ ),

### Mode Select B/External Interrupt Request B ( $\overline{MODB}/\overline{IRQB}$ )

These two inputs have dual functions: 1) to select the initial chip operating mode and 2) to receive an interrupt request from an external source.  $\overline{MODA}$  and  $\overline{MODB}$  are read and internally latched in the DSP when the processor exits the  $\overline{RESET}$  state. Therefore these two pins should be forced into the proper state during reset. After leaving the  $\overline{RESET}$  state, the  $\overline{MODA}$  and  $\overline{MODB}$  pins automatically change to external interrupt requests  $\overline{IRQA}$  and  $\overline{IRQB}$ . After leaving the reset state the chip operating mode can be changed by software.  $\overline{IRQA}$  and  $\overline{IRQB}$  may be programmed to be level sensitive or negative edge triggered. When edge triggered, triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal, however, the probability of noise on  $\overline{IRQA}$  or  $\overline{IRQB}$  generating multiple interrupts increases with increasing fall time of the interrupt signal. These pins are inputs during  $\overline{RESET}$ .

### Reset ( $\overline{RESET}$ )

This Schmitt trigger input pin is used to reset the DSP56001. When  $\overline{RESET}$  is asserted, the DSP56001 is initialized and placed in the reset state. When the  $\overline{RESET}$  signal is deasserted, the initial chip operating mode is latched from the  $\overline{MODA}$  and  $\overline{MODB}$  pins. When coming out of reset, deassertion occurs at a voltage level and is not directly related to the rise time of the reset signal; however, the probability of noise on  $\overline{RESET}$  generating multiple resets increases with increasing rise time of the reset signal.

## POWER AND CLOCK

### Power ( $V_{CC}$ ), Ground ( $GND$ )

There are five sets of power and ground pins used for the four groups of logic on the chip, two pairs for internal logic, one power and two ground for Port A address and control pins, one power and two ground for Port A data pins, and one pair for peripherals. Refer to the pin assignments in the **LAYOUT PRACTICES** section.

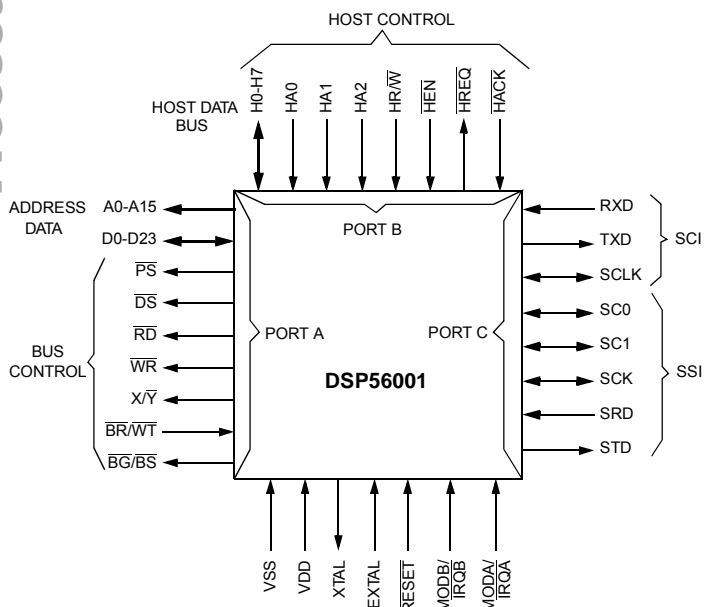


Figure 2. Functional Signal Groups

DSP56001

## External Clock/Crystal Input (EXTAL)

EXTAL may be used to interface the crystal oscillator input to an external crystal or an external clock.

## Crystal Output (XTAL)

This output connects the internal crystal oscillator output to an external crystal. If an external clock is used, XTAL should not be connected.

## HOST INTERFACE

### Host Data Bus (H0-H7)

This bidirectional data bus is used to transfer data between the host processor and the DSP56001. This bus is an input unless enabled by a host processor read. H0-H7 may be programmed as general purpose parallel I/O pins called PB0-PB7 when the Host Interface is not being used. These pins are configured as a GPIO input pins during hardware reset.

### Host Address (HA0-HA2)

These inputs provide the address selection for each Host Interface register. HA0-HA2 may be programmed as general purpose parallel I/O pins called PB8-PB10 when the Host Interface is not being used. These pins are configured as a GPIO input pins during hardware reset.

### Host Read/Write (HR $\overline{W}$ )

This input selects the direction of data transfer for each host processor access. HR $\overline{W}$  may be programmed as a general purpose I/O pin called PB11 when the Host Interface is not being used. This pin is configured as a GPIO input pins during hardware reset.

### Host Enable (H $\overline{EN}$ )

This input enables a data transfer on the host data bus. When H $\overline{EN}$  is asserted and HR $\overline{W}$  is high, H0-H7 become outputs, and DSP56001 data may be read by the host processor. When H $\overline{EN}$  is asserted and HR $\overline{W}$  is low, H0-H7 become inputs and host data is latched inside the DSP when H $\overline{EN}$  is deasserted. Normally a chip select signal, derived from host address decoding and an enable clock, is used to generate H $\overline{EN}$ . H $\overline{EN}$  may be programmed as a general purpose I/O pin called PB12 when the Host Interface is not being used. This pin is configured as a GPIO input pins during hardware reset.

### Host Request (H $\overline{REQ}$ )

This open-drain output signal is used by the DSP56001 Host Interface to request service from the host processor, DMA controller, or simple external controller. H $\overline{REQ}$  may be programmed as a general purpose I/O pin (not open-drain) called PB13 when the Host interface is not being used. H $\overline{REQ}$  should be pulled high when not in use. This pin is configured as a GPIO input pins during hardware reset.

### Host Acknowledge (H $\overline{ACK}$ )

This input has two functions: 1) to receive a Host Acknowledge handshake signal for DMA transfers and, 2) to receive a Host Interrupt Acknowledge compatible with MC68000 Family processors. H $\overline{ACK}$  may be programmed as a general purpose I/O pin called PB14 when the Host Interface is not being used. This pin is configured as a GPIO input pins during hardware reset. **H $\overline{ACK}$  should be pulled high when not in use.**

## SERIAL COMMUNICATIONS INTERFACE (SCI)

### Receive Data (RXD)

This input receives byte-oriented data into the SCI Receive Shift Register. Input data is sampled on the positive edge of the Receive Clock. RXD may be programmed as a general purpose I/O pin called PC0 when the SCI is not being used. This pin is configured as a GPIO input pins during hardware reset.

### Transmit Data (TXD)

This output transmits serial data from the SCI Transmit Shift Register. Data changes on the negative edge of the transmit clock. This output is stable on the positive edge of the transmit clock. TXD may be programmed as a general purpose I/O pin called PC1 when the SCI is not being used. This pin is configured as a GPIO input pins during hardware reset.

### SCI Serial Clock (SCLK)

This bidirectional pin provides an input or output clock from which the transmit and/or receive baud rate is derived in the asynchronous mode and from which data is transferred in the synchronous mode. SCLK may be programmed as a general purpose I/O pin called PC2 when the SCI is not being used. This pin is configured as a GPIO input pins during hardware reset.

## SYNCHRONOUS SERIAL INTERFACE (SSI)

### Serial Control Zero (SC0)

This bidirectional pin is used for control by the SSI. SC0 may be programmed as a general purpose I/O pin called PC3 when the SSI is not being used. This pin is configured as a GPIO input pins during hardware reset.

### Serial Control One (SC1)

This bidirectional pin is used for control by the SSI. SC1 may be programmed as a general purpose I/O pin called PC4 when the SSI is not being used. This pin is configured as a GPIO input pins during hardware reset.

### Serial Control Two (SC2)

This bidirectional pin is used for control by the SSI. SC2 may be programmed as a general purpose I/O pin called PC5 when the SSI is not being used. This pin is configured as a GPIO input pins during hardware reset.

### SSI Serial Clock (SCK)

This bidirectional pin provides the serial bit rate clock for the SSI when only one clock is used. SCK may be programmed as a general purpose I/O pin called PC6 when the SSI is not being used. This pin is configured as a GPIO input pins during hardware reset.

### SSI Receive Data (SRD)

This input pin receives serial data into the SSI Receive Shift Register. SRD may be programmed as a general purpose I/O pin called PC7 when the SSI is not being used. This pin is configured as a GPIO input pins during hardware reset.

### SSI Transmit Data (STD)

This output pin transmits serial data from the SSI Transmit Shift Register. STD may be programmed as a general purpose I/O pin called PC8 when the SSI is not being used. This pin is configured as a GPIO input pins during hardware reset.

**DSP56001 Electrical Characteristics  
Electrical Specifications**

The DSP is fabricated in high density CMOS with TTL compatible inputs and outputs.

**Maximum Ratings ( $V_{SS} = 0$  Vdc)**

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	-0.3 to +7.0	V
All Input Voltages	Vin	$V_{SS} - 0.5$ to $V_{cc} + 0.5$	V
Current Drain per Pin excluding Vcc and $V_{SS}$	I	10	mA
Operating Temperature Range	$T_J$	-40 to +105	°C
Storage Temperature	Tstg	-55 to +150	°C

**Maximum Electrical Ratings**

**Thermal Characteristics - PGA Package**

Characteristics	Symbol	Value	Rating
<b>Thermal Resistance - Ceramic</b>			
Junction to Ambient	$\theta_{JA}$	27	°C/W
Junction to Case (estimated)	$\theta_{JC}$	6.5	°C/W

**Thermal Characteristics - CQFP Package**

Characteristics	Symbol	Value	Rating
<b>Thermal Resistance - Ceramic</b>			
Junction to Ambient	$\theta_{JA}$	40	°C/W
Junction to Case (estimated)	$\theta_{JC}$	7.0	°C/W

**Thermal Characteristics - PQFP Package**

Characteristics	Symbol	Value	Rating
<b>Thermal Resistance - Plastic</b>			
Junction to Ambient	$\theta_{JA}$	38	°C/W
Junction to Case (estimated)	$\theta_{JC}$	13.0	°C/W

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either Gnd or Vcc).

## DSP56001 Electrical Characteristics

### Power Considerations

The average chip-junction temperature,  $T_J$ , in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

$T_A$  = Ambient Temperature, °C

$\Theta_{JA}$  = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$ , Watts - Chip Internal Power

$P_{I/O}$  = Power Dissipation on Input and Output Pins - User Determined

For most applications  $P_{I/O} \ll P_{INT}$  and can be neglected; however,  $P_{I/O} + P_{INT}$  **must not** exceed  $P_d$ . An appropriate relationship between  $P_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is:

$$P_D = K/(T_J + 273^\circ \text{C}) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273^\circ \text{C}) + \Theta_{JA} \times P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation (2) by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving equations (1) and (2) iteratively for any value of  $T_A$ . The total thermal resistance of a package ( $\Theta_{JA}$ ) can be separated into two components,  $\Theta_{JC}$  and  $C_A$ , representing the barrier to heat flow from the semiconductor junction to the package (case) surface ( $\Theta_{JC}$ ) and from the case to the outside ambient ( $C_A$ ). These terms are related by the equation:

$$\Theta_{JA} = \Theta_{JC} + C_A \quad (4)$$

$\Theta_{JC}$  is device related and cannot be influenced by the user. However,  $C_A$  is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling, and thermal convection. Thus, good thermal management on the part of the user can significantly reduce  $C_A$  so that  $\Theta_{JA}$  approximately equals  $\Theta_{JC}$ . Substitution of  $\Theta_{JC}$  for  $\Theta_{JA}$  in equation (1) will result in a lower semiconductor junction temperature. Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in Freescale Reliability Report 7843, "Thermal Resistance Measurement Method for MC68XX Microcomponent Devices", and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User-derived values for thermal resistance may differ.

### Layout Practices

Each Vcc pin on the DSP56001 should be provided with a low-impedance path to +5 volts. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive four distinct groups of logic on chip. They are:

Vcc	GND	Function
G12,C6	G11,B7	Internal Logic supply pins
L8	L6,L9	Address bus output buffer supply pins
G3	D3,J3	Data bus output buffer supply pins
C9	E11	Port B and C output buffer supply pins

**Power and Ground Connections for PGA**

Vcc	GND	Function
35, 36, 128, 129	33, 34, 130, 131	Internal Logic supply pins
63, 64	55, 56, 73, 74	Address bus output buffer supply pins
100, 101	90, 91, 111, 112	Data bus output buffer supply pins
12, 13	23, 24	Port B and C output buffer supply pins

**Power and Ground Connections for CQFP and PQFP**

## DSP56001 Electrical Characteristics

### Power and Ground Connections

The Vcc power supply should be bypassed to ground using at least four 0.1 uF by-pass capacitors located either underneath the chip or as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip Vcc and Gnd should be kept to less than 1/2" per capacitor lead. A four-layer board is recommended, employing two inner layers as Vcc and Gnd planes. All output pins on the DSP56001 have fast rise and fall times — typically less than 3 ns. with a 10 pf. load. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses as well as the  $\overline{RD}$ ,  $\overline{WR}$ ,  $\overline{IRQA}$ ,  $\overline{IRQB}$ , and  $\overline{HEN}$  pins. Maximum PC trace lengths on the order of 6" are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the Vcc and GND circuits. Pull up/down all unused inputs or signals that will be inputs during reset.

### Signal Stability

When designing hardware to interface with the Host Interface, it is important to ensure that all signals be clean and free from noise. Particular attention should be given to the quality of the Host Enable ( $\overline{HEN}$ ). All inputs to the port should be stable when  $\overline{HEN}$  is asserted and should remain stable until  $\overline{HEN}$  has fully returned to the deasserted state. It is important to note that such phenomena as ground-bounce and cross-talk can inadvertently cause  $\overline{HEN}$  to temporarily rise above  $V_{il\ max}$ . Should this occur without completing the full logic transition to  $V_{ih\ min}$ , the DSP56001 Host Port may not correctly update the port status information which can result in storing two or more copies of a single down loaded data word. Of course, if a full logic transition occurs, the part will complete a normal data transfer operation.

DSP56001 Electrical Characteristics

DC Electrical Characteristics (Vcc = 5.0 Vdc ± 10%; Tj = -40 to +105° C at 20.5 MHz and 27 MHz)  
(Vcc = 5.0 Vdc ± 5%; Tj = -40 to +105° C at 33 MHz)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage 20, 27 MHz 33 MHz	Vcc	4.5 4.75	5.0	5.5 5.25	V
Input High Voltage Except EXTAL, $\overline{\text{RESET}}$ , $\overline{\text{MODA/IRQA}}$ , $\overline{\text{MODB/IRQB}}$	V <sub>IH</sub>	2.0	—	Vcc	V
Input Low Voltage Except EXTAL, $\overline{\text{MODA/IRQA}}$ , $\overline{\text{MODB/IRQB}}$	V <sub>IL</sub>	-0.5	—	0.8	V
Input High Voltage EXTAL	V <sub>IHC</sub>	4.0	—	Vcc	V
Input Low Voltage EXTAL	V <sub>ILC</sub>	-0.5	—	0.6	V
Input High Voltage $\overline{\text{RESET}}$	V <sub>IHR</sub>	2.5	—	Vcc	V
Input High Voltage MODA/IRQA and MODB/IRQB	V <sub>IHM</sub>	3.5	—	Vcc	V
Input Low Voltage MODA/IRQA and MODB/IRQB	V <sub>ILM</sub>	-0.5	—	2.0	V
Input Leakage Current EXTAL, $\overline{\text{RESET}}$ , $\overline{\text{MODA/IRQA}}$ , $\overline{\text{MODB/IRQB}}$ , $\overline{\text{BR}}$	I <sub>in</sub>	-1	—	1	uA
Three-State (Off-State) Input Current (@2.4 V/0.4 V)	I <sub>TSI</sub>	-10	—	10	uA
Output High Voltage (I <sub>OH</sub> = -0.4 mA)	V <sub>OH</sub>	2.4	—	—	V
Output Low Voltage (I <sub>OL</sub> = 1.6 mA; RD, WR I <sub>OL</sub> = 1.6 mA; Open Drain HREQ I <sub>OL</sub> = 6.7 mA, TXD IOL = 6.7 mA)	V <sub>OL</sub>	—	—	0.4	V
Total Supply Current 5.25 V, 33 MHz 5.5 V, 27 MHz 5.5 V, 20 MHz in WAIT Mode (see Note 1) in STOP Mode (see Note 1)	I <sub>DD33</sub> I <sub>DD27</sub> I <sub>DD20</sub> I <sub>DDW</sub> I <sub>DDS</sub>	— — — — —	160 130 100 10 100	185 155 115 25 2000	mA mA mA mA uA
Input Capacitance (see Note 2)	Cin	—	10	—	pf

Notes:

1. In order to obtain these results all inputs must be terminated (i.e., not allowed to float).
2. Periodically sampled and not 100% tested.



## DSP56001 Electrical Characteristics

### AC Electrical Characteristics

The timing waveforms in the **AC Electrical Characteristics** are tested with a  $V_{IL}$  maximum of 0.5 V and a  $V_{IH}$  minimum of 2.4 V for all pins, except EXTAL, RESET, MODA, and MODB. These four pins are tested using the input levels set forth in the **DC Electrical Characteristics**. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56001 output levels are measured with the production test machine  $V_{OL}$  and  $V_{OH}$  reference levels set at 0.8 V and 2.0 V respectively.

### AC Electrical Characteristics - Clock Operation

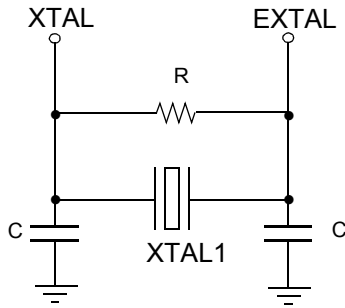
The DSP56001 system clock may be derived from the on-chip crystal oscillator as shown in Clock Figure 1, or it may be externally supplied. An externally supplied square wave voltage source should be connected to EXTAL, leaving XTAL physically unconnected (see Clock Figure 2) to the board or socket. The rise and fall time of this external clock should be 5 ns maximum.

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
	Frequency of Operation (EXTAL Pin)	4.0	20.5	4.0	27.0	4.0	33.0	MHz
1	External Clock Input High (tch) — EXTAL Pin (see Note 1 and 2)	22	150	17	150	13.5	150	ns
2	External Clock Input Low (tcl) — EXTAL Pin (see Note 1 and 2)	22	150	17	150	13.5	150	ns
3	Clock Cycle Time = cyc = 2T	48.75	250	37	250	30.33	250	ns
4	Instruction Cycle Time = lcy = 4T	97.5	500	74	500	60	500	ns

#### Notes:

- External Clock Input High and External Clock Input Low are measured at 50% of the input transition. tch and tcl are dependent on the duty cycle.
- $T = lcy / 4$  is used in the electrical characteristics. T represents an average which is independent of the duty cycle.

**DSP56001 Electrical Characteristics**



**Fundamental Frequency  
Crystal Oscillator**

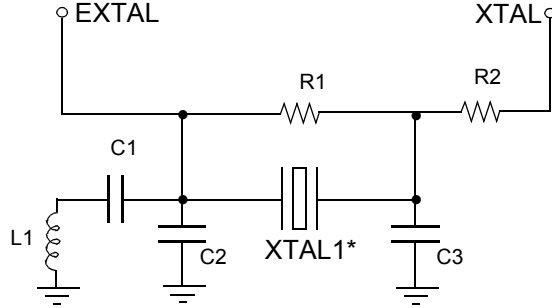
Suggested Component Values

**For  $f_{osc} = 4$  MHz:**  
 $R = 680\text{ K}\Omega \pm 10\%$   
 $C = 20\text{ pf} \pm 20\%$

**For  $f_{osc} = 30$  MHz:**  
 $R = 680\text{ K}\Omega \pm 10\%$   
 $C = 20\text{ pf} \pm 20\%$

Notes:

(1) The suggested crystal source is ICM, # 433163 - 4.00 (4MHz fundamental, 20 pf load) or # 436163 - 30.00 (30 MHz fundamental, 20 pf load).



**3<sup>rd</sup> Overtone  
Crystal Oscillator**

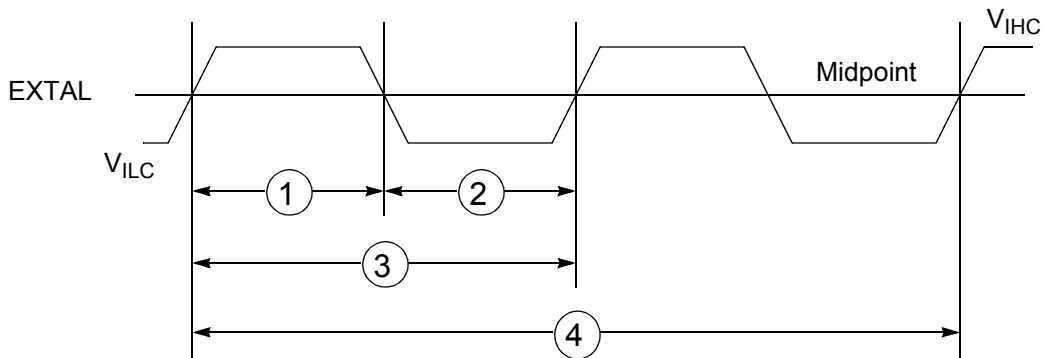
Suggested Component Values

$R1 = 470\text{ K}\Omega \pm 10\%$   
 $R2 = 330\ \Omega \pm 10\%$   
 $C1 = 0.1\ \mu\text{f} \pm 20\%$   
 $C2 = 26\text{ pf} \pm 20\%$   
 $C3 = 20\text{ pf} \pm 10\%$   
 $L1 = 2.37\ \mu\text{H} \pm 10\%$   
 $XTAL = 33\text{ MHz, AT cut, 20 pf load, } 50\ \Omega \text{ max series resistance}$

Notes:

(1) \*3<sup>rd</sup> overtone crystal.  
 (2) The suggested crystal source is ICM, # 471163 - 33.00 (33 MHz 3<sup>rd</sup> overtone, 20 pf load).  
 (3) R2 limits crystal current  
 (4) Reference Benjamin Parzen, The Design of Crystal and Other Harmonic Oscillators, John Wiley & Sons, 1983

**Clock Figure 1. Crystal Oscillator Circuits**



**Note:** The midpoint is  $V_{ILC} + 0.5(V_{IHC} - V_{ILC})$ .

**Clock Figure 2. External Clock Timing**

DSP56001 Electrical Characteristics

AC Electrical Characteristics - Reset, Stop, Mode Select and Interrupt Timing

(Vcc = 5.0 Vdc ±10%, Tj = -40 to +105° C, CL = 50 pf + 1 TTL Load at 20.5 MHz and 27 MHz)

(Vcc = 5.0 Vdc ± 5%, Tj = -40 to +105° C, CL = 50 pf + 1 TTL Load at 33 MHz)

(See Control Figure 1 through 8)

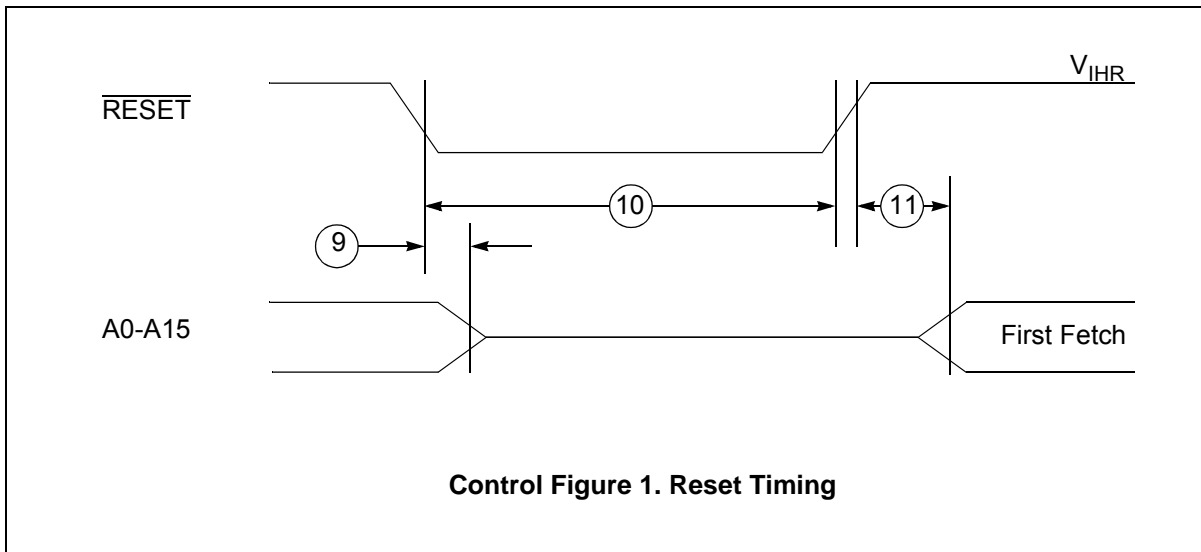
cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles

WS = Number of wait states (1 WS = 1 cyc = 2T) programmed into external bus access using BCR (WS = 0 - 15)

tch = Clock high period

tcl = Clock low period

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
9	Delay from $\overline{\text{RESET}}$ Assertion to Address High Impedance (periodically sampled and not 100% tested)	—	50	—	38	—	31	ns
10	Minimum Stabilization Duration Internal Osc. (see Note 1) External Clock (see Note 2)	75000*cyc 25*cyc	— —	75000*cyc 25*cyc	— —	75000*cyc 25*cyc	— —	ns ns
11	Delay from Asynchronous $\overline{\text{RESET}}$ Deassertion to First External Address Output (Internal Reset Negation)	8*cyc	9*cyc+40	8*cyc	9*cyc+31	8*cyc	9*cyc+25	ns
12	Synchronous Reset Setup Time from $\overline{\text{RESET}}$ Deassertion to Falling Edge of External Clock	20	cyc-10	15	cyc-8	13	cyc-7	ns
13	Synchronous Reset Delay Time from the Synchronous Falling Edge of External Clock to the First External Address Output	8*cyc+5	8*cyc+30	8*cyc+5	8*cyc+23	8*cyc+5	8*cyc+19	ns
14	Mode Select Setup Time	100	—	77	—	62	—	ns
15	Mode Select Hold Time	0	—	0	—	0	—	ns
16	Edge-Triggered Interrupt Request							
16a	assertion	25	—	17	—	16	—	ns
	deassertion	15	—	10	—	10	—	ns



**DSP56001 Electrical Characteristics**

**AC Electrical Characteristics - Reset, Stop, Mode Select, and Interrupt Timing  
(Continued)**

**NOTE**

When using fast interrupts and  $\overline{IRQA}$  and  $\overline{IRQB}$  are defined as *level-sensitive*, then timings 19 through 22 apply to prevent multiple interrupt service. To avoid these timing restrictions, the negative edge-triggered mode is recommended when using fast interrupt. Long interrupts are recommended when using level-sensitive mode.

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
17	Delay from $\overline{IRQA}$ , $\overline{IRQB}$ Assertion to External Memory Access Address Out Valid Caused by First Interrupt Instruction Fetch Instruction Execution	5 <sub>*</sub> cyc+tch	—	5 <sub>*</sub> cyc+tch	—	5 <sub>*</sub> cyc+tch	—	ns
		9 <sub>*</sub> cyc+tch	—	9 <sub>*</sub> cyc+tch	—	9 <sub>*</sub> cyc+tch	—	ns
18	Delay from $\overline{IRQA}$ , $\overline{IRQB}$ Assertion to General Purpose Transfer Output Valid Caused by First Interrupt Instruction Execution	11+cyc+tch	—	11 <sub>*</sub> cyc+tch	—	11 <sub>*</sub> cyc+tch	—	ns
19	Delay from Address Output Valid Caused by First Interrupt Instruction Execution to Interrupt Request Deassertion for Level Sensitive Fast Interrupts	—	2 <sub>*</sub> cyc+tcl+ (cyc <sub>*</sub> WS) -44	—	2 <sub>*</sub> cyc+tcl+ (cyc <sub>*</sub> WS) -34	—	2 <sub>*</sub> cyc+tcl+ (cyc <sub>*</sub> WS) -27	ns
20	Delay from $\overline{RD}$ Assertion to Interrupt Request Deassertion for Level Sensitive Fast Interrupts	—	2 <sub>*</sub> cyc+ (cyc <sub>*</sub> WS) -40	—	2 <sub>*</sub> cyc+ (cyc <sub>*</sub> WS) -31	—	2 <sub>*</sub> cyc+ (cyc <sub>*</sub> WS) -25	ns
21	Delay from $\overline{WR}$ Assertion to WS=0 Interrupt Request Deassertion for WS>0 Level Sensitive Fast Interrupts	—	2 <sub>*</sub> cyc-40 cyc+tcl+ (cyc <sub>*</sub> WS) -40	—	2 <sub>*</sub> cyc-31 cyc+tcl+ (cyc <sub>*</sub> WS) -31	—	2 <sub>*</sub> cyc-25 cyc+tcl+ (cyc <sub>*</sub> WS) -25	ns ns
22	Delay from General-Purpose Output Valid to Interrupt Request Deassertion for Level Sensitive Fast Interrupts - If Second Interrupt Instruction is: Single Cycle Two Cycle	—	tcl-60	—	tcl-46	—	tcl-37	ns
		—	(2 <sub>*</sub> cyc)+tcl -60	—	(2 <sub>*</sub> cyc)+tcl -46	—	(2 <sub>*</sub> cyc)+tcl -37	ns

**DSP56001 Electrical Characteristics**

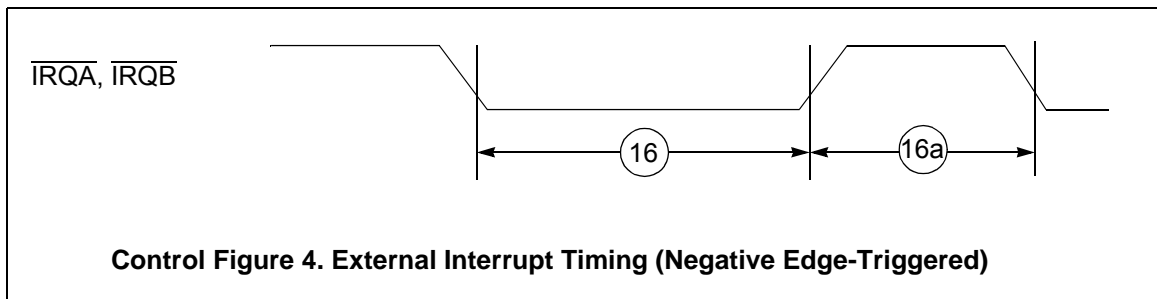
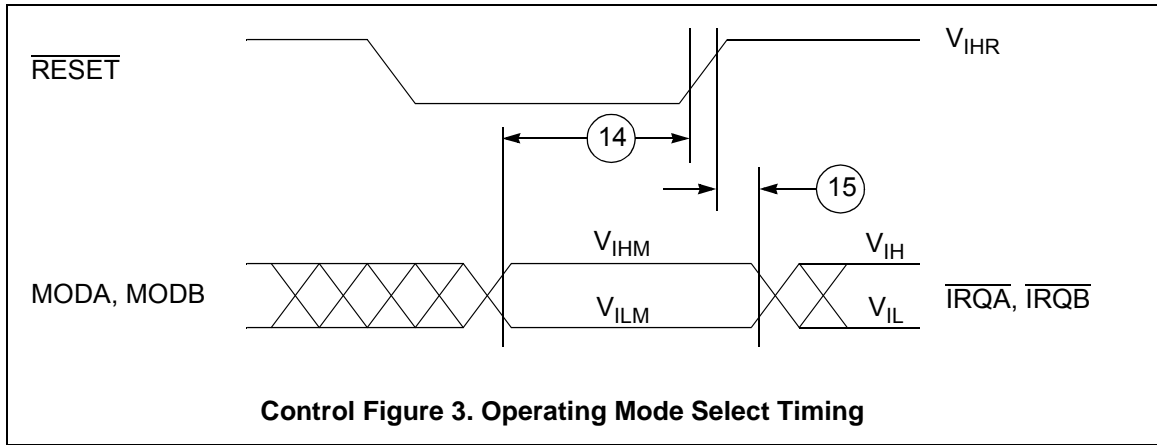
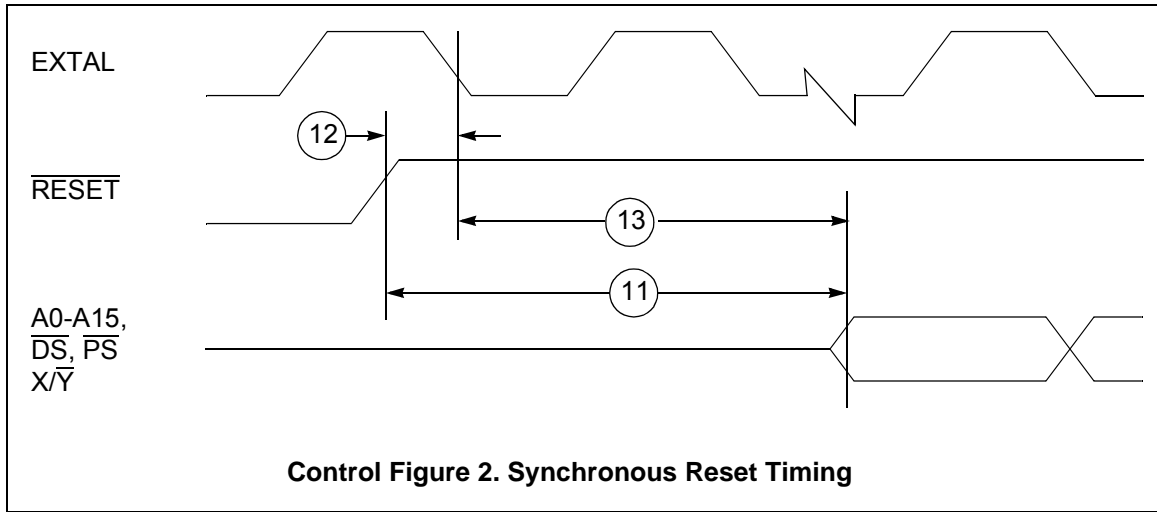
**AC Electrical Characteristics - Reset, Stop, Mode Select, and Interrupt Timing  
(Continued)**

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
23	Synchronous Interrupt Setup Time from $\overline{IRQA}$ , $\overline{IRQB}$ Assertion to the Synchronous Rising Edge of External Clock (see Notes 5, 6)	25	cyc-10	19	cyc-8	16	cyc-7	ns
24	Synchronous Interrupt Delay Time from the Synchronous Rising Edge of External Clock to the First External Address Output Valid Caused by the First Instruction Fetch after Coming out of Wait State (see Notes 3, 5)	13 <sub>*</sub> cyc+ tch+8	13 <sub>*</sub> cyc+ tch+30	13 <sub>*</sub> cyc+ tch+6	13 <sub>*</sub> cyc+ tch+23	13 <sub>*</sub> cyc+ tch+5	13 <sub>*</sub> cyc+ tch+19	ns
25	Duration for $\overline{IRQA}$ Assertion to Recover from Stop State (see Note 4)	25	—	19	—	16	—	ns
26	Delay from $\overline{IRQA}$ Assertion to Fetch of First Instruction (for Stop) for Internal Osc / OMR bit 6 = 0 External Clock / OMR bit 6 = 1 (see Notes 1, 2, and 7)	65545 <sub>*</sub> cyc	—	65545 <sub>*</sub> cyc	—	65545 <sub>*</sub> cyc	—	ns
		17 <sub>*</sub> cyc	—	17 <sub>*</sub> cyc	—	17 <sub>*</sub> cyc	—	ns
27	Duration for Level Sensitive $\overline{IRQA}$ Assertion to Fetch of First Interrupt Instruction (for Stop) for Internal Osc / OMR bit 6 = 0 External Clock / OMR bit 6 = 1 (see Notes 1, 2, and 7)	65533 <sub>*</sub> cyc +tcl	—	65533 <sub>*</sub> cyc +tcl	—	65533 <sub>*</sub> cyc +tcl	—	ns
		5 <sub>*</sub> cyc+tcl	—	5 <sub>*</sub> cyc+tcl	—	5 <sub>*</sub> cyc+tcl	—	ns
28	Delay from Level Sensitive $\overline{IRQA}$ Assertion to Fetch of First Interrupt Instruction (for Stop) for Internal Osc / OMR bit 6 = 0 External Clock / OMR bit 6 = 1 (see Notes 1, 2, and 7)	65545 <sub>*</sub> cyc	—	65545 <sub>*</sub> cyc	—	65545 <sub>*</sub> cyc	—	ns
		17 <sub>*</sub> cyc	—	17 <sub>*</sub> cyc	—	17 <sub>*</sub> cyc	—	ns

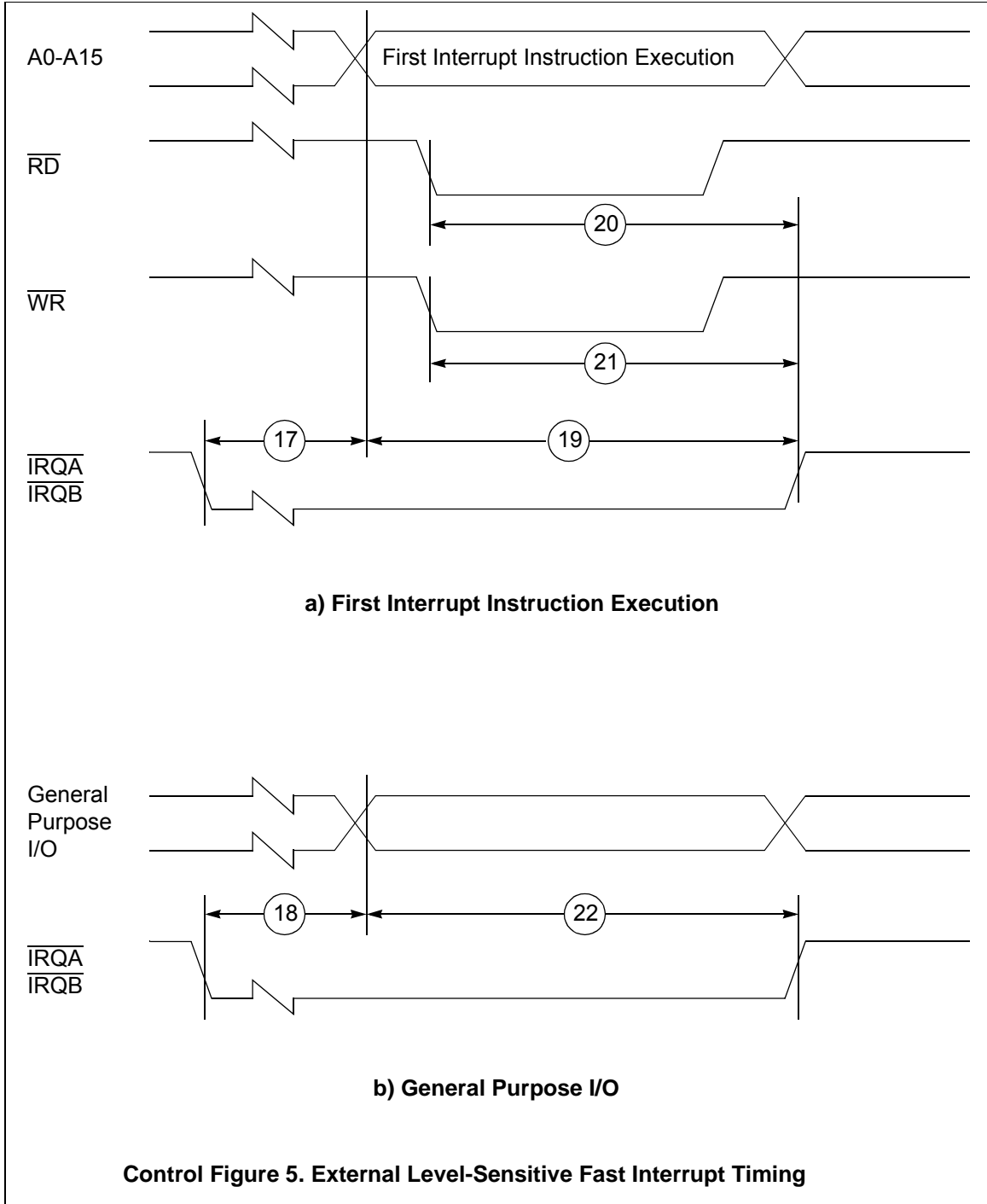
**Notes:**

- A clock stabilization delay is required when using the on-chip crystal oscillator in two cases:
  - after power-on reset, and
  - when recovering from Stop mode.
 During this stabilization period, T will not be constant. Since this stabilization period varies, a delay of 150,000T is typically allowed to assure that the oscillator is stabilized before executing programs. While it is possible to set OMR bit 6 = 1 when using the internal crystal oscillator, it is not recommended and these specifications do not guarantee timings for that case. See Section 8.5 in the *DSP56000/DSP56001 User's Manual* for additional information.
- Circuit stabilization delay is required during reset when using an external clock in two cases:
  - after power-on reset, and
  - when recovering from Stop mode.
- For Revision B silicon, the min and max numbers are 12cyc+Tch+8 and 12cyc+Tch+30, respectively.
- The minimum is specified for the duration of an edge triggered  $\overline{IRQA}$  interrupt required to recover from the STOP state without having the  $\overline{IRQA}$  interrupt accepted.
- Timing #23 is for all IRQx interrupts while timing #24 is only when exiting WAIT.
- Timing #23 triggers off T1 in the normal state and off T1/T3 when exiting the WAIT state.
- The timings in the table are for Rev. C parts. The timings for Rev. C parts are shorter by 1 cyc than the Rev. B parts when OMR6=0.

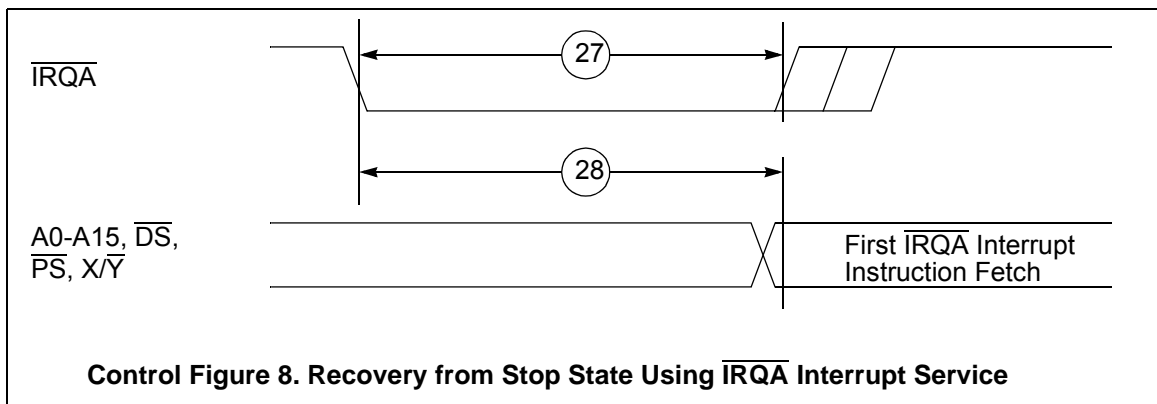
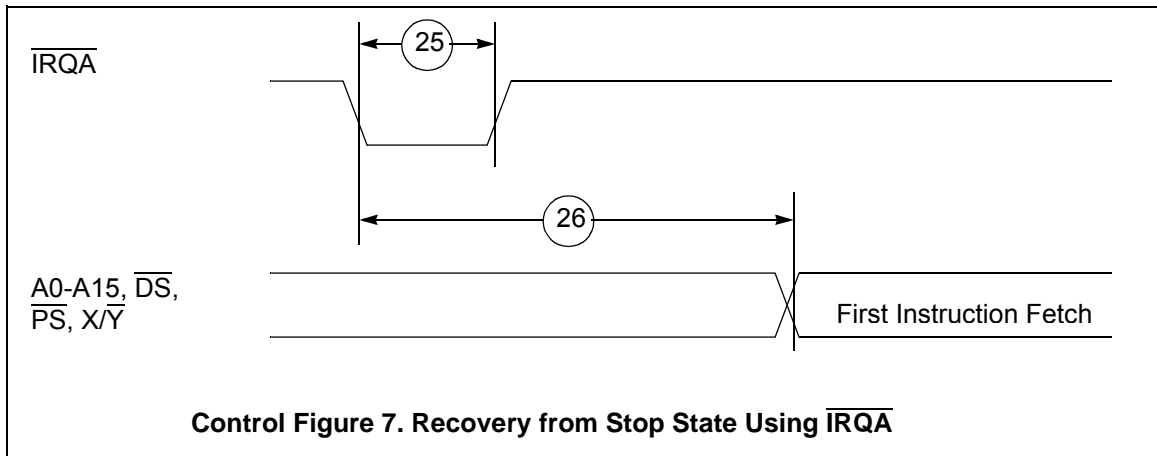
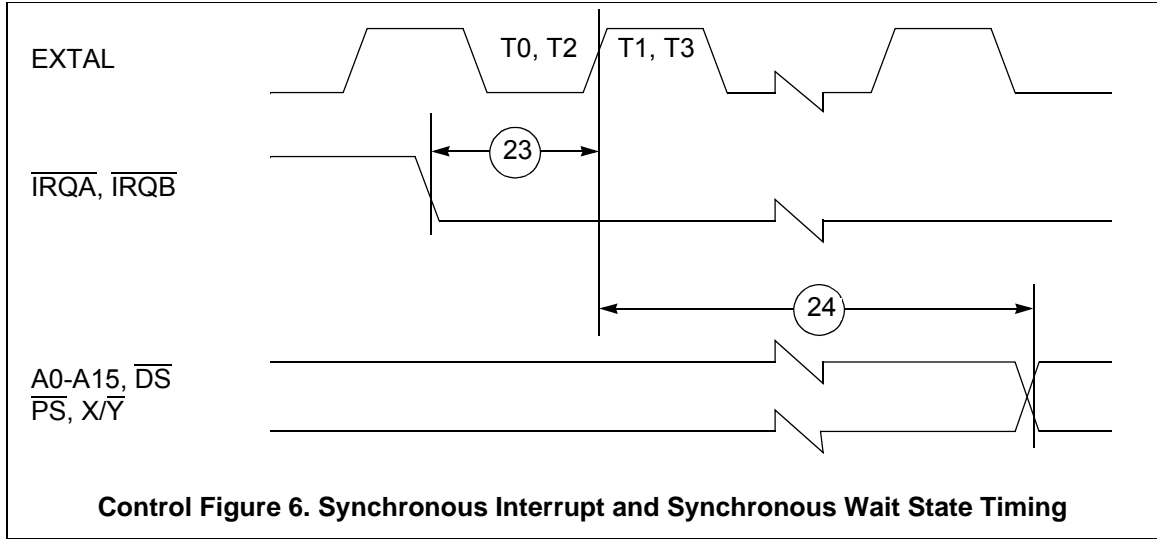
DSP56001 Electrical Characteristics



DSP56001 Electrical Characteristics



DSP56001 Electrical Characteristics





## DSP56001 Electrical Characteristics HOST PORT USAGE CONSIDERATIONS

Careful synchronization is required when reading multibit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected. The situation exists in the Host port. The considerations for proper operation are discussed below.

### Host Programmer Considerations

1. **Unsynchronized Reading of Receive Byte Registers**  
When reading receive byte registers, RXH, RXM, or RXL, the Host programmer should use interrupts or poll the RXDF flag which indicates that data is available. This assures that the data in the receive byte registers will be stable.
2. **Overwriting Transmit Byte Registers**  
The Host programmer should not write to the transmit byte registers, TXH, TXM, or TXL, unless the TXDE bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers will transfer valid data to the HRX register.
3. **Synchronization of Status Bits from DSP to Host**  
HC, HREQ, DMA, HF3, HF2, TRDY, TXDE, and RXDF (refer to *DSP56000/DSP56001 User's Manual*, I/O Interface section, Host/DMA Interface Programming Model for descriptions of these status bits) status bits are set or cleared from inside the DSP and read by the Host processor. The Host can read these status bits very quickly without regard to the clock rate used by the DSP, but the possibility exists that the state of the bit could be changing during the read operation. This is generally not a system problem, since the bit will be read correctly in the next pass of any Host polling routine.

However, if the Host asserts the  $\overline{\text{HEN}}$  for more than timing number 31a (T31a), with a minimum cycle time of timing number 32a (T32a), then the status is guaranteed to be stable.

A potential problem exists when reading status bits HF3 and HF2 as an encoded pair. If the DSP changes HF3 and HF2 from 00 to 11, there is a small probability that the Host could read the bits during the transition and receive 01 or 10 instead of 11. If the combination of HF3 and HF2 has significance, the Host could read the wrong combination.

Solution:

- a. Read the bits twice and check for consensus.
  - b. Assert  $\overline{\text{HEN}}$  access for T31a so that status bit transitions are stabilized.
4. **Overwriting the Host Vector**  
The Host programmer should change the Host Vector register only when the Host Command bit (HC) is clear. This change will guarantee that the DSP interrupt control logic will receive a stable vector.
  5. **Cancelling a Pending Host Command Exception**  
The Host processor may elect to clear the HC bit to cancel the Host Command Exception request at any time before it is recognized by the DSP. Because the Host does not know exactly when the exception will be recognized (due to exception processing synchronization and pipeline delays), the DSP may execute the Host exception after the HC bit is cleared. For these reasons, the HV bits must not be changed at the same time the HC bit is cleared.

### DSP Programmer Considerations

1. **Reading HF0 and HF1 as an Encoded Pair**  
DMA, HF1, HF0, and HCP, HTDE, and HRDF (refer to *DSP56000/DSP56001 User's Manual*, I/O Interface section, Host/DMA Interface Programming Model for descriptions of these status bits) status bits are set or cleared by the Host processor side of the interface. These bits are individually synchronized to the DSP clock.

A potential problem exists when reading status bits HF1 and HF2 as an encoded pair, i.e., the four combinations 00, 01, 10, and 11 each have significance. A very small probability exists that the DSP will read the status bits synchronized during transition. The solution to this potential problem is to read the bits twice for consensus.

DSP56001 Electrical Characteristics

AC Electrical Characteristics - Host I/O Timing

(Vcc = 5.0 Vdc ± 10%, Tj = -40 to +105° C, CL = 50 pf + 1 TTL Load at 20.5 MHz and 27 MHz)

(Vcc = 5.0 Vdc ± 5%, Tj = -40 to +105° C, CL = 50 pf + 1 TTL Load at 33 MHz)

(see Host Figures 1 through 6)

cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles

tHSDL = Host Synchronization Delay Time

Active low lines should be "pulled up" in a manner consistent with the AC and DC specifications

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
30	Host Synchronous Delay (see Note 1)	tcl	cyc+tcl	tcl	cyc+tcl	tcl	cyc+tcl	ns
31	HEN/HACK Assertion Width (see Note 2)							
	a.CVR, ICR, ISR Read (see Note 4)	cyc+60	—	cyc+46	—	cyc+37	—	ns
	b.Read	50	—	39	—	31	—	ns
	c.Write	25	—	19	—	16	—	ns
32	HEN/HACK Deassertion Width (see Note 2 and 5)	25	—	19	—	16	—	ns
32a	Minimum Cycle Time Between Two HEN Assertion for Consecutive CVR, ICR, and ISR Reads (see Note 2)	2*cyc+60	—	2*cyc+46	—	2*cyc+37	—	ns
33	Host Data Input Setup Time Before HEN/HACK Deassertion	5	—	4	—	4	—	ns
34	Host Data Input Hold Time After HEN/ HACK Deassertion	5	—	4	—	4	—	ns
35	HEN/HACK Assertion to Output Data Active from High Impedance	0	—	0	—	0	—	ns
36	HEN/HACK Assertion to Output Data Valid (periodically sampled, and not 100% tested)	—	50	—	39	—	31	ns
37	HEN/HACK Deassertion to Output Data High Impedance	—	35	—	27	—	22	ns
38	Output Data Hold Time After HEN/ HACK Deassertion	5	—	4	—	4	—	ns
39	HR/W Low Setup Time Before HEN Assertion	0	—	0	—	0	—	ns
40	HR/W Low Hold Time After HEN Deassertion	5	—	4	—	4	—	ns
41	HR/W High Setup Time to HEN Assertion	0	—	0	—	0	—	ns
42	HR/W High Hold Time After HEN/ HACK Deassertion	5	—	4	—	4	—	ns
43	HA0-HA2 Setup Time Before HEN Assertion	0	—	0	—	0	—	ns
44	HA0-HA2 Hold Time After HEN Deassertion	5	—	4	—	4	—	ns
45	DMA HACK Assertion to HREQ Deassertion (see Note 3)	5	60	4	46	4	49	ns

DSP56001 Electrical Characteristics

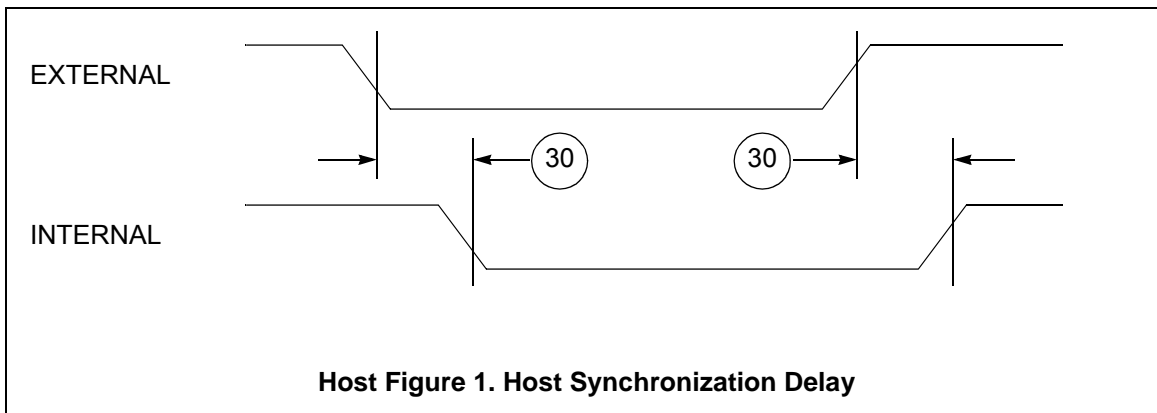
AC Electrical Characteristics - Host I/O Timing (Continued)

(Vcc = 5.0 Vdc ± 10%, Tj = -40 to +105° C, CL = 50 pf + 1 TTL Load at 20.5 MHz and 27 MHz  
 (Vcc = 5.0 Vdc ± 5%, Tj = -40 to +105° C, CL = 50 pf + 1 TTL Load at 33 MHz,  
 see Host Figures 1 through 6)  
 cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles  
 tHSDL = Host Synchronization Delay Time  
 Active low lines should be "pulled up" in a manner consistent with the AC and DC specifications

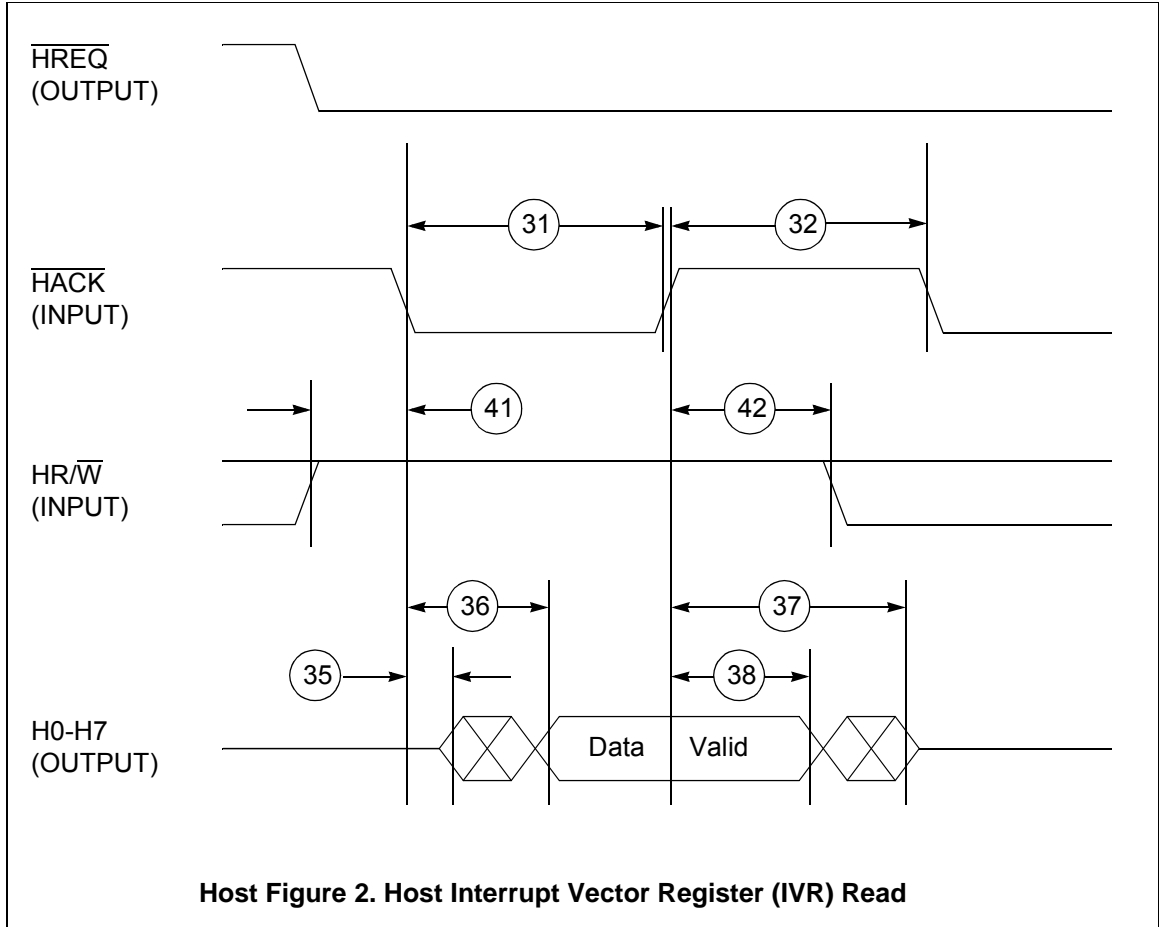
Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
46	DMA $\overline{\text{HACK}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion (see Note 3) for DMA RXL Read	tHSDL+cyc+tch+5	—	tHSDL+cyc+tch+4	—	tHSDL+cyc+tch+4	—	ns
	for DMA TXL Write	tHSDL+cyc+5	—	tHSDL+cyc+4	—	tHSDL+cyc+4	—	ns
	for All Other Cases	5	—	4	—	4	—	ns
47	Delay from $\overline{\text{HEN}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion for RXL Read (see Note 3)	tHSDL+cyc+tch+5	—	tHSDL+cyc+tch+4	—	tHSDL+cyc+tch+4	—	ns
48	Delay from $\overline{\text{HEN}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion for TXL Write (see Note 3)	tHSDL+cyc+5	—	tHSDL+cyc+4	—	tHSDL+cyc+4	—	ns
49	Delay from $\overline{\text{HEN}}$ Assertion to $\overline{\text{HREQ}}$ Deassertion for RXL Read, TXL Write (see Note 3)	5	75	4	70	4	65	ns

Notes:

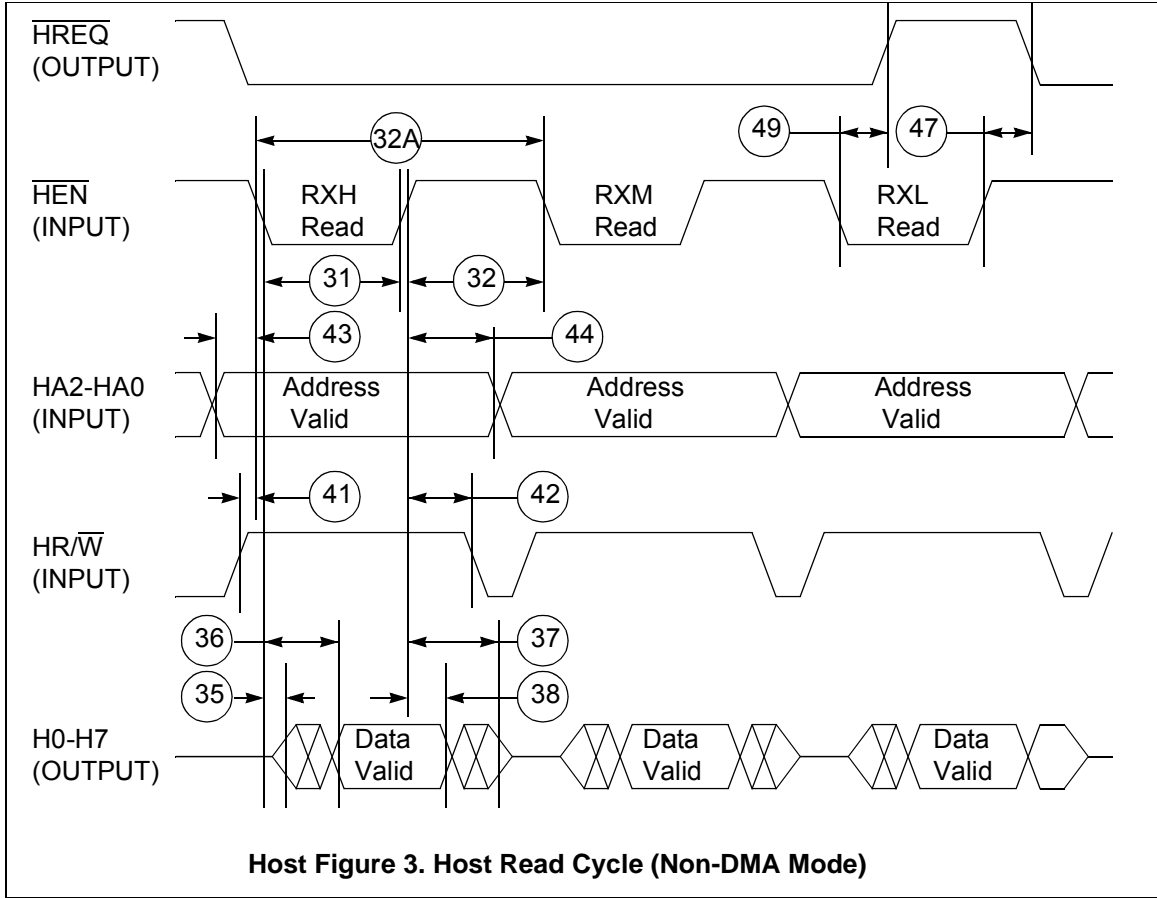
1. "Host synchronization delay (tHSDL)" is the time period required for the DSP56001 to sample any external asynchronous input signal, determine whether it is high or low, and synchronize it to the DSP56001 internal clock.
2. See **HOST PORT USAGE CONSIDERATIONS**.
3.  $\overline{\text{HREQ}}$  is pulled up by a 1kΩ resistor.
4. This timing must be adhered to only if two consecutive reads from one of these registers are executed.
5. It is recommended that timing #32 be 2cyc+tch+10 minimum for 20.5 MHz, 2cyc+tch+7 minimum for 27 MHz, and 2cyc+tch+6 minimum for 33 MHz if two consecutive writes to TXL are executed without polling TXDE or  $\overline{\text{HREQ}}$ .



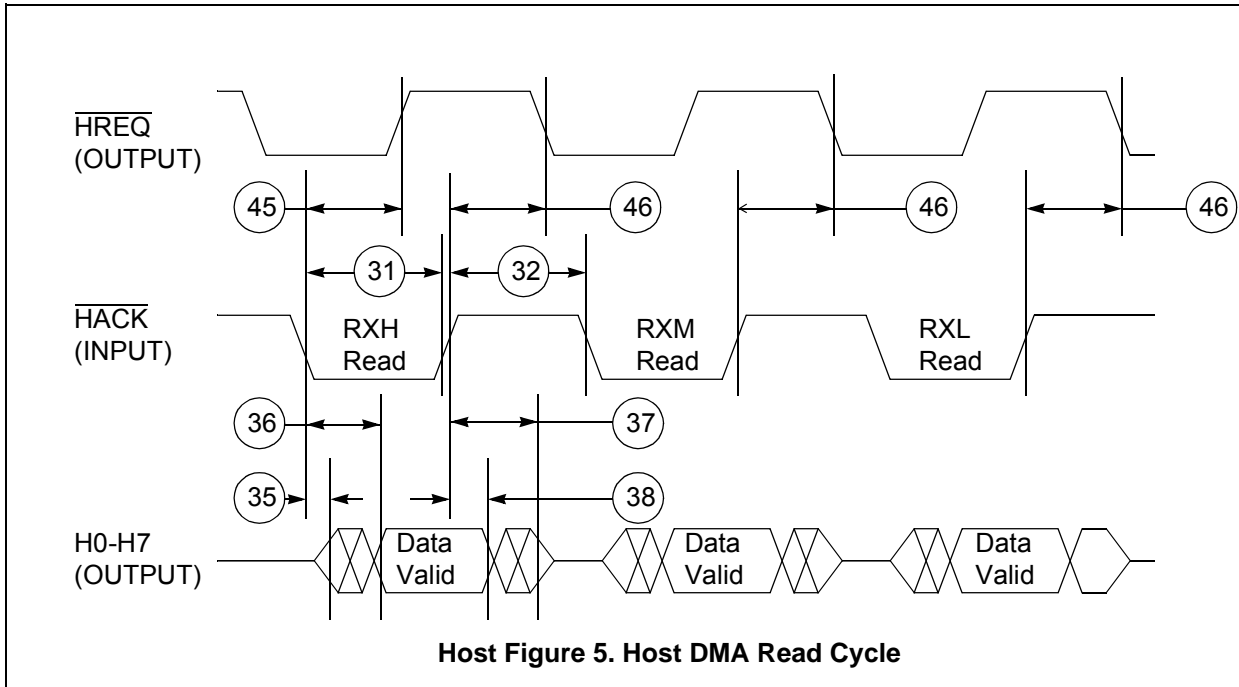
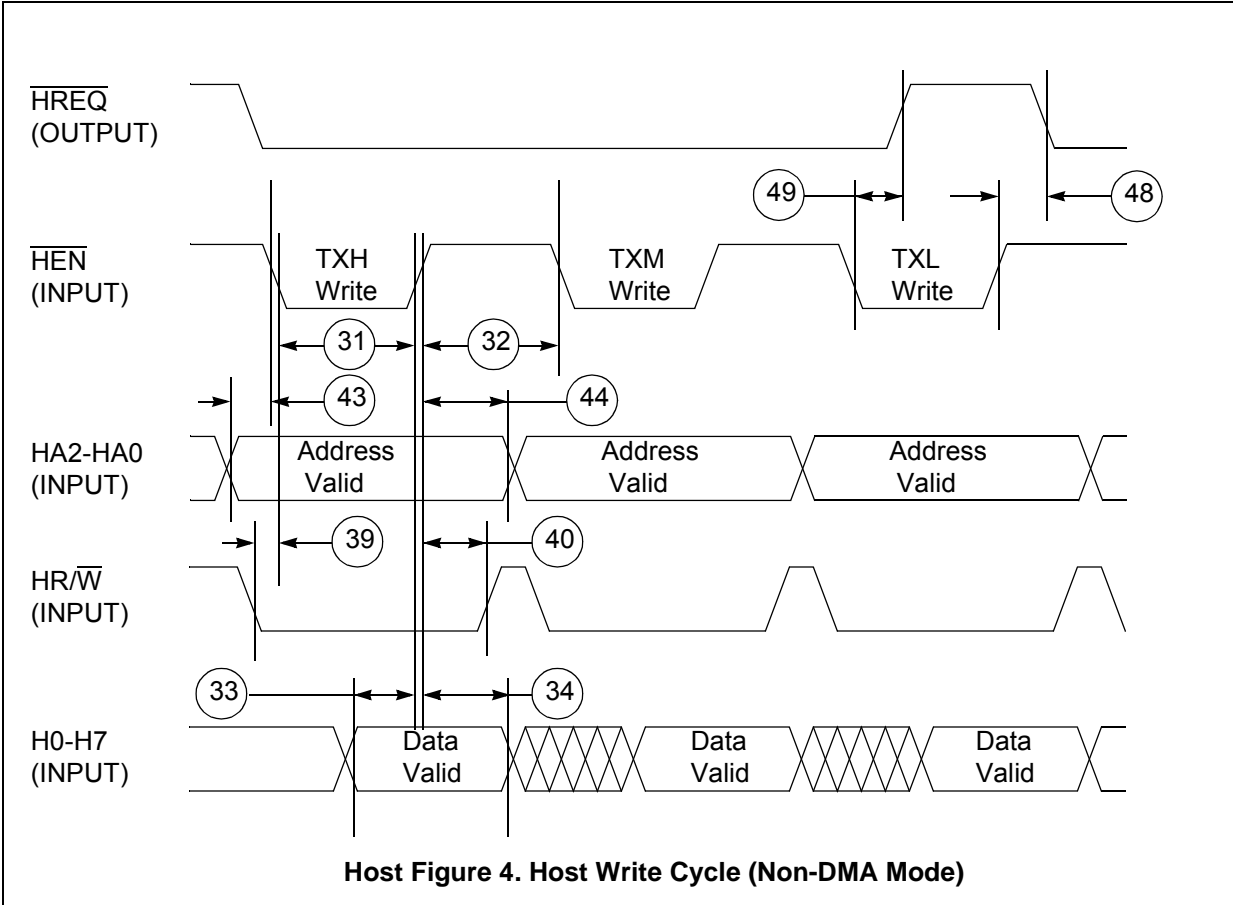
DSP56001 Electrical Characteristics



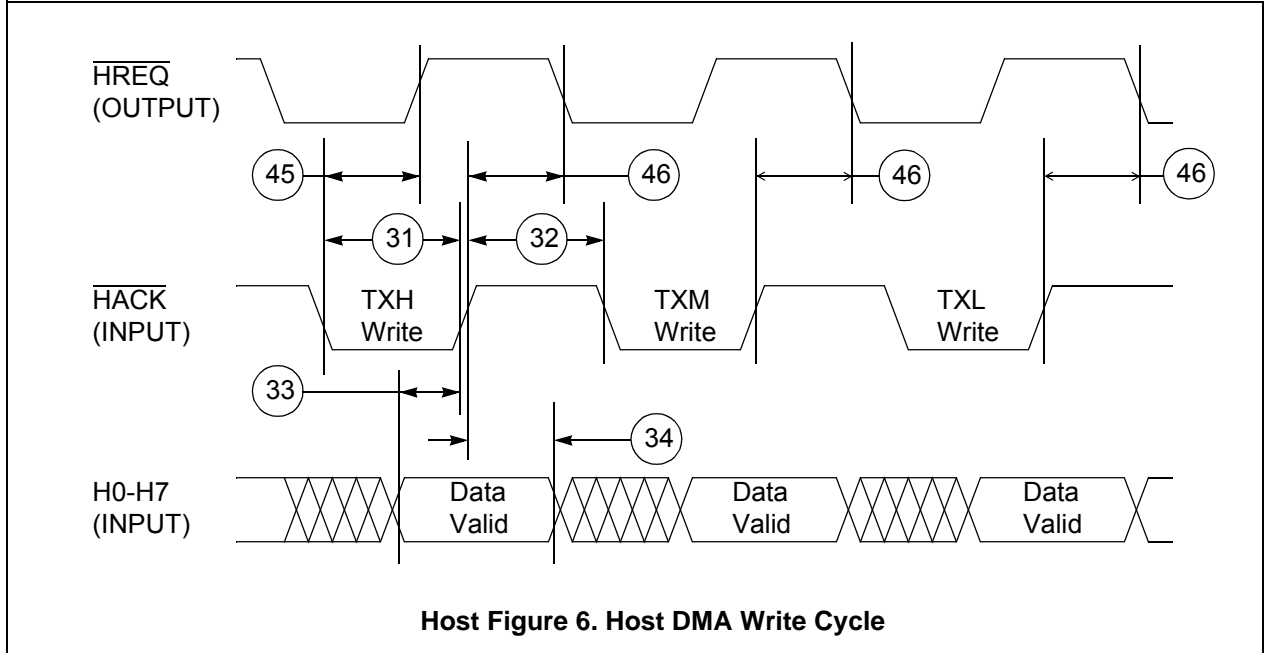
DSP56001 Electrical Characteristics



DSP56001 Electrical Characteristics



DSP56001 Electrical Characteristics



**DSP56001 Electrical Characteristics**

**AC Electrical Characteristics - SCI Timing**

(Vcc = 5.0 Vdc ± 10%, Tj = -40 to +105° C, CL = 50 pf + 1 TTL Load at 20.5 MHz and 27 MHz,

Vcc = 5.0 Vdc ± 5%, Tj = -40 to +105° C, CL = 50 pf + 1 TTL Load at 33 MHz,

see SCI Figures 1 and 2)

cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles

tSCC = Synchronous Clock Cycle Time (for internal clock tSCC is determined by the SCI clock control register and Iccyc.)

**SCI Synchronous Mode Timing**

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
55	Synchronous Clock Cycle — tSCC	8 <sub>*</sub> cyc	—	8 <sub>*</sub> cyc	—	8 <sub>*</sub> cyc	—	ns
56	Clock Low Period	4 <sub>*</sub> cyc-20	—	4 <sub>*</sub> cyc-15	—	4 <sub>*</sub> cyc-13	—	ns
57	Clock High Period	4 <sub>*</sub> cyc-20	—	4 <sub>*</sub> cyc-15	—	4 <sub>*</sub> cyc-13	—	ns
59	Output Data Setup to Clock Falling Edge (Internal Clock)	2 <sub>*</sub> cyc +tcl-50	—	2 <sub>*</sub> cyc +tcl-39	—	2 <sub>*</sub> cyc +tcl-31	—	ns
60	Output Data Hold After Clock Rising Edge (Internal Clock)	2 <sub>*</sub> cyc -tcl-15	—	2 <sub>*</sub> cyc -tcl-11	—	2 <sub>*</sub> cyc -tcl-9	—	ns
61	Input Data Setup Time Before Clock Rising Edge (Internal Clock)	2 <sub>*</sub> cyc +tcl+45	—	2 <sub>*</sub> cyc +tcl+35	—	2 <sub>*</sub> cyc +tcl+28	—	ns
62	Input Data Not Valid Before Clock Rising Edge (Internal Clock)	—	2 <sub>*</sub> cyc +tcl-10	—	2 <sub>*</sub> cyc +tcl-8	—	2 <sub>*</sub> cyc +tcl-6	ns
63	Clock Falling Edge to Output Data Valid (External Clock)	—	63	—	48	—	39	ns
64	Output Data Hold After Clock Rising Edge (External Clock)	cyc+12	—	cyc+9	—	cyc+8	—	ns
65	Input Data Setup Time Before Clock Rising Edge (External Clock)	30	—	23	—	19	—	ns
66	Input Data Hold Time After Clock Rising Edge (External Clock)	40	—	31	—	25	—	ns



**DSP56001 Electrical Characteristics**

**AC Electrical Characteristics - SCI Timing**

(Vcc = 5.0 Vdc ± 10%, Tj = -40 to +105° C, CL = 50 pf + 1 TTL Load at 20.5 MHz and 27 MHz,

Vcc = 5.0 Vdc ± 5%, Tj = -40 to +105° C, CL = 50 pf + 1 TTL Load at 33 MHz,

see SCI Figures 1 and 2)

cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles

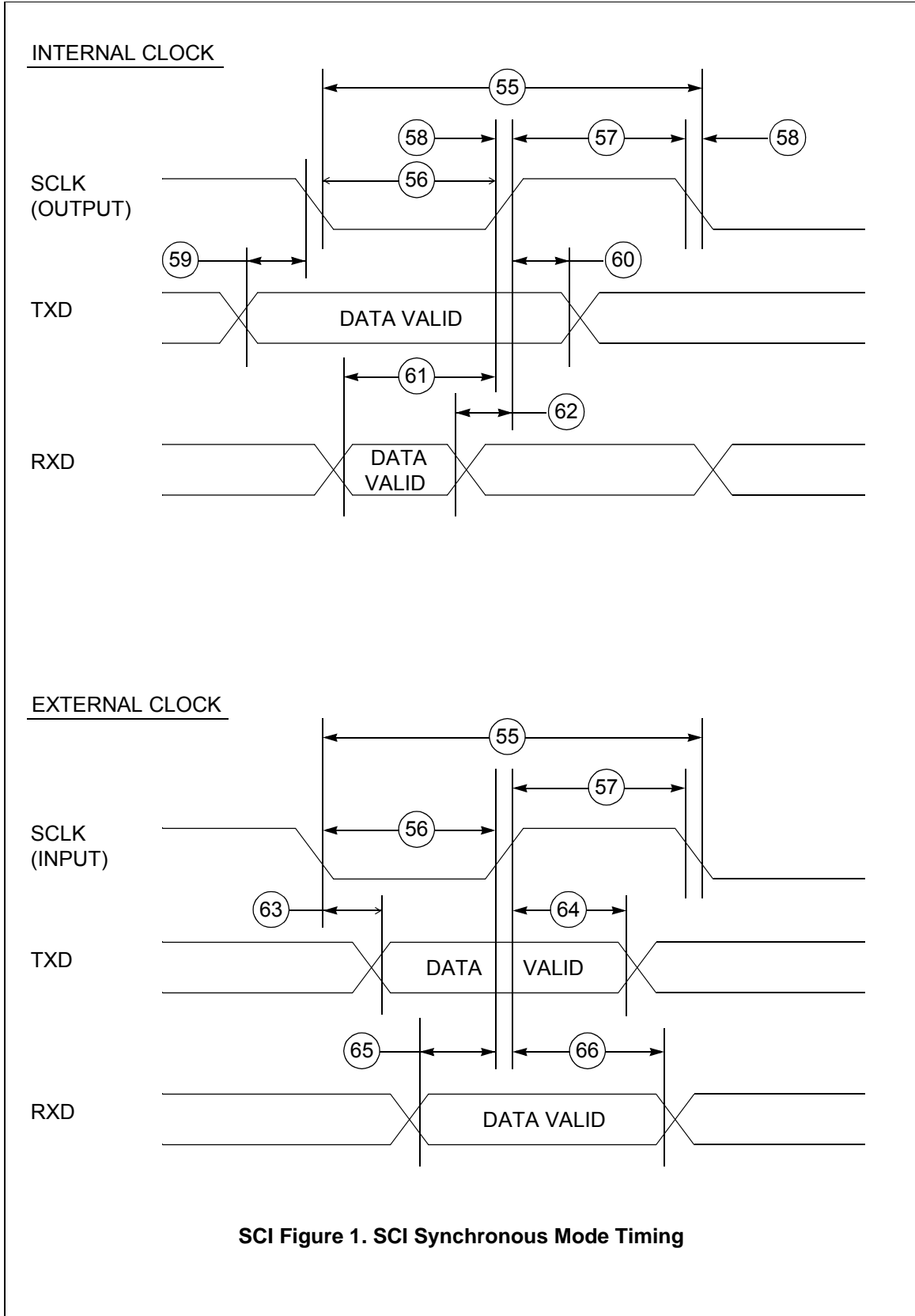
tACC = Asynchronous clock cycle time

tACC = Asynchronous Clock Cycle Time (for internal clock tACC is determined by the SCI clock control register and Icy)

**SCI Asynchronous Mode Timing - 1X Clock**

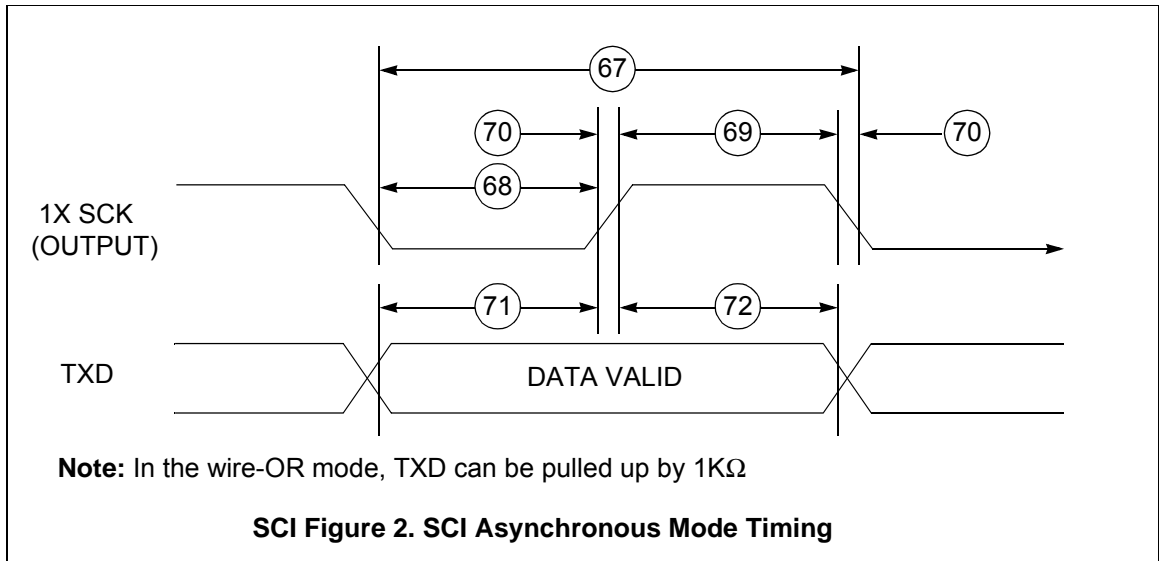
Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
67	Asynchronous Clock Cycle	64 <sub>*</sub> cyc	—	64 <sub>*</sub> cyc	—	64 <sub>*</sub> cyc	—	ns
68	Clock Low Period	32 <sub>*</sub> cyc-20	—	32 <sub>*</sub> cyc-15	—	32 <sub>*</sub> cyc-13	—	ns
69	Clock High Period	32 <sub>*</sub> cyc-20	—	32 <sub>*</sub> cyc-15	—	32 <sub>*</sub> cyc-13	—	ns
71	Output Data Setup to Clock Rising Edge (Internal Clock)	32 <sub>*</sub> cyc -100	—	32 <sub>*</sub> cyc -77	—	32 <sub>*</sub> cyc -61	—	ns
72	Output Data Hold After Clock Rising Edge (Internal Clock)	32 <sub>*</sub> cyc -100	—	32 <sub>*</sub> cyc -77	—	32 <sub>*</sub> cyc -61	—	ns

DSP56001 Electrical Characteristics



SCI Figure 1. SCI Synchronous Mode Timing

DSP56001 Electrical Characteristics



DSP56001 Electrical Characteristics

AC Electrical Characteristics - SSI Timing

(Vcc = 5.0 Vdc ± 10%, Tj = -40 to +105° C, CL = 50 pf + 1 TTL Load at 20.5 MHz and 27 MHz,

Vcc = 5.0 Vdc ± 5%, Tj = -40 to +105° C, CL = 50 pf + 1 TTL Load at 33 MHz,

see SSI Figures 1 and 2)

cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles

tSSICC = SSI clock cycle time

TXC (SCK Pin) = Transmit Clock

RXC (SC0 or SCK Pin) = Receive Clock

FST (SC2 Pin) = Transmit Frame Sync

FSR (SC1 or SC2 Pin) = Receive Frame Sync

i ck = Internal Clock

x ck = External Clock

g ck = Gated Clock

i ck a = Internal Clock, Asynchronous Mode (Asynchronous implies that TXC and RXC are two different clocks)

i ck s = Internal Clock, Synchronous Mode (Synchronous implies that TXC and RXC are the same clock)

bl = bit length

wl = word length

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
80	Clock Cycle (see Note 1)	4 <sub>x</sub> cyc	—	4 <sub>x</sub> cyc	—	4 <sub>x</sub> cyc	—	ns
81	Clock High Period	2 <sub>x</sub> cyc-20	—	2 <sub>x</sub> cyc-15	—	2 <sub>x</sub> cyc-13	—	ns
82	Clock High Period	2 <sub>x</sub> cyc-20	—	2 <sub>x</sub> cyc-15	—	2 <sub>x</sub> cyc-13	—	ns
84	RXC Rising Edge to FSR Out (bl) High	x ck	80	—	61	—	48	ns
		i ck a	50	—	38	—	31	ns
85	RXC Rising Edge to FSR Out (bl) Low	x ck	70	—	54	—	43	ns
		i ck a	40	—	31	—	25	ns
86	RXC Rising Edge to FSR Out (wl) High	x ck	70	—	54	—	43	ns
		i ck a	40	—	31	—	25	ns
87	RXC Rising Edge to FSR Out (wl) Low	x ck	70	—	54	—	43	ns
		i ck a	40	—	31	—	25	ns
88	Data In Setup Time Before RXC (SCK in Synchronous Mode) Falling Edge	x ck	15	—	12	—	10	ns
		i ck a	35	—	27	—	22	ns
		i ck s	25	—	19	—	16	ns
89	Data In Hold Time After RXC Falling Edge	x ck	35	—	27	—	22	ns
		i ck a	5	—	4	—	4	ns
90	FSR Input (bl) High Before RXC Falling Edge	x ck	15	—	12	—	10	ns
		i ck a	35	—	27	—	23	ns
91	FSR Input (wl) High Before RXC Falling Edge	x ck	20	—	15	—	13	ns
		i ck a	55	—	42	—	34	ns
92	FSR Input Hold Time After RXC Falling Edge	x ck	35	—	27	—	22	ns
		i ck a	5	—	4	—	4	ns

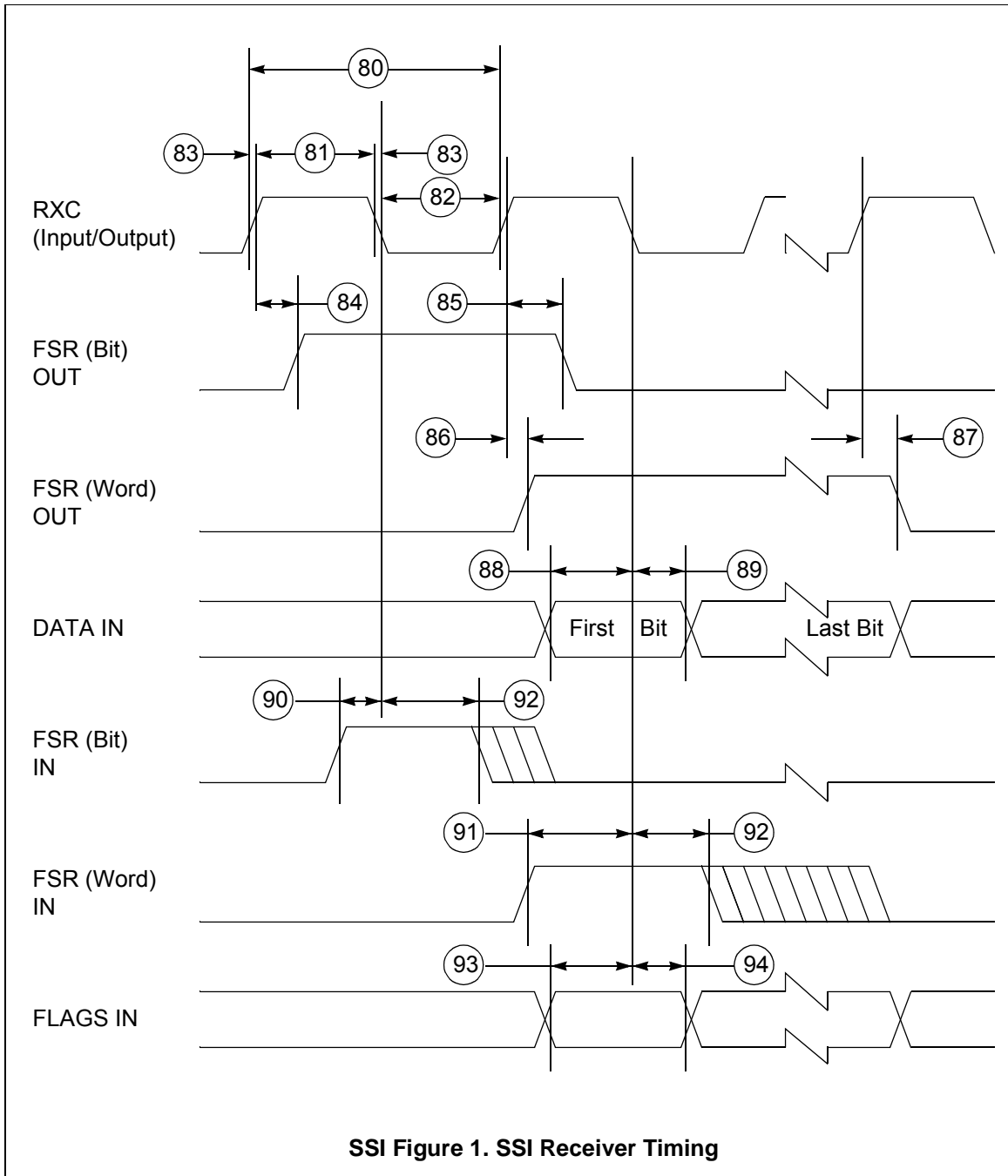
**DSP56001 Electrical Characteristics**  
**AC Electrical Characteristics - SSI Timing (Continued)**

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
93	Flags Input Setup Before RXC Falling Edge x ck i ck a	30 50	— —	23 39	— —	19 31	— —	ns nss
94	Flags Input Hold Time After RXC Falling Edge x ck i ck a	35 5	— —	27 4	— —	22 4	— —	ns ns
95	TXC Rising Edge to FST Out (bl) High x ck i ck a	— —	70 30	— —	54 23	— —	43 19	ns ns
96	TXC Rising Edge to FST Out (bl) Low x ck i ck a	— —	65 35	— —	50 27	— —	40 22	ns ns
97	TXC Rising Edge to FST Out (wl) High x ck i ck a	— —	65 35	— —	50 27	— —	40 22	ns ns
98	TXC Rising Edge to FST Out (wl) Low x ck i ck a	— —	65 35	— —	50 27	— —	40 22	ns ns
99	TXC Rising Edge to Data Out Enable from High Impedance x ck i ck a	— —	65 40	— —	50 31	— —	40 25	ns ns
100	TXC Rising Edge to Data Out Valid x ck i ck a	— —	65 40	— —	50 31	— —	40 25	ns ns
101	TXC Rising Edge to Data Out High Impedance (periodically sampled, and not 100% tested) x ck i ck a	— —	70 40	— —	54 31	— —	43 25	ns ns
101a	TXC Falling Edge to Data Out High Impedance for Gated Clock Mode Only g ck	cyc+tch	—	cyc+tch	—	cyc+tch	—	ns
102	FST Input (bl) Setup Time Before TXC Falling Edge x ck i ck a	15 35	— —	12 27	— —	10 23	— —	ns ns
103	FST Input (wl) to Data Out Enable from High Impedance	—	60	—	46	—	37	ns
104	FST Input (wl) Setup Time Before TXC Falling Edge x ck i ck a	20 55	— —	15 42	— —	13 34	— —	ns ns
105	FST Input Hold Time After TXC Falling Edge x ck i ck a	35 5	— —	27 4	— —	22 4	— —	ns ns
106	Flag Output Valid After TXC Rising Edge x ck i ck a	— —	70 40	— —	54 31	— —	43 25	ns ns

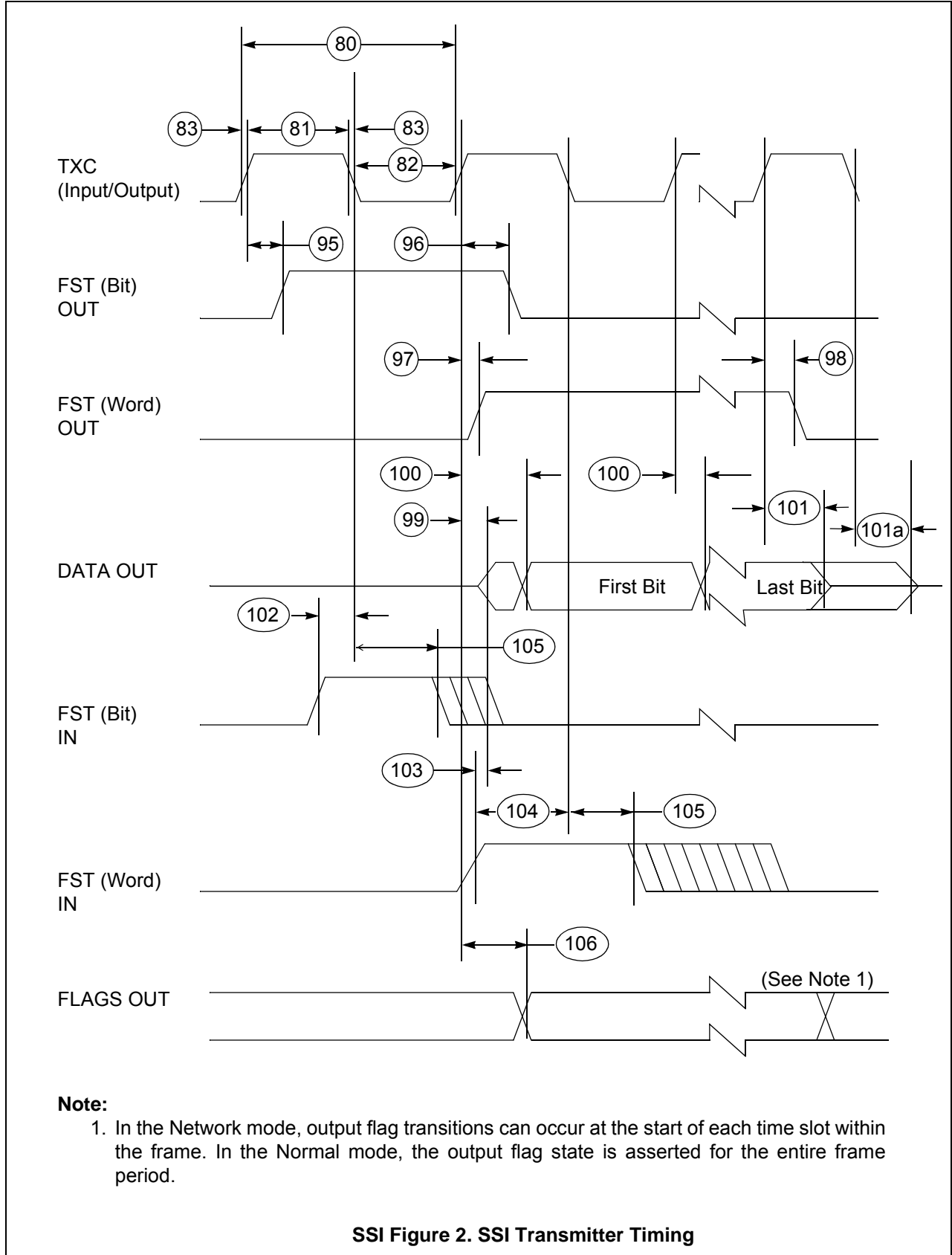
**Note:**

1. For internal clock, External Clock Cycle is defined by l<sub>cyc</sub> and SSI control register.

DSP56001 Electrical Characteristics



DSP56001 Electrical Characteristics



**Note:**

1. In the Network mode, output flag transitions can occur at the start of each time slot within the frame. In the Normal mode, the output flag state is asserted for the entire frame period.

SSI Figure 2. SSI Transmitter Timing

DSP56001 Electrical Characteristics

AC Electrical Characteristics —

Capacitance Derating — External Bus Asynchronous Timing

Vcc = 5.0 Vdc ± 10%, Tj = -40 to +105° C, CL = 50 pf + 1 TTL Load at 20.5 MHz and 27 MHz,

Vcc = 5.0 Vdc ± 5%, Tj = -40 to +105° C, CL = 50 pf + 1 TTL Load at 33 MHz, see Bus Figures 1 and 2

cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles

WS = Number of Wait States, Determined by BCR Register (WS = 0 to 15)

The DSP56001 External Bus Timing Specifications are designed and tested at the maximum capacitive load of 50 pf, including stray capacitance. Typically, the drive capability of the External Bus pins (A0-A15, D0-D23,  $\overline{PS}$ ,  $\overline{DS}$ ,  $\overline{RD}$ ,  $\overline{WR}$ ,  $X/\overline{Y}$ ) derates linearly at 1 ns per 12 pf of additional capacitance from 50 pf to 250 pf of loading. Port B and C pins derate linearly at 1 ns per 5 pf of additional capacitance from 50 pf to 250 pf of loading.

Active low inputs should be “pulled up” in a manner consistent with the AC and DC specifications.

To conserve power, when an internal memory access follows an external memory access, the  $\overline{RD}$  and  $\overline{WR}$  strobes remain deasserted and A0-A15 and  $X/\overline{Y}$  do not change from their previous state. Both  $\overline{PS}$  and  $\overline{DS}$  will be deasserted (they do not change between two external accesses to the same memory space) indicating that no external memory access is occurring. If BR has been asserted, then the bus signals will be three-stated according to the timing information in this data sheet.

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit	
		Min	Max	Min	Max	Min	Max		
115	Delay from $\overline{BR}$ Assertion to $\overline{BG}$ Assertion (see Note 1)	$2 \times \text{cyc} + \text{tch}$	$4 \times \text{cyc} + \text{tch} + 20$	$2 \times \text{cyc} + \text{tch}$	$4 \times \text{cyc} + \text{tch} + 15$	$2 \times \text{cyc} + \text{tch}$	$4 \times \text{cyc} + \text{tch} + 13$	ns	
		cyc+tch	$4 \times \text{cyc} + \text{tch} + \text{cyc} \times \text{WS} + 20$	cyc+tch	$4 \times \text{cyc} + \text{tch} + \text{cyc} \times \text{WS} + 15$	cyc+tch	$4 \times \text{cyc} + \text{tch} + \text{cyc} \times \text{WS} + 13$	ns	
		cyc+tch	$6 \times \text{cyc} + \text{tch} + 2 \times \text{cyc} \times \text{WS} + 20$	cyc+tch	$6 \times \text{cyc} + \text{tch} + 2 \times \text{cyc} \times \text{WS} + 15$	cyc+tch	$6 \times \text{cyc} + \text{tch} + 2 \times \text{cyc} \times \text{WS} + 13$	ns	
		Infinity	—	Infinity	—	Infinity	—	ns	
		tch+4	cyc+tch+30	tch+3	cyc+tch+23	tch+3	cyc+tch+19	ns	
116	Flags Input Hold Time After RXC Falling Edge Deassertion	$2 \times \text{cyc}$	$4 \times \text{cyc} + 20$	$2 \times \text{cyc}$	$4 \times \text{cyc} + 15$	$2 \times \text{cyc}$	$4 \times \text{cyc} + 13$	ns	
117	$\overline{BG}$ Deassertion Duration	$2 \times \text{cyc} - 10$	—	$2 \times \text{cyc} - 8$	—	$2 \times \text{cyc} - 6$	—	ns	
118	Delay from Address, Data, and Control Bus High Impedance to $\overline{BG}$ Assertion	0	—	0	—	0	—	ns	
119	Delay from $\overline{BG}$ Deassertion to Address, Data, and Control Bus Enabled	—	tch-10	—	tch-8	—	tch-6	ns	
120	Address Valid to $\overline{WR}$ Assertion	WS=0	tcl-9	tcl+5	tcl-7	tcl+5	tcl-5.5	tcl+5	ns
		WS>0	cyc-9	cyc+5	cyc-7	cyc+5	cyc-5.5	cyc+5	ns
121	$\overline{WR}$ Assertion Width	WS=0	cyc-9	—	cyc-7	—	cyc-5.0	—	ns
		WS>0	WS*cyc+tcl-9	—	WS*cyc+tcl-7	—	WS*cyc+tcl-5.0	—	ns
122	$\overline{WR}$ Deassertion to Address Not Valid	tch-12	—	tch-9	—	tch-7.5	—	ns	
123	$\overline{WR}$ Assertion to Data Out Valid	WS=0	tch-9	tch+10	tch-7	tch+8	tch-5.5	tch+6.5	ns
		WS>0	0	10	0	8	0	6.5	ns
124	Data Out Hold Time from $\overline{WR}$ Deassertion (The maximum specification is periodically sampled, and not 100% tested.)	tch-9	tch+7	tch-7	tch+6	tch-5.5	tch+4.5	ns	
125	Data Out Setup Time to $\overline{WR}$ Deassertion (see Note 6)	WS=0	tcl-5	—	tcl-5	—	tcl-5	—	ns
		WS>0	WS*cyc+tcl-5	—	WS*cyc+tcl-5	—	WS*cyc+tcl-5	—	ns
126	$\overline{RD}$ Deassertion to Address Not Valid	tch-9	—	tch-7	—	tch-5.5	—	ns	



DSP56001 Electrical Characteristics

AC Electrical Characteristics - External Bus Asynchronous Timing  
(Continued)

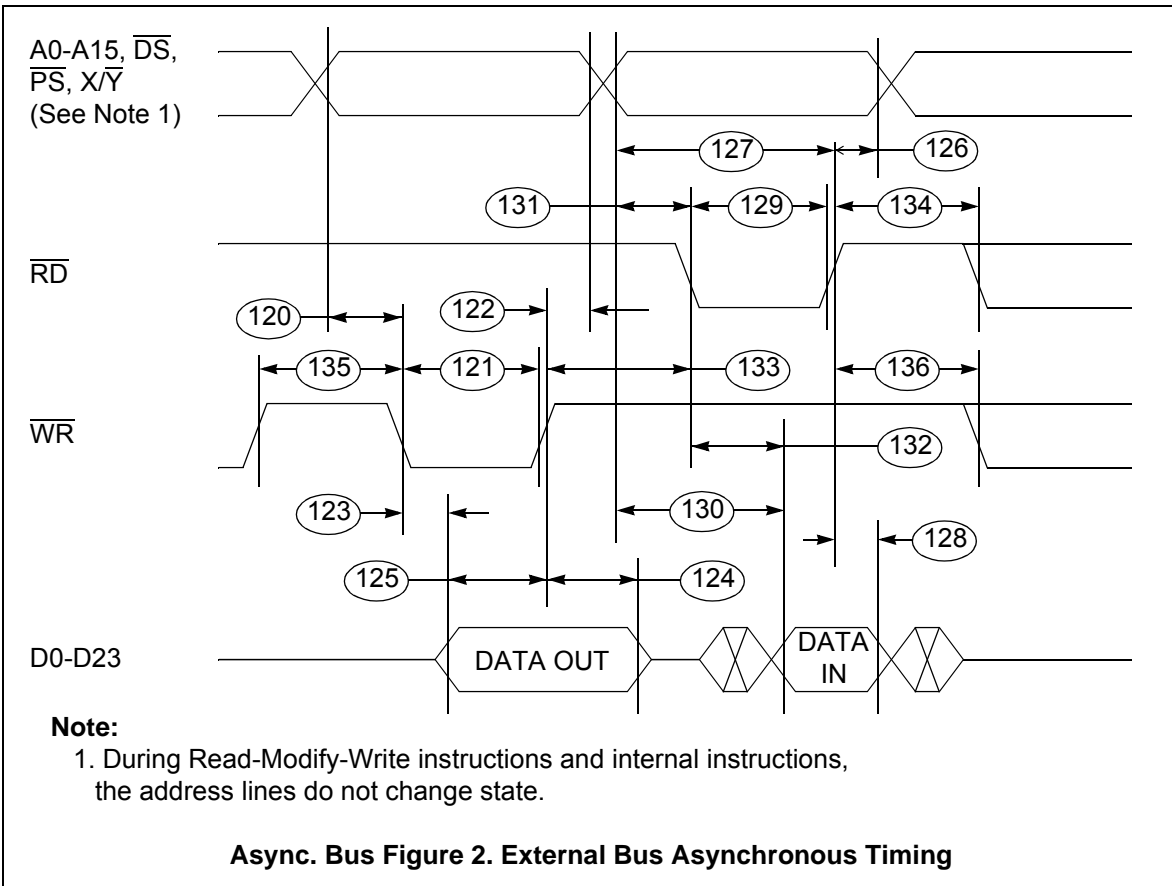
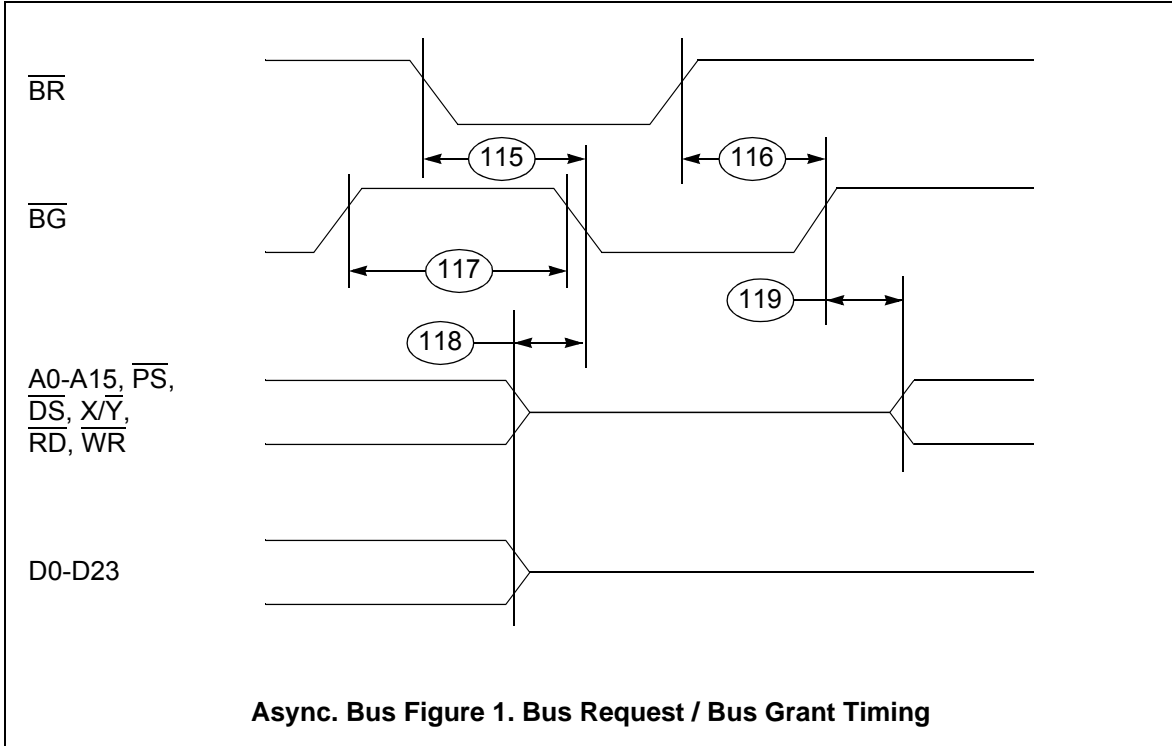
Num	Characteristics		20.5 MHz		27 MHz		33 MHz		Unit
			Min	Max	Min	Max	Min	Max	
127	Address Valid to $\overline{\text{RD}}$ deassertion	WS = 0 WS > 0	cyc+tcl-8 ((WS+1) <sub>*</sub> cyc)+tcl-8	— —	cyc+tcl-6 ((WS+1) <sub>*</sub> cyc)+tcl-6	— —	cyc+tcl-6 ((WS+1) <sub>*</sub> cyc)+tcl-6	— —	ns ns
128	Input Data Hold Time to $\overline{\text{RD}}$ Deassertion		0	—	0	—	0	—	ns
129	$\overline{\text{RD}}$ Assertion Width	WS = 0 WS > 0	cyc-9 ((WS+1) <sub>*</sub> cyc)-9	— —	cyc-7 ((WS+1) <sub>*</sub> cyc)-7	— —	cyc-5.5 ((WS+1) <sub>*</sub> cyc)-5.5	— —	ns ns
130	Address Valid to Input Data Valid	WS = 0 WS > 0	— —	cyc+tcl-18 ((WS+1) <sub>*</sub> cyc)+tcl-18	— —	cyc+tcl-14 ((WS+1) <sub>*</sub> cyc)+tcl-14	— —	cyc+tcl-11 ((WS+1) <sub>*</sub> cyc)+tcl-11	ns ns
131	Address Valid to $\overline{\text{RD}}$ Assertion		tcl-9	tcl+5	tcl-7	tcl+5	tcl-5.5	tcl+5	ns
132	$\overline{\text{RD}}$ Assertion to Input Data Valid	WS=0 WS>0	— —	cyc-14 ((WS+1) <sub>*</sub> cyc)-14	— —	cyc-11 ((WS+1) <sub>*</sub> cyc)-11	— —	cyc-9 ((WS+1) <sub>*</sub> cyc)-9	ns ns
133	$\overline{\text{WR}}$ Deassertion to $\overline{\text{RD}}$ Assertion		cyc-15	—	cyc-12	—	cyc-10	—	ns
134	$\overline{\text{RD}}$ Deassertion to $\overline{\text{RD}}$ Assertion		cyc-10	—	cyc-8	—	cyc-6.5	—	ns
135	$\overline{\text{WR}}$ Deassertion to $\overline{\text{WR}}$ Assertion	WS=0 WS>0	cyc-15 cyc+tch-15	— —	cyc-12 cyc+tch-12	— —	cyc-10 cyc+tch-10	— —	ns ns
136	$\overline{\text{RD}}$ Deassertion to $\overline{\text{WR}}$ Assertion	WS=0 WS>0	cyc-10 cyc+tch-10	— —	cyc-8 cyc+tch-8	— —	cyc-6.5 cyc+tch-6.5	— —	ns ns

Notes:

1. With no external access from the DSP.
2. During external read or write access.
3. During external read-modify-write access.
4. During the STOP mode the external bus will not be released and  $\overline{\text{BG}}$  will not go low. However, if the bus is released ( $\overline{\text{BG}} = 0$ ) and the STOP instruction is executed while  $\overline{\text{BG}} = 0$  then the bus will remain released while the DSP is in the stop state and  $\overline{\text{BG}}$  will remain low.
5. During the WAIT mode the  $\overline{\text{BR}}/\overline{\text{BG}}$  circuits remain active.
6. Typical values at 5V are:
 

at 20.5 MHz and WS=0,	Min =	tcl-4
at 20.5 MHz and WS>0,	Min =	WS <sub>*</sub> cyc+tcl-4
at 27 MHz and WS=0,	Min =	tcl-3
at 27 MHz and WS>0,	Min =	WS <sub>*</sub> cyc+tcl-3
at 33 MHz and WS=0,	Min =	tcl-2.5
at 33 MHz and WS>0,	Min =	WS <sub>*</sub> cyc+tcl-2.5

DSP56001 Electrical Characteristics



DSP56001 Electrical Characteristics

AC Electrical Characteristics - External Bus Synchronous Timing

V<sub>cc</sub> = 5.0 Vdc ± 10%; T<sub>J</sub> = -40 to 105° C at 20.5 MHz 27 MHz

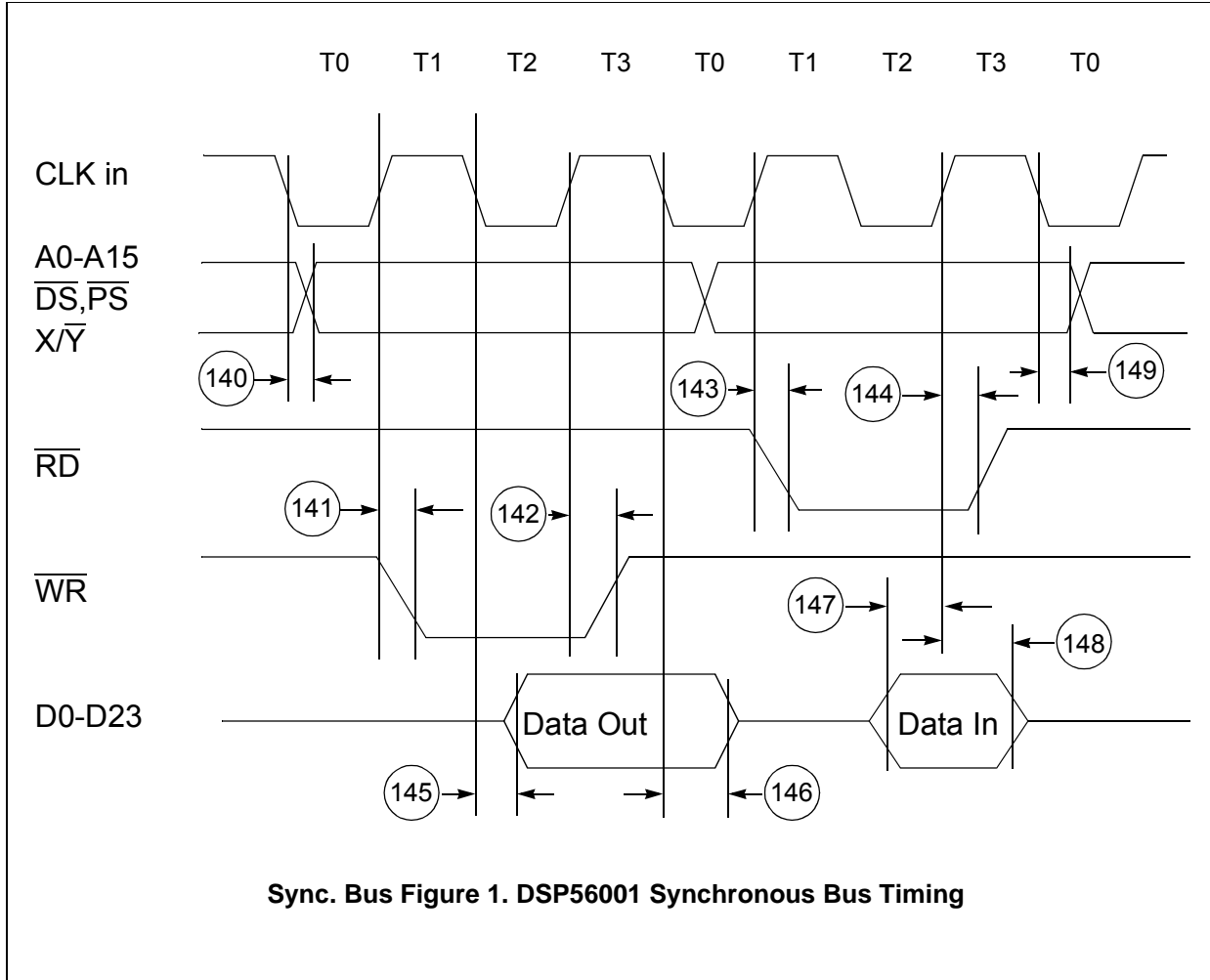
V<sub>cc</sub> = 5.0 Vdc ± 5%; T<sub>J</sub> = -40 to 105° C at 33 MHz

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
140	Clk Low Transition To Address Valid	—	24	—	19	—	19	ns
141	Clk High Transition To WR Assertion (see Note 2)	WS = 0	19	0	15	0	17	ns
		WS > 0	tch+19	0	tch+15	0	tch+17	ns
142	Clk High Transition To $\overline{WR}$ Deassertion	5	21	5	16	5	13	ns
143	Clk High Transition To $\overline{RD}$ Assertion	0	19	0	15	0	16	ns
144	Clk High Transition To $\overline{RD}$ Deassertion	5	17	5	13	4.5	10.5	ns
145	Clk Low Transition To Data-Out Valid	—	25	—	19	—	19	ns
146	Clk Low Transition To Data-Out Invalid (see Note 3)	5	—	4	—	3.5	—	ns
147	Data-In Valid To Clk High Transition (Setup)	0	—	0	—	0	—	ns
148	Clk High Transition To Data-In Invalid (Hold)	12	—	12	—	13	—	ns ns
149	Clk Low To Address Invalid (see Note 3)	3	—	3	—	3	—	ns

Notes:

1. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition.
2. WS are wait state values specified in the BCR.
3. Clk low to data-out invalid (spec. 146) and Clk low to address invalid (spec. 149) indicate the time after which data/address are no longer guaranteed to be valid.

DSP56001 Electrical Characteristics



**Note:** During Read-Modify-Write Instructions, the address lines do not change states.

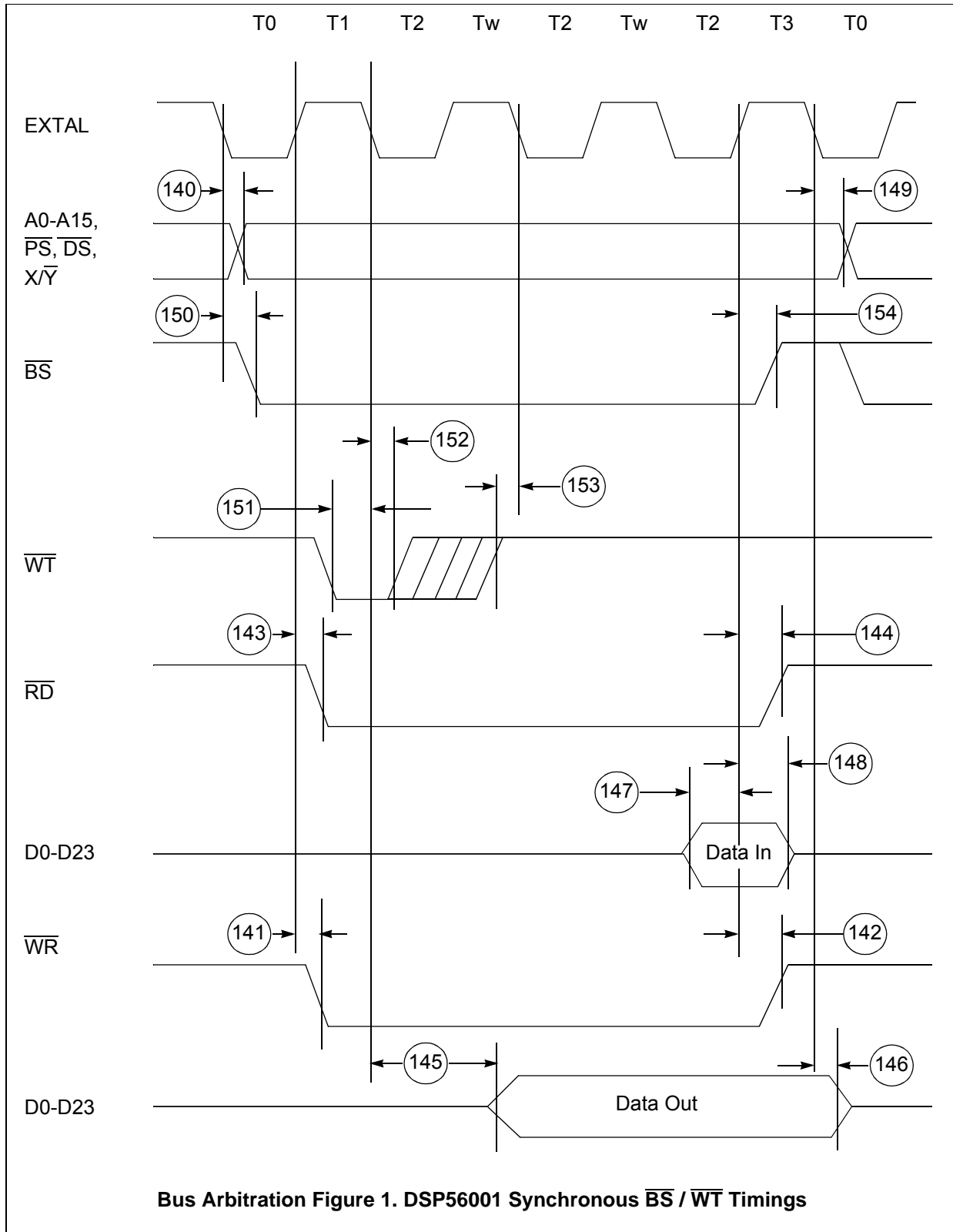
DSP56001 Electrical Characteristics  
AC Electrical Characteristics - Bus Strobe / Wait Timing

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit	
		Min	Max	Min	Max	Min	Max		
150	Clk Low Transition To $\overline{BS}$ Assertion	4	24	3	19	2.5	19	ns	
151	$\overline{WT}$ Assertion To Clk Low Transition (setup time)	4	—	3	—	2.5	—	ns ns	
152	Clk Low Transition To $\overline{WT}$ Deassertion For Minimum Timing	14	cyc-8	11	cyc-6	12	cyc-5	ns	
153	$\overline{WT}$ Deassertion To Clk Low Transition For Maximum Timing (2 wait states)	8	—	6	—	5	—	ns	
154	Clk High Transition To $\overline{BS}$ Deassertion	5	26	4	20	3.5	19	ns	
155	$\overline{BS}$ Assertion To Address Valid	-2	10	-2	8	-2	6.5	ns	
156	$\overline{BS}$ Assertion To $\overline{WT}$ Assertion (see Note 2)	0	cyc-15	0	cyc-11	0	cyc-10	ns	
157	$\overline{BS}$ Assertion To $\overline{WT}$ Deassertion (See Note 2 and Note 4)	$WS \leq 2$ $WS \geq 2$	cyc (WS-1) *cyc	$2 * cyc - 15$ $WS * cyc - 15$	cyc (WS-1) *cyc	$2 * cyc - 11$ $WS * cyc - 11$	cyc+4 (WS-1) *cyc+4	$2 * cyc - 10$ $WS * cyc - 10$	ns ns
158	$\overline{WT}$ Deassertion To $\overline{BS}$ Deassertion	cyc+tcl	$2 * cyc + tcl + 23$	cyc+tcl	$2 * cyc + tcl + 17$	cyc+tcl	$2 * cyc + tcl + 15$	ns	
159	Minimum $\overline{BS}$ Deassertion Width For Consecutive External Accesses	tch-7	—	tch-6	—	tch-4.5	—	ns	
160	$\overline{BS}$ Deassertion To Address Invalid (see Note 3)	tch-10	—	tch-8	—	tch-6.5	—	ns	
161	Data-In Valid to $\overline{RD}$ Deassertion (Set Up)	16	—	12	—	10	—	ns	

Note:

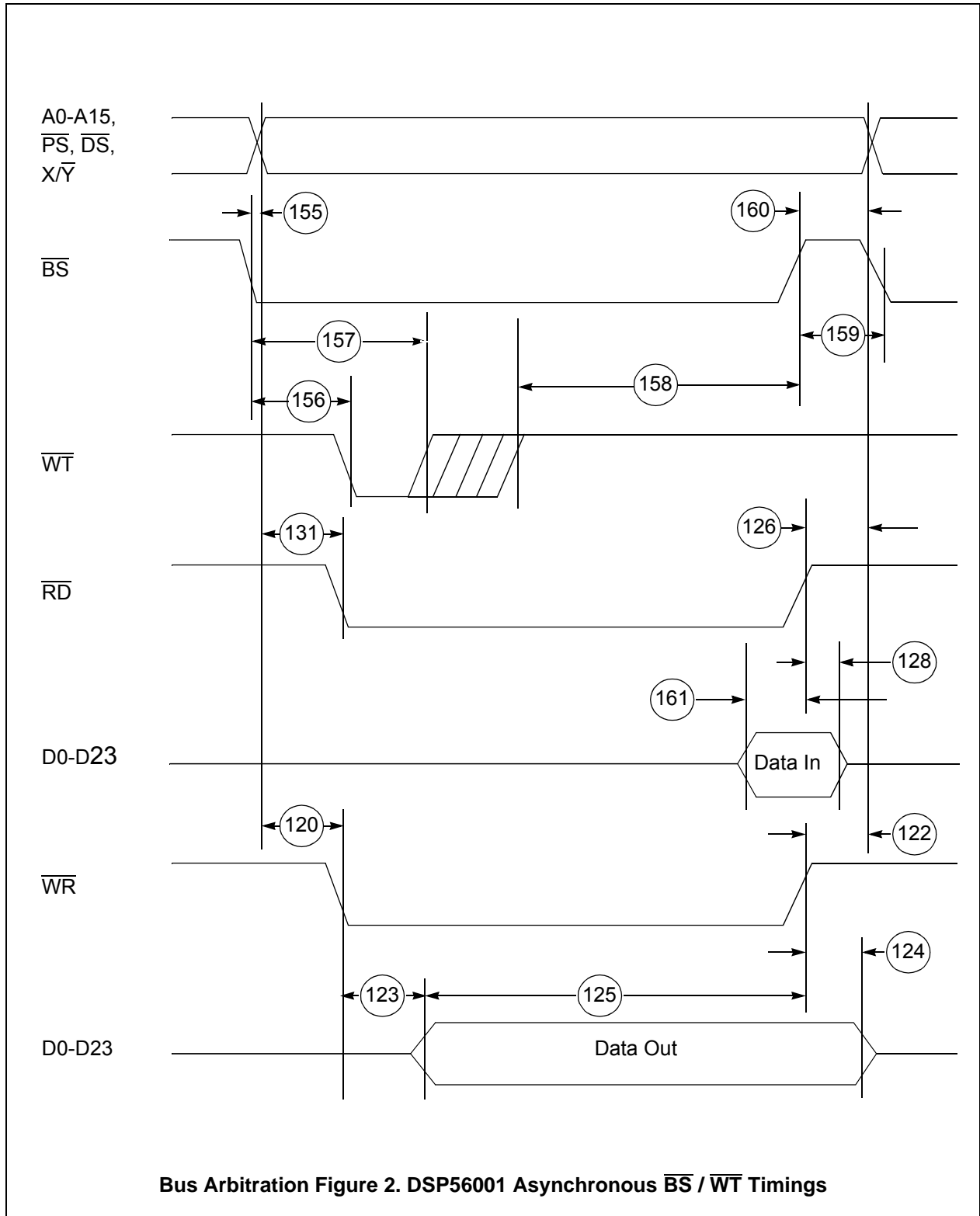
- AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition.
- If wait states are also inserted using the BCR and if the number of wait states is greater than 2, then specification numbers 156 and 157 can be increased accordingly.
- $\overline{BS}$  deassertion to address invalid indicates the time after which the address are no longer guaranteed to be valid.
- The minimum number of wait states when using  $\overline{BS}/\overline{WT}$  is two (2).
- For read-modify-write instructions, the address lines will not change states between the read and the write cycle. However,  $\overline{BS}$  will deassert before asserting again for the write cycle. If wait states are desired for each of the read and write cycle, the  $\overline{WT}$  pin must be asserted once for each cycle.

DSP56001 Electrical Characteristics



**Note:** During Read-Modify-Write Instructions, the address lines do not change state. However,  $\overline{BS}$  will deassert before asserting again for the write cycle.

DSP56001 Electrical Characteristics



**Note:** During Read-Modify-Write Instructions, the address lines will not change states. However,  $\overline{BS}$  will deassert before asserting again for the write cycle.

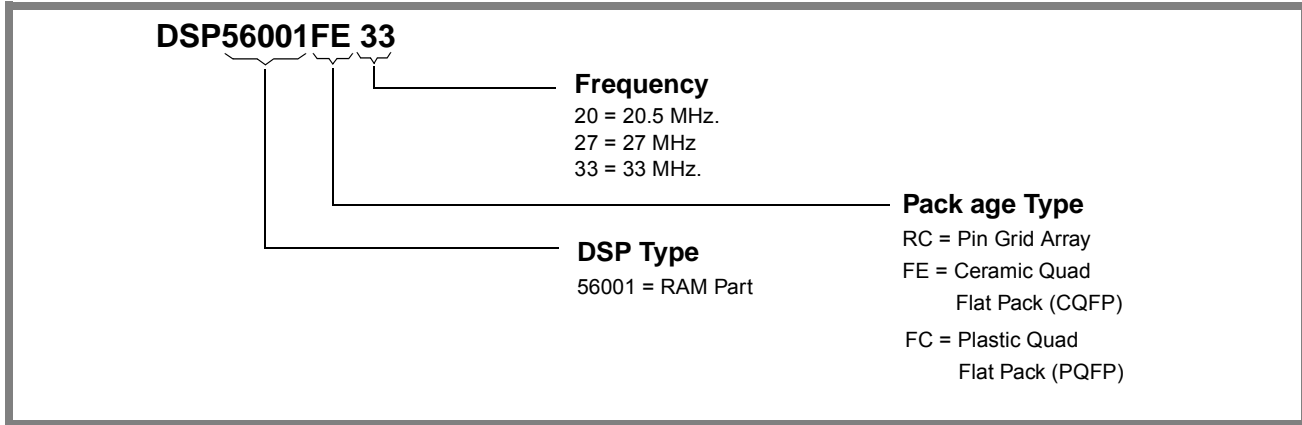




# Freescale Semiconductor, Inc.

## APPENDIX A

### ORDERING INFORMATION



### DSP56001 SOCKET INFORMATION

#### PGA

Supplier	Telephone	Socket Type	Part Number	Comment
Advanced Interconnections	(401) 823-5200	Standard 88 Pin	4CS088-01TG <sup>2</sup>	Includes Cutout in Center
AMP	(717) 564-0100	Standard 88 Pin	1-916223-3 1-55283-9	Low Insertion Force ZIF Production
		Standard 128 Pin	1-55383-4	ZIF Burn-In and Test
Robinson Nugent	(812) 945-0211	Custom Pinout	PGA-088CM3P-S-TG <sup>3</sup> PGA-088CHP3-SL-TG <sup>3</sup>	High Temp, Longer Leads
Samtec	(812) 944-6733	Standard 120 Pin Custom 88 Pin	MVAS-120-ZSTT-13 <sup>1</sup> CPAS-88-ZSTT-13BF <sup>1</sup>	Includes Cutout in Center No Cutout

**NOTES:**

- Please specify wirewrap and plating options. The part numbers shown specify low profile solder tail pins having a tin contact and tin shell.
- Please specify wirewrap and plating options. The part number shown specifies gold contact and tin shell.
- Cutout in the center, unused holes are plugged, solder tail.

#### CQFP

Supplier	Telephone	Socket Type	Part Number	Comment
AMP	(717)564-0100	—	822054-2 <sup>1</sup>	Converts CQFP to fit AMP's 132 position PQFP "Micro-Pitch Socket".

**NOTES:**

- This part is not a socket. It is a converter that allows a CQFP part to be used in the PQFP socket described below.

#### PQFP

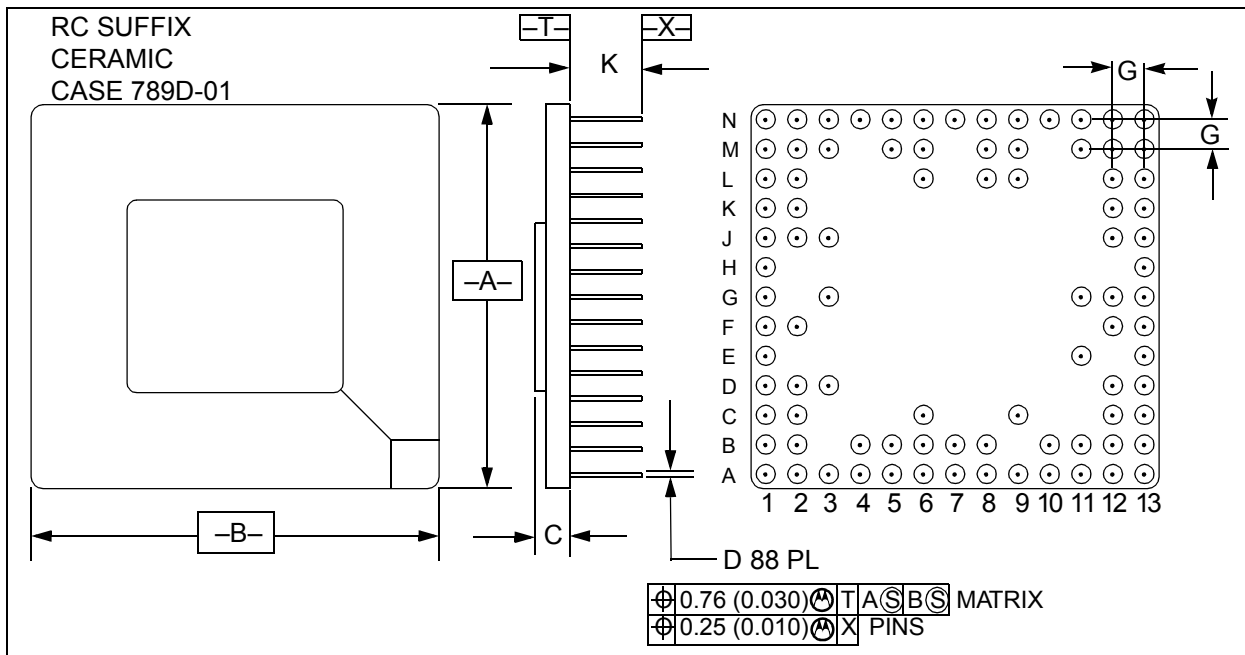
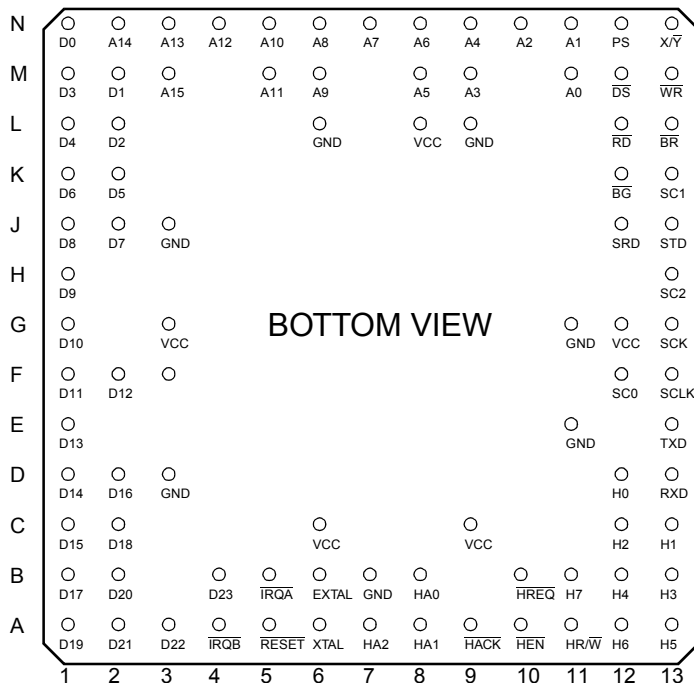
Supplier	Telephone	Socket Type	Part Number	Comment
AMP	(717)564-0100	132 Pin	821949-5 <sup>1</sup> 821942-1 <sup>1</sup>	Housing Sub-Assembly and Cover for 132 position PQFP "Micro-Pitch Socket".

**NOTES:**

- One housing sub-assembly and one cover are required for each socket.

# Freescale Semiconductor, Inc.

## PIN ASSIGNMENT



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	34.04	35.05	1.340	1.380
B	34.04	35.05	1.340	1.380
C	2.16	3.04	0.085	0.120
D	0.44	0.55	0.017	0.022
G	2.54 BSC		0.100 BSC	
K	4.20	5.08	0.165	0.200

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M. 1982.
- CONTROLLING DIMENSION: INCH.

Mechanical Specification Figure A-1. Pin Grid Array Mechanical Specification

## Mechanical Specification Table A-1. CQFP and PQFP Pin Out

PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION
17	NO CONNECT	116	NO CONNECT	83	NO CONNECT	50	NO CONNECT
16	H4	115	D20	82	D1	49	$\overline{DS}$
15	H5	114	D19	81	D0	48	$X/\overline{Y}$
14	H6	113	D18	80	A15	47	$\overline{RD}$
13	PERIPHERAL VCC	112	DATA BUS GND	79	A14	46	$\overline{WR}$
12	PERIPHERAL VCC	111	DATA BUS GND	78	NO CONNECT	45	$\overline{BR}$
11	H7	110	NO CONNECT	77	A13	44	NO CONNECT
10	$\overline{HREQ}$	109	D17	76	A12	43	$\overline{BG}$
9	$\overline{HR/W}$	108	D16	75	A11	42	SRD
8	$\overline{HEN}$	107	NO CONNECT	74	ADDRESS BUS GND	41	NO CONNECT
7	NO CONNECT	106	D15	73	ADDRESS BUS GND	40	SC1
6	$\overline{HACK}$	105	D14	72	NO CONNECT	39	STD
5	HA0	104	D13	71	A10	38	NO CONNECT
4	NO CONNECT	103	NO CONNECT	70	A9	37	SC2
3	NO CONNECT	102	D12	69	NO CONNECT	36	INTERNAL LOGIC VCC
2	HA1	101	DATA BUS VCC	68	A8	35	INTERNAL LOGIC VCC
1	HA2	100	DATA BUS VCC	67	A7	34	INTERNAL LOGIC GND
132	NO CONNECT	99	D11	66	NO CONNECT	33	INTERNAL LOGIC GND
131	INTERNAL LOGIC GND	98	NO CONNECT	65	A6	32	SCK
130	INTERNAL LOGIC GND	97	D10	64	ADDRESS BUS VCC	31	SC0
129	INTERNAL LOGIC VCC	96	D9	63	ADDRESS BUS VCC	30	NO CONNECT
128	INTERNAL LOGIC VCC	95	NO CONNECT	62	NO CONNECT	29	SCLK
127	EXTAL	94	D8	61	A5	28	TXD
126	XTAL	93	D7	60	A4	27	RXD
125	NO CONNECT	92	D6	59	NO CONNECT	26	NO CONNECT
124	$\overline{RESET}$	91	DATA BUS GND	58	A3	25	H0
123	$\overline{MODA/IRQA}$	90	DATA BUS GND	57	A2	24	PERIPHERAL GND
122	NO CONNECT	89	NO CONNECT	56	ADDRESS BUS GND	23	PERIPHERAL GND
121	$\overline{NMI/MODB/IRQB}$	88	D5	55	ADDRESS BUS GND	22	H1
120	D23	87	D4	54	A1	21	NO CONNECT
119	D22	86	D3	53	A0	20	H2
118	D21	85	D2	52	$\overline{PS}$	19	H3
117	NO CONNECT	84	NO CONNECT	51	NO CONNECT	18	NO CONNECT

Note: Do not connect to "NO CONNECT" pins.  
 "NO CONNECT" pins are reserved for future enhancements.

**Mechanical Specification Figure A-2. Ceramic Quad Flat Pack**

**Mechanical Specification Figure A-2. Ceramic Quad Flat Pack (Continued)**

**Mechanical Specification Figure A-3. Plastic Quad Flat Pack**

**Mechanical Specification Figure A-3. Plastic Quad Flat Pack (Continued)**





Figure B-3 shows the DSP56001 bootstrapping via the Host Port from an MC68000.

Systems with external program memory can load the on-chip PRAM without using the bootstrap mode. In Figure B-4, the

DSP56001 is operated in mode 2 with external program memory at location \$E000. The programmer can overlay the high speed on-chip PRAM with DSP algorithms by using the MOVEM instruction.

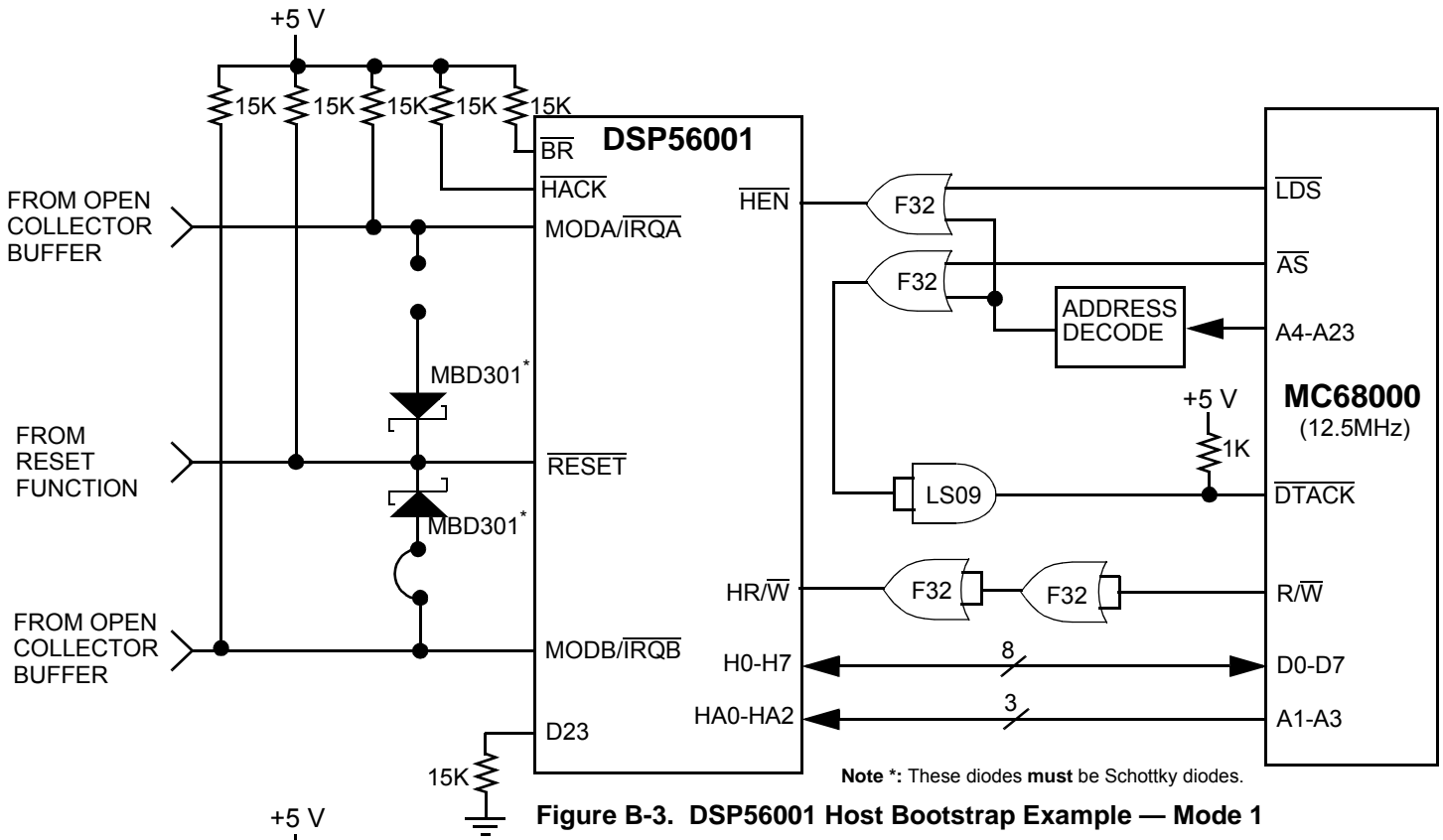


Figure B-3. DSP56001 Host Bootstrap Example — Mode 1

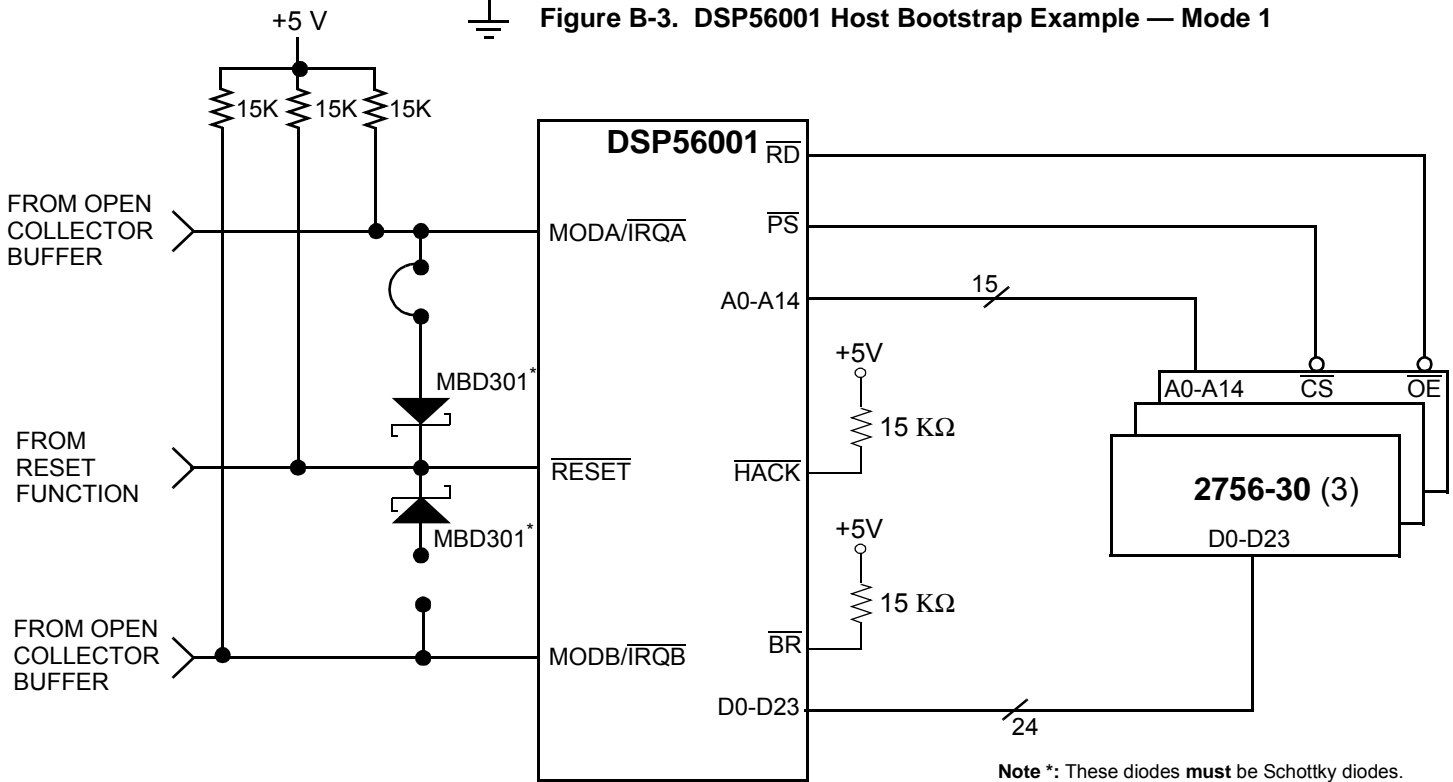


Figure B-4. 32K Words of External Program ROM — Mode 2

Figure B-5 shows an alternative clock oscillator circuit used in the Graphic Equalizer application note (APR2). The 330Ω resistor provides additional current limiting in the crystal. Figure B-6 shows a circuit which waits until Vcc on the DSP is at least 4.5 V

before initiating a 3.75 ms minimum (150,000T) oscillator stabilization delay required for the on-chip oscillator (only 50T is required for an external oscillator). This insures that the DSP is operational and stable before releasing the reset signal.

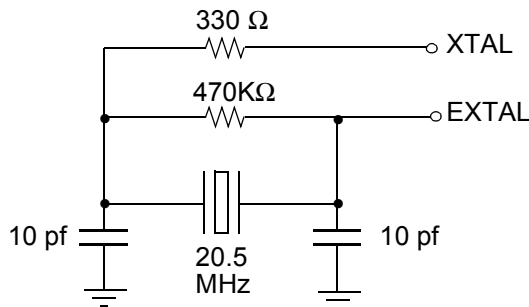


Figure B-5. Alternative Clock Circuit from the Graphic Equalizer (APR2)

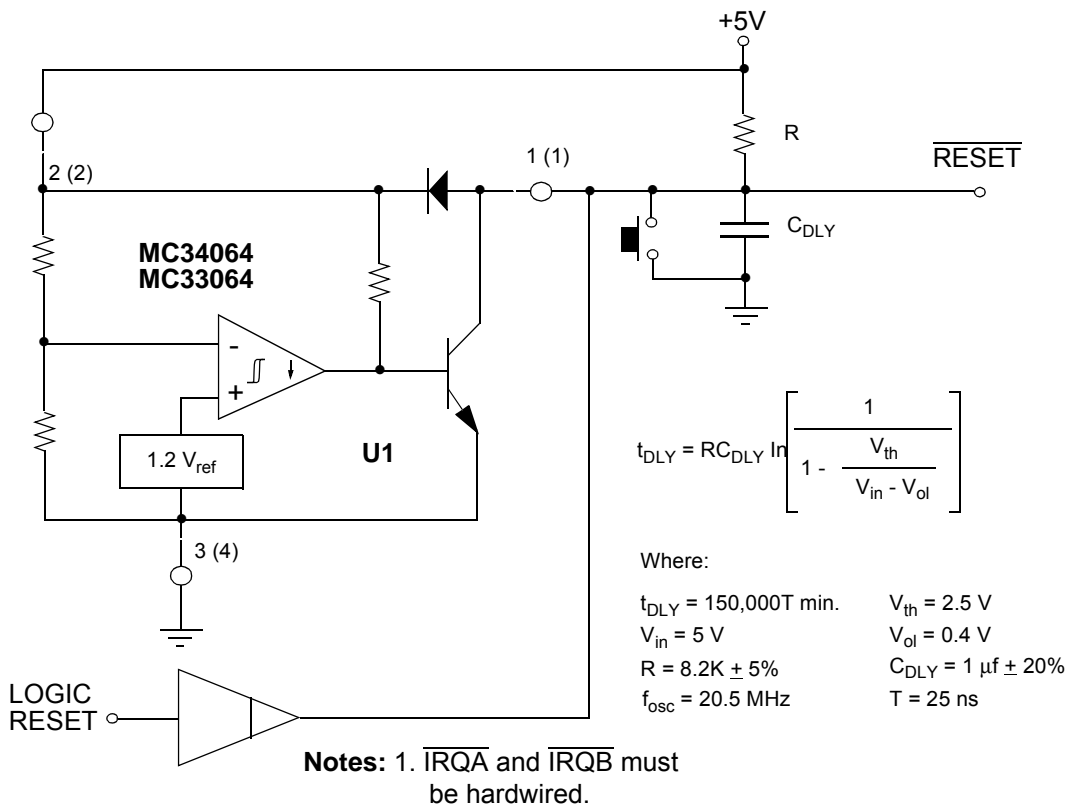


Figure B-6. Reset Circuit Using MC34064/MC33064

Figure 7 illustrates how to connect a 20 ns static RAM with a 33 MHz DSP56001. The important parameters are  $T_{DW} \leq 10$  ns,  $T_{DOE} \leq 10$  ns, and  $T_{AA} = 20$  ns maximum. A 7.5 ns PLD is used to minimize decoding delays. This example maps the static RAM

into the ranges X:\$1000-1FFF and Y:\$1000-1FFF. The PLD equation is:

$$\overline{RAM\_ENABLE} = \overline{PS} \& \overline{!DS} \& \overline{!A15} \& \overline{!A14} \& \overline{!A13} \& \overline{!A12}$$

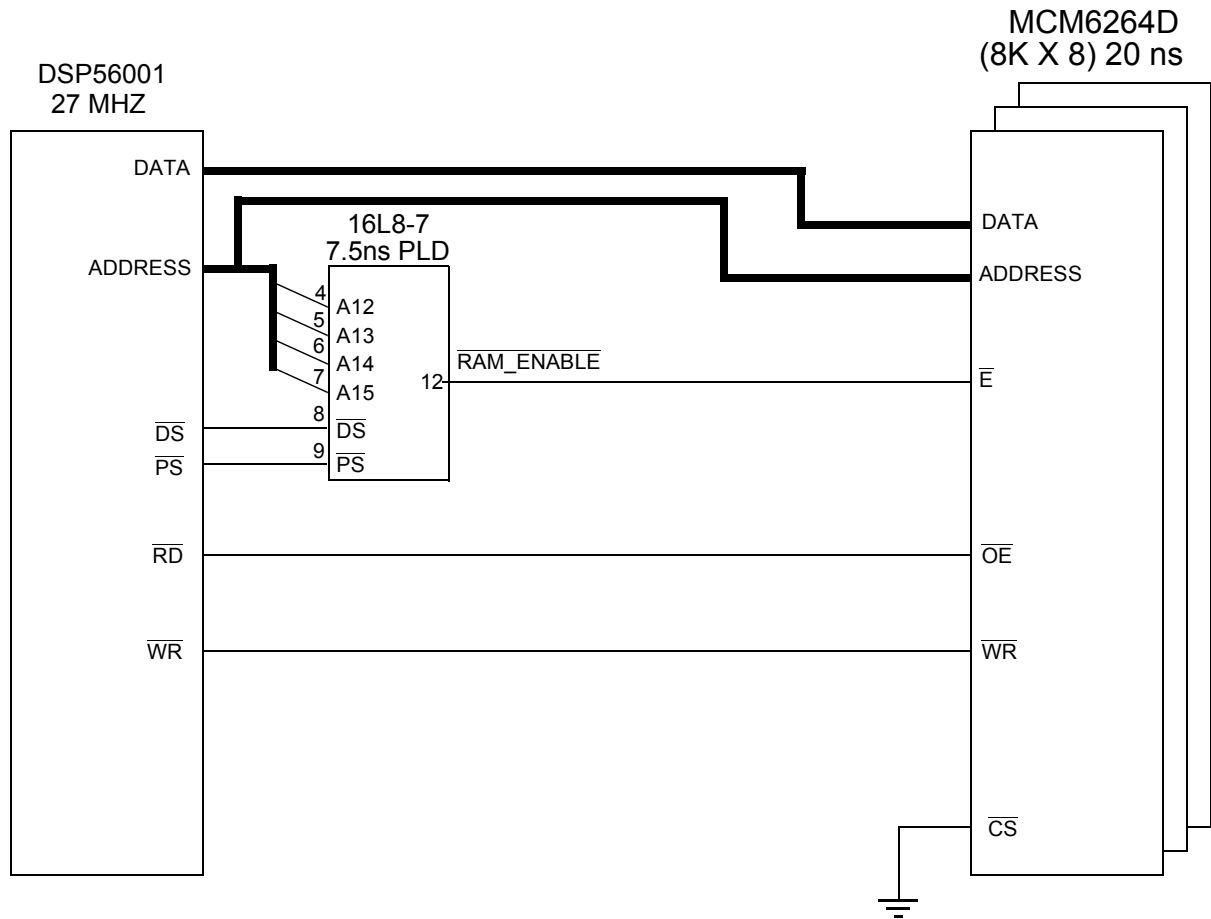


Figure B-7. 27 MHz DSP56001 with 20 ns SRAM

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Figure B-8 shows the DSP56001 connected to the bus of an IBM-PC computer. The PAL equations and other details of this circuit are available in "An ISA BUS INTERFACE FOR THE

DSP56001" which is provided on request by the Freescale DSP Marketing Department (512-891-2030).

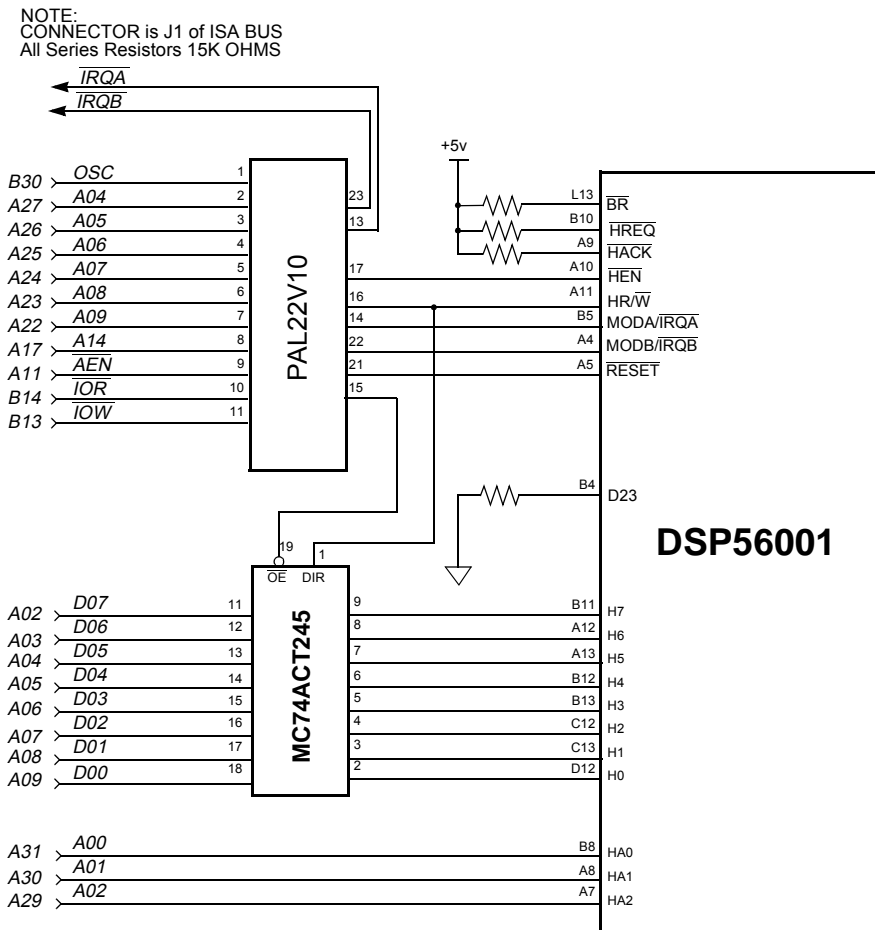


Figure B-8. DSP56001-to-ISA Bus Interface Schematic

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## APPENDIX C MU-LAW / A-LAW EXPANSION TABLES

	ORG	X:\$100		M_3F	DC	\$07BC00	;	495
;				M_40	DC	\$075C00	;	471
M_00	DC	\$7D7C00	;	8031				
M_01	DC	\$797C00	;	7775				
M_02	DC	\$757C00	;	7519				
M_03	DC	\$717C00	;	7263				
M_04	DC	\$6D7C00	;	7007				
M_05	DC	\$697C00	;	6751				
M_06	DC	\$657C00	;	6495				
M_07	DC	\$617C00	;	6239				
M_08	DC	\$5D7C00	;	5983				
M_09	DC	\$597C00	;	5727				
M_0A	DC	\$557C00	;	5471				
M_0B	DC	\$517C00	;	5215				
M_0C	DC	\$4D7C00	;	4959				
M_0D	DC	\$497C00	;	4703				
M_0E	DC	\$457C00	;	4447				
M_0F	DC	\$417C00	;	4191				
M_10	DC	\$3E7C00	;	3999				
M_11	DC	\$3C7C00	;	3871				
M_12	DC	\$3A7C00	;	3743				
M_13	DC	\$387C00	;	3615				
M_14	DC	\$367C00	;	3487				
M_15	DC	\$347C00	;	3359				
M_16	DC	\$327C00	;	3231				
M_17	DC	\$307C00	;	3103				
M_18	DC	\$2E7C00	;	2975				
M_19	DC	\$2C7C00	;	2847				
M_1A	DC	\$2A7C00	;	2719				
M_1B	DC	\$287C00	;	2591				
M_1C	DC	\$267C00	;	2463				
M_1D	DC	\$247C00	;	2335				
M_1E	DC	\$227C00	;	2207				
M_1F	DC	\$207C00	;	2079				
M_20	DC	\$1EFC00	;	1983				
M_21	DC	\$1DFC00	;	1919				
M_22	DC	\$1CFC00	;	1855				
M_23	DC	\$1BFC00	;	1791				
M_24	DC	\$1AFC00	;	1727				
M_25	DC	\$19FC00	;	1663				
M_26	DC	\$18FC00	;	1599				
M_27	DC	\$17FC00	;	1535				
M_28	DC	\$16FC00	;	1471				
M_29	DC	\$15FC00	;	1407				
M_2A	DC	\$14FC00	;	1343				
M_2B	DC	\$13FC00	;	1279				
M_2C	DC	\$12FC00	;	1215				
M_2D	DC	\$11FC00	;	1151				
M_2E	DC	\$10FC00	;	1087				
M_2F	DC	\$0FFC00	;	1023				
M_30	DC	\$0F3C00	;	975				
M_31	DC	\$0EBC00	;	943				
M_32	DC	\$0E3C00	;	911				
M_33	DC	\$0DBC00	;	879				
M_34	DC	\$0D3C00	;	847				
M_35	DC	\$0CBC00	;	815				
M_36	DC	\$0C3C00	;	783				
M_37	DC	\$0BBC00	;	751				
M_38	DC	\$0B3C00	;	719				
M_39	DC	\$0ABC00	;	687				
M_3A	DC	\$0A3C00	;	655				
M_3B	DC	\$09BC00	;	623				
M_3C	DC	\$093C00	;	591				
M_3D	DC	\$08BC00	;	559				
M_3E	DC	\$083C00	;	527				
				M_41	DC	\$071C00	;	455
				M_42	DC	\$06DC00	;	439
				M_43	DC	\$069C00	;	423
				M_44	DC	\$065C00	;	407
				M_45	DC	\$061C00	;	391
				M_46	DC	\$05DC00	;	375
				M_47	DC	\$059C00	;	359
				M_48	DC	\$055C00	;	343
				M_49	DC	\$051C00	;	327
				M_4A	DC	\$04DC00	;	311
				M_4B	DC	\$049C00	;	295
				M_4C	DC	\$045C00	;	279
				M_4D	DC	\$041C00	;	263
				M_4E	DC	\$03DC00	;	247
				M_4F	DC	\$039C00	;	231
				M_50	DC	\$036C00	;	219
				M_51	DC	\$034C00	;	211
				M_52	DC	\$032C00	;	203
				M_53	DC	\$030C00	;	195
				M_54	DC	\$02EC00	;	187
				M_55	DC	\$02CC00	;	179
				M_56	DC	\$02AC00	;	171
				M_57	DC	\$028C00	;	163
				M_58	DC	\$026C00	;	155
				M_59	DC	\$024C00	;	147
				M_5A	DC	\$022C00	;	139
				M_5B	DC	\$020C00	;	131
				M_5C	DC	\$01EC00	;	123
				M_5D	DC	\$01CC00	;	115
				M_5E	DC	\$01AC00	;	107
				M_5F	DC	\$018C00	;	99
				M_60	DC	\$017400	;	93
				M_61	DC	\$016400	;	89
				M_62	DC	\$015400	;	85
				M_63	DC	\$014400	;	81
				M_64	DC	\$013400	;	77
				M_65	DC	\$012400	;	73
				M_66	DC	\$011400	;	69
				M_67	DC	\$010400	;	65
				M_68	DC	\$00F400	;	61
				M_69	DC	\$00E400	;	57
				M_6A	DC	\$00D400	;	53
				M_6B	DC	\$00C400	;	49
				M_6C	DC	\$00B400	;	45
				M_6D	DC	\$00A400	;	41
				M_6E	DC	\$009400	;	37
				M_6F	DC	\$008400	;	33
				M_70	DC	\$007800	;	30
				M_71	DC	\$007000	;	28
				M_72	DC	\$006800	;	26
				M_73	DC	\$006000	;	24
				M_74	DC	\$005800	;	22
				M_75	DC	\$005000	;	20
				M_76	DC	\$004800	;	18
				M_77	DC	\$004000	;	16
				M_78	DC	\$003800	;	14
				M_79	DC	\$003000	;	12
				M_7A	DC	\$002800	;	10
				M_7B	DC	\$002000	;	8
				M_7C	DC	\$001800	;	6
				M_7D	DC	\$001000	;	4
				M_7E	DC	\$000800	;	2
				M_7F	DC	\$000000	;	0

Figure C-1. Mu-Law/A-Law Expansion Table Contents (Sheet 1 of 2)

# Freescale Semiconductor, Inc.

A_80	DC	\$158000	;	688	A_C0	DC	\$015800	;	43
A_81	DC	\$148000	;	656	A_C1	DC	\$014800	;	41
A_82	DC	\$178000	;	752	A_C2	DC	\$017800	;	47
A_83	DC	\$168000	;	720	A_C3	DC	\$016800	;	45
A_84	DC	\$118000	;	560	A_C4	DC	\$011800	;	35
A_85	DC	\$108000	;	528	A_C5	DC	\$010800	;	33
A_86	DC	\$138000	;	624	A_C6	DC	\$013800	;	39
A_87	DC	\$128000	;	592	A_C7	DC	\$012800	;	37
A_88	DC	\$1D8000	;	944	A_C8	DC	\$01D800	;	59
A_89	DC	\$1C8000	;	912	A_C9	DC	\$01C800	;	57
A_8A	DC	\$1F8000	;	1008	A_CA	DC	\$01F800	;	63
A_8B	DC	\$1E8000	;	976	A_CB	DC	\$01E800	;	61
A_8C	DC	\$198000	;	816	A_CC	DC	\$019800	;	51
A_8D	DC	\$188000	;	784	A_CD	DC	\$018800	;	49
A_8E	DC	\$1B8000	;	880	A_CE	DC	\$01B800	;	55
A_8F	DC	\$1A8000	;	848	A_CF	DC	\$01A800	;	53
A_90	DC	\$0AC000	;	344	A_D0	DC	\$005800	;	11
A_91	DC	\$0A4000	;	328	A_D1	DC	\$004800	;	9
A_92	DC	\$0BC000	;	376	A_D2	DC	\$007800	;	15
A_93	DC	\$0B4000	;	360	A_D3	DC	\$006800	;	13
A_94	DC	\$08C000	;	280	A_D4	DC	\$001800	;	3
A_95	DC	\$084000	;	264	A_D5	DC	\$000800	;	1
A_96	DC	\$09C000	;	312	A_D6	DC	\$003800	;	7
A_97	DC	\$094000	;	296	A_D7	DC	\$002800	;	5
A_98	DC	\$0EC000	;	472	A_D8	DC	\$00D800	;	27
A_99	DC	\$0E4000	;	456	A_D9	DC	\$00C800	;	25
A_9A	DC	\$0FC000	;	504	A_DA	DC	\$00F800	;	31
A_9B	DC	\$0F4000	;	488	A_DB	DC	\$00E800	;	29
A_9C	DC	\$0CC000	;	408	A_DC	DC	\$009800	;	19
A_9D	DC	\$0C4000	;	392	A_DD	DC	\$008800	;	17
A_9E	DC	\$0DC000	;	440	A_DE	DC	\$00B800	;	23
A_9F	DC	\$0D4000	;	424	A_DF	DC	\$00A800	;	21
A_A0	DC	\$560000	;	2752	A_E0	DC	\$056000	;	172
A_A1	DC	\$520000	;	2624	A_E1	DC	\$052000	;	164
A_A2	DC	\$5E0000	;	3008	A_E2	DC	\$05E000	;	188
A_A3	DC	\$5A0000	;	2880	A_E3	DC	\$05A000	;	180
A_A4	DC	\$460000	;	2240	A_E4	DC	\$046000	;	140
A_A5	DC	\$420000	;	2112	A_E5	DC	\$042000	;	132
A_A6	DC	\$4E0000	;	2496	A_E6	DC	\$04E000	;	156
A_A7	DC	\$4A0000	;	2368	A_E7	DC	\$04A000	;	148
A_A8	DC	\$760000	;	3776	A_E8	DC	\$076000	;	236
A_A9	DC	\$720000	;	3648	A_E9	DC	\$072000	;	228
A_AA	DC	\$7E0000	;	4032	A_EA	DC	\$07E000	;	252
A_AB	DC	\$7A0000	;	3904	A_EB	DC	\$07A000	;	244
A_AC	DC	\$660000	;	3264	A_EC	DC	\$066000	;	204
A_AD	DC	\$620000	;	3136	A_ED	DC	\$062000	;	196
A_AE	DC	\$6E0000	;	3520	A_EE	DC	\$06E000	;	220
A_AF	DC	\$6A0000	;	3392	A_EF	DC	\$06A000	;	212
A_B0	DC	\$2B0000	;	1376	A_F0	DC	\$02B000	;	86
A_B1	DC	\$290000	;	1312	A_F1	DC	\$029000	;	82
A_B2	DC	\$2F0000	;	1504	A_F2	DC	\$02F000	;	94
A_B3	DC	\$2D0000	;	1440	A_F3	DC	\$02D000	;	90
A_B4	DC	\$230000	;	1120	A_F4	DC	\$023000	;	70
A_B5	DC	\$210000	;	1056	A_F5	DC	\$021000	;	66
A_B6	DC	\$270000	;	1248	A_F6	DC	\$027000	;	78
A_B7	DC	\$250000	;	1184	A_F7	DC	\$025000	;	74
A_B8	DC	\$3B0000	;	1888	A_F8	DC	\$03B000	;	118
A_B9	DC	\$390000	;	1824	A_F9	DC	\$039000	;	114
A_BA	DC	\$3F0000	;	2016	A_FA	DC	\$03F000	;	126
A_BB	DC	\$3D0000	;	1952	A_FB	DC	\$03D000	;	122
A_BC	DC	\$330000	;	1632	A_FC	DC	\$033000	;	102
A_BD	DC	\$310000	;	1568	A_FD	DC	\$031000	;	98
A_BE	DC	\$370000	;	1760	A_FE	DC	\$037000	;	110
A_BF	DC	\$350000	;	1696	A_FF	DC	\$035000	;	106

Figure C-1. Mu-Law/A-Law Expansion Table Contents (Sheet 2 of 2)

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## APPENDIX D SINE WAVE TABLE

This sine wave table is normally used by FFT routines which use bit reversed address pointers. This table can be used as it is for up to 512 point FFTs; however, for larger FFTs, the table must be copied to a different memory location to allow the reverse-carry addressing mode to be used (see Section 5.3.2.3 REVERSE-CARRY MODIFIER (Mn=\$0000) in the DSP56000/DSP56001 Digital Signal Processor User's Manual for additional information).

	ORG	Y:\$100		S_38	DC	\$7D8A5F	; +0.9807853103
				S_39	DC	\$7E1D94	; +0.9852777123
				S_3A	DC	\$7E9D56	; +0.9891765118
				S_3B	DC	\$7F0992	; +0.9924796224
				S_3C	DC	\$7F6237	; +0.9951847792
				S_3D	DC	\$7FA737	; +0.9972904921
				S_3E	DC	\$7FD888	; +0.9987955093
				S_3F	DC	\$7FF622	; +0.9996988773
				S_40	DC	\$7FFFFFF	; +0.9999988808
				S_41	DC	\$7FF622	; +0.9996988773
				S_42	DC	\$7FD888	; +0.9987955093
				S_43	DC	\$7FA737	; +0.9972904921
				S_44	DC	\$7F6237	; +0.9951847792
				S_45	DC	\$7F0992	; +0.9924796224
				S_46	DC	\$7E9D56	; +0.9891765118
				S_47	DC	\$7E1D94	; +0.9852777123
				S_48	DC	\$7D8A5F	; +0.9807853103
				S_49	DC	\$7CE3CF	; +0.9757022262
				S_4A	DC	\$7C29FC	; +0.9700313210
				S_4B	DC	\$7B5D04	; +0.9637761116
				S_4C	DC	\$7A7D05	; +0.9569402933
				S_4D	DC	\$798A24	; +0.9495282173
				S_4E	DC	\$788484	; +0.9415441155
				S_4F	DC	\$776C4F	; +0.9329928160
				S_50	DC	\$7641AF	; +0.9238795042
				S_51	DC	\$7504D3	; +0.9142097235
				S_52	DC	\$73B5EC	; +0.9039893150
				S_53	DC	\$72552D	; +0.8932244182
				S_54	DC	\$70E2CC	; +0.8819212914
				S_55	DC	\$6F5F03	; +0.8700870275
				S_56	DC	\$6DCA0D	; +0.8577286005
				S_57	DC	\$6C2429	; +0.8448535204
				S_58	DC	\$6A6D99	; +0.8314697146
				S_59	DC	\$68A69F	; +0.8175848722
				S_5A	DC	\$66CF81	; +0.8032075167
				S_5B	DC	\$64E889	; +0.7883464098
				S_5C	DC	\$62F202	; +0.7730104923
				S_5D	DC	\$60EC38	; +0.7572088242
				S_5E	DC	\$5ED77D	; +0.7409511805
				S_5F	DC	\$5CB421	; +0.7242470980
				S_60	DC	\$5A827A	; +0.7071068287
				S_61	DC	\$5842DD	; +0.6895405054
				S_62	DC	\$55F5A5	; +0.6715589762
				S_63	DC	\$539B2B	; +0.6531729102
				S_64	DC	\$5133CD	; +0.6343932748
				S_65	DC	\$4EBFE9	; +0.6152315736
				S_66	DC	\$4C3FE0	; +0.5956993103
				S_67	DC	\$49B415	; +0.5758082271
				S_68	DC	\$471CED	; +0.5555701852
				S_69	DC	\$447ACD	; +0.5349975824
				S_6A	DC	\$41CE1E	; +0.5141026974
				S_6B	DC	\$3F174A	; +0.4928981960
				S_6C	DC	\$3C56BA	; +0.4713967144
				S_6D	DC	\$398CDD	; +0.4496113062
				S_6E	DC	\$36BA20	; +0.4275551140
				S_6F	DC	\$33DEF3	; +0.4052414000
				S_70	DC	\$30FBC5	; +0.3826833963
				S_71	DC	\$2E110A	; +0.3598949909
				S_72	DC	\$2B1F35	; +0.3368898928

Figure D-1. Sine Wave Table Contents (Sheet 1 of 3)

# Freescale Semiconductor, Inc.

S_73	DC	\$2826B9	; +0.3136816919	S_B4	DC	\$8582FB	; -0.9569402933
S_74	DC	\$25280C	; +0.2902846038	S_B5	DC	\$84A2FC	; -0.9637761116
S_75	DC	\$2223A5	; +0.2667128146	S_B6	DC	\$83D604	; -0.9700313210
S_76	DC	\$1F19F9	; +0.2429800928	S_B7	DC	\$831C31	; -0.9757022262
S_77	DC	\$1C0B82	; +0.2191012055	S_B8	DC	\$8275A1	; -0.9807853103
S_78	DC	\$18F8B8	; +0.1950902939	S_B9	DC	\$81E26C	; -0.9852777123
S_79	DC	\$15E214	; +0.1709619015	S_BA	DC	\$8162AA	; -0.9891765118
S_7A	DC	\$12C810	; +0.1467303932	S_BB	DC	\$80F66E	; -0.9924796224
S_7B	DC	\$0FAB27	; +0.1224106997	S_BC	DC	\$809DC9	; -0.9951847792
S_7C	DC	\$0C8BD3	; +0.0980170965	S_BD	DC	\$8058C9	; -0.9972904921
S_7D	DC	\$096A90	; +0.0735644996	S_BE	DC	\$802778	; -0.9987955093
S_7E	DC	\$0647D9	; +0.0490676016	S_BF	DC	\$8009DE	; -0.9996988773
S_7F	DC	\$03242B	; +0.0245412998	S_C0	DC	\$800000	; -1.0000000000
S_80	DC	\$000000	; +0.0000000000	S_C1	DC	\$8009DE	; -0.9996988773
S_81	DC	\$FCDBD5	; -0.0245412998	S_C2	DC	\$802778	; -0.9987955093
S_82	DC	\$F9B827	; -0.0490676016	S_C3	DC	\$8058C9	; -0.9972904921
S_83	DC	\$F69570	; -0.0735644996	S_C4	DC	\$809DC9	; -0.9951847792
S_84	DC	\$F3742D	; -0.0980170965	S_C5	DC	\$80F66E	; -0.9924796224
S_85	DC	\$F054D9	; -0.1224106997	S_C6	DC	\$8162AA	; -0.9891765118
S_86	DC	\$ED37F0	; -0.1467303932	S_C7	DC	\$81E26C	; -0.9852777123
S_87	DC	\$EA1DEC	; -0.1709619015	S_C8	DC	\$8275A1	; -0.9807853103
S_88	DC	\$E70748	; -0.1950902939	S_C9	DC	\$831C31	; -0.9757022262
S_89	DC	\$E3F47E	; -0.2191012055	S_CA	DC	\$83D604	; -0.9700313210
S_8A	DC	\$E0E607	; -0.2429800928	S_CB	DC	\$84A2FC	; -0.9637761116
S_8B	DC	\$DDDC5B	; -0.2667128146	S_CC	DC	\$8582FB	; -0.9569402933
S_8C	DC	\$DAD7F4	; -0.2902846038	S_CD	DC	\$8675DC	; -0.9495282173
S_8D	DC	\$D7D947	; -0.3136816919	S_CE	DC	\$877B7C	; -0.9415441155
S_8E	DC	\$D4E0CB	; -0.3368898928	S_CF	DC	\$8893B1	; -0.9329928160
S_8F	DC	\$D1EEF6	; -0.3598949909	S_D0	DC	\$89BE51	; -0.9238795042
S_90	DC	\$CF043B	; -0.3826833963	S_D1	DC	\$8AFB2D	; -0.9142097235
S_91	DC	\$CC210D	; -0.4052414000	S_D2	DC	\$8C4A14	; -0.9039893150
S_92	DC	\$C945E0	; -0.4275551140	S_D3	DC	\$8DAAD3	; -0.8932244182
S_93	DC	\$C67323	; -0.4496113062	S_D4	DC	\$8F1D34	; -0.8819212914
S_94	DC	\$C3A946	; -0.4713967144	S_D5	DC	\$90A0FD	; -0.8700870275
S_95	DC	\$C0E8B6	; -0.4928981960	S_D6	DC	\$9235F3	; -0.8577286005
S_96	DC	\$BE31E2	; -0.5141026974	S_D7	DC	\$93DBD7	; -0.8448535204
S_97	DC	\$BB8533	; -0.5349975824	S_D8	DC	\$959267	; -0.8314697146
S_98	DC	\$B8E313	; -0.5555701852	S_D9	DC	\$975961	; -0.8175848722
S_99	DC	\$B64BEB	; -0.5758082271	S_DA	DC	\$99307F	; -0.8032075167
S_9A	DC	\$B3C020	; -0.5956993103	S_DB	DC	\$9B1777	; -0.7883464098
S_9B	DC	\$B14017	; -0.6152315736	S_DC	DC	\$9D0DFE	; -0.7730104923
S_9C	DC	\$AEC333	; -0.6343932748	S_DD	DC	\$9F13C8	; -0.7572088242
S_9D	DC	\$AC64D5	; -0.6531729102	S_DE	DC	\$A12883	; -0.7409511805
S_9E	DC	\$AA0A5B	; -0.6715589762	S_DF	DC	\$A34BDF	; -0.7242470980
S_9F	DC	\$A7BD23	; -0.6895405054	S_E0	DC	\$A57D86	; -0.7071068287
S_A0	DC	\$A57D86	; -0.7071068287	S_E1	DC	\$A7BD23	; -0.6895405054
S_A1	DC	\$A34BDF	; -0.7242470980	S_E2	DC	\$AA0A5B	; -0.6715589762
S_A2	DC	\$A12883	; -0.7409511805	S_E3	DC	\$AC64D5	; -0.6531729102
S_A3	DC	\$9F13C8	; -0.7572088242	S_E4	DC	\$AEC333	; -0.6343932748
S_A4	DC	\$9D0DFE	; -0.7730104923	S_E5	DC	\$B14017	; -0.6152315736
S_A5	DC	\$9B1777	; -0.7883464098	S_E6	DC	\$B3C020	; -0.5956993103
S_A6	DC	\$99307F	; -0.8032075167	S_E7	DC	\$B64BEB	; -0.5758082271
S_A7	DC	\$975961	; -0.8175848722	S_E8	DC	\$B8E313	; -0.5555701852
S_A8	DC	\$959267	; -0.8314697146	S_E9	DC	\$BB8533	; -0.5349975824
S_A9	DC	\$93DBD7	; -0.8448535204	S_EA	DC	\$BE31E2	; -0.5141026974
S_AA	DC	\$9235F3	; -0.8577286005	S_EB	DC	\$C0E8B6	; -0.4928981960
S_AB	DC	\$90A0FD	; -0.8700870275	S_EC	DC	\$C3A946	; -0.4713967144
S_AC	DC	\$8F1D34	; -0.8819212914	S_ED	DC	\$C67323	; -0.4496113062
S_AD	DC	\$8DAAD3	; -0.8932244182	S_EE	DC	\$C945E0	; -0.4275551140
S_AE	DC	\$8C4A14	; -0.9039893150	S_EF	DC	\$CC210D	; -0.4052414000
S_AF	DC	\$8AFB2D	; -0.9142097235	S_F0	DC	\$CF043B	; -0.3826833963
S_B0	DC	\$89BE51	; -0.9238795042	S_F1	DC	\$D1EEF6	; -0.3598949909
S_B1	DC	\$8893B1	; -0.9329928160	S_F2	DC	\$D4E0CB	; -0.3368898928
S_B2	DC	\$877B7C	; -0.9415441155	S_F3	DC	\$D7D947	; -0.3136816919
S_B3	DC	\$8675DC	; -0.9495282173	S_F4	DC	\$DAD7F4	; -0.2902846038

Figure D-1. Sine Wave Table Contents (Sheet 2 of 3)



# Freescale Semiconductor, Inc.

S_F5	DC	\$DDDC5B	;	-0.2667128146	S_FB	DC	\$F054D9	;	-0.1224106997
S_F6	DC	\$E0E607	;	-0.2429800928	S_FC	DC	\$F3742D	;	-0.0980170965
S_F7	DC	\$E3F47E	;	-0.2191012055	S_FD	DC	\$F69570	;	-0.0735644996
S_F8	DC	\$E70748	;	-0.1950902939	S_FE	DC	\$F9B827	;	-0.0490676016
S_F9	DC	\$EA1DEC	;	-0.1709619015	S_FF	DC	\$FCDBD5	;	-0.0245412998
S_FA	DC	\$ED37F0	;	-0.1467303932					

Figure D-1. Sine Wave Table Contents (Sheet 3 of 3)

## APPENDIX E BOOTSTRAP MODE — OPERATING MODE 1

The bootstrap feature of the DSP56001 consists of four special on-chip modules: the 512 words of PRAM, a 32-word bootstrap ROM, the bootstrap control logic, and the bootstrap firmware program.

### BOOTSTRAP ROM

This 32-word on-chip ROM has been factory programmed to perform the actual bootstrap operation from the memory expansion port (Port A) or from the Host Interface. You have no access to the bootstrap ROM other than through the bootstrap process. Control logic will disable the bootstrap ROM during normal operations.

### BOOTSTRAP CONTROL LOGIC

The bootstrap mode control logic is activated when the DSP56001 is placed in Operating Mode 1. The control logic maps the bootstrap ROM into program memory space as long as the DSP56001 remains in Operating Mode 1. The bootstrap firmware changes operating modes when the bootstrap load is completed. When the DSP56001 exits the reset state in Mode 1, the following actions occur.

1. The control logic maps the bootstrap ROM into the internal DSP program memory space starting at location \$0000. This P: space is read-only.
2. The control logic forces the entire P: space to be write-only memory during the bootstrap loading process. Attempts to read from this space will result in fetches from the read-only bootstrap ROM.
3. Program execution begins at location \$0000 in the bootstrap ROM. The bootstrap ROM program is able to perform the PRAM load through either the memory expansion port from a byte-wide external memory, or through the Host Interface.
4. The bootstrap ROM program executes the following sequence to end the bootstrap operation and begin your program execution.
  - A. Enter Operating Mode 2 by writing to the OMR. This action will be timed to remove the bootstrap ROM from the program memory map and re-enable read/write access to the PRAM.
  - B. The change to Mode 2 is timed exactly to allow the boot program to execute a single cycle instruction then a JMP #00 and begin execution of the program at location \$0000.

You may also select the bootstrap mode by writing Operating Mode 1 into the OMR. This initiates a timed operation to map the bootstrap ROM into the program address space after a delay to allow execution of a single cycle instruction and then a JMP #<00 (e.g., see Bootstrap code for DSP56001) to begin the bootstrap process as described above in steps 1-4. This technique allows the DSP56001 user to reboot the system (with a different program if desired).

### BOOTSTRAP FIRMWARE PROGRAM

Bootstrap ROM contains the bootstrap firmware program that performs initial loading of the DSP56001 PRAM. The program is written in DSP56000/DSP56001 assembly language. It contains two separate methods of initializing the PRAM: loading from a byte-wide memory starting at location P:\$C000 or loading

through the Host Interface. The particular method used is selected by the level of program memory location \$C000, bit 23. If location P:\$C000, bit 23 is read as a one, the external bus version of the bootstrap program will be selected. Typically, a byte wide EPROM will be connected to the DSP56001 Address and Data Bus as shown in Figure B-1 of the applications examples given in **APPENDIX B APPLICATIONS EXAMPLES**. The data contents of the EPROM must be organized as shown below.

Address of External Byte Wide P Memory	Contents Loaded to Internal PRAM at:
P:\$C000	P:\$0000 low byte
P:\$C001	P:\$0000 mid byte
P:\$C002	P:\$0000 high byte
.	.
.	.
.	.
P:\$C5FD	P:\$01FF low byte
P:\$C5FE	P:\$01FF mid byte
P:\$C5FF	P:\$01FF high byte

If location P:\$C000, bit 23 is read as a zero, the Host Interface version of the bootstrap program will be selected. Typically a host microprocessor will be connected to the DSP56001 Host Interface. The host microprocessor must write the Host Interface registers THX, TXM, and then TSL with the desired contents of PRAM from location P:\$0000 up to P:\$01FF. If less than 512 words are to be loaded, the host programmer can exit the bootstrap program and force the DSP56001 to begin executing at location P:\$0000 by setting HF0=1 in the Host Interface during the bootstrap load. In most systems, the DSP56001 responds so fast that handshaking between the DSP56001 and the host is not necessary.

The bootstrap program is shown in flowchart form in Figure E-1 and in assembler listing format in Figure E-2.

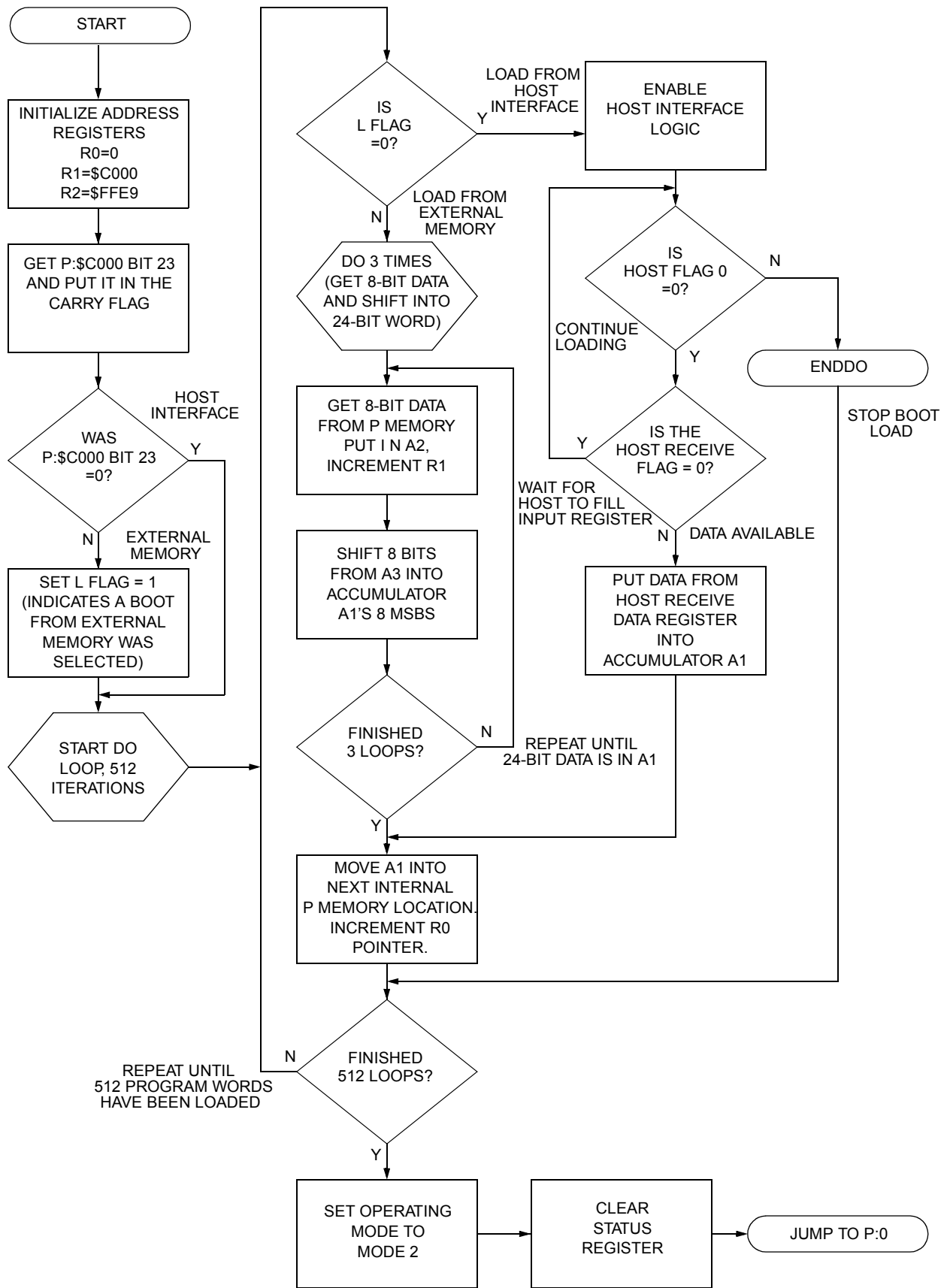


Figure E-1. Bootstrap Program Flowchart

# Freescale Semiconductor, Inc.

Freescale DSP56000 Macro Cross Assembler Version 2.00 87-08-23 09:57:46 bootcode.asm Page 1

```

1          PAGE 132,50,0,10
2          ; BOOTSTRAP SOURCE CODE FOR DSP56001 - (C) Copyright 1986 Motorola Inc.
3          ; Host algorithm / AND / external bus method
4          ; This is the Bootstrap source code contained in the DSP56001 32 word boot ROM.
5          ; This program can load the internal program memory from one of two external sources.
6          ; The program reads P:$C000 bit 23 to decide which external source to access. If
7          ; P:$C000 bit 23 = 0 then it loads internal PRAM from H0-H7, using the Host Interface
8          ; logic. If P:$C000 bit 23 = 1 then it loads from 1,536 consecutive byte-wide P:
9          ; memory locations (starting at P:$C000).
10         0000C000      BOOT      EQU      $C000          ; The location in P: memory
11                                     ; where the external byte-wide
12                                     ; EPROM is expected to be mapped.
13         p:0000          ORG      PL:$0          ; Bootstrap code starts at P:$0
14
15         P:0000      62F400      START      MOVE      #$FFE9,R2      ; R2 = address of the Host
16                                     00FFE9
17
18         P:0002      61F400          MOVE      #BOOT,R1      ; Interface status register.
19                                     00C000          ; R1 = starting P: address of
20
21         P:0004      300000          MOVE      #0,R0          ; external bootstrap byte-wide ROM.
22                                     ; R0 = starting P: address of
23                                     ; internal memory where program
24                                     ; will begin loading.
25
26         P:0005      07E18C          MOVE      P:(R1),AI      ; Get the data at P:$C000
27         P:0006      200037          ROL      A          ; Shift bit 23 into the Carry flag
28         P:0007      0E0009          JCC      <INLOOP      ; Perform load from Host Interface
29                                     ; if carry is zero.
30
31
32         ; IMPORTANT NOTE: This routine assumes that the L bit has been cleared before entering
33         ; this program and that M0 and M1 have been preloaded with $FFFF (linear addressing).
34         ; This would be the case after a reset. If this program is entered by changing the OMR

```

**Figure E-2. Assembler Listing for Bootstrap Program (Sheet 1 of 3)**

# Freescale Semiconductor, Inc.

Freescale DSP56000 Macro Cross Assembler Version 2.00 87-08-23 09:57:46 bootcode.asm Page 2

```
35           ; to bootstrap operating mode, make certain that the L bit is cleared and registers M0
36           ; and M1 have been set to $FFFF. Also, make sure the BCR is set to $xxFx since
37           ; EPROMS are slow and BCR is set to $FFFF after a reset. If the L bit was set before
38           ; changing modes, the program will load from external program memory.
39
40 P:0008    0040F9           ORI    #$40,CCR           ; Set the L bit to indicate
41                                     ; that the bootstrap program
42                                     ; is being loaded from the
43                                     ; external P: space.
44
45           ; The first routine will load 1,536 bytes from the external P: memory space beginning
46           ; at P:$C000 (bits 7-0). These will be packed into 512 24-bit words and stored in
47           ; contiguous internal PRAM memory locations starting at P:$0.
48
49           ; The shifter moves the 8-bit input data from register A2 into register A1 eight bits
50           ; at a time. After assembling one 24-bit word (this takes three loops) it stores the
51           ; result in internal PRAM and continues until internal PRAM is filled. Note that the
52           ; first routine loads data starting with the least significant byte of P:$0 first.
53
54           ; The second routine loads the internal PRAM using the Host Interface logic.
55           ; If the host only wants to load a portion of the PRAM, the Host Interface bootstrap
56           ; load program can be aborted and execution of the loaded program started, by setting
57           ; the Host Flag (HF0) = 1 at any time during the load from the Host Processor.
58
59 P:0009    060082           INLOOP  D0    #512,_LOOP1           ; Load 512 instruction words.
60          00001B
61
62           ; This is the context switch
63 P:000B    0E6012           JLC    <_HOSTLD           ; Load from the Host Interface
64                                     ; if the Limit flag is clear.
65
66           ; This is the first routine. It loads from external P: memory.
67
68 P:000C    060380           DO     #3,_LOOP2           ; Each instruction has 3 bytes.
69          000010
```

Figure E-2. Assembler Listing for Bootstrap Program (Sheet 2 of 3)

# Freescale Semiconductor, Inc.

Freescale DSP56000 Macro Cross Assembler Version 2.00 87-08-23 09:57:46 bootcode.asm Page 3

```
69 P:000E 07D98A          MOVE          P:(R1)+,A2      ; Get the 8 LSB from external
70                                     ; P: memory.
71 P:000F 0608A0          REP          #8              ; Shift 8 bit data into A1
72 P:0010 200022          ASR          A
73                                     ;
74 P:0011 0C001B          _LOOP2      JMP          <_STORE        ; Get another byte
75                                     ; then put the word in PRAM.
76                                     ; This is the second routine. It loads from the Host Interface pins.
77
78 P:0012 0AA020          _HOSTLD     BSET          #0,X:$FFE0      ; Configure Port B as Host Interface
79 P:0013 0AA983          _LBLA      JCLR          #3,X:$FFE9, _LBLB ; If HF0=1, stop loading data.
80                                     000017
81 P:0015 00008C          ENDDO
82 P:0016 0C001C          JMP          <_BOOTEND      ; Must terminate the DO loop
83 P:0017 0A6280          _LBLB      JCLR          #0,X:(R2), _LBLA ; Wait for HRDF to go high
84                                     000013
85                                     ; (meaning 24-bit data is present)
86 P:0019 54F000          MOVE          X:$FFEB,A1      ; Put 24-bit host data in A1
87                                     00FFEB
88 P:001B 07588C          _STORE     MOVE          A1,P:(R0)+      ; Store 24-bit result in PRAM.
89                                     ;
90                                     _LOOP1      ; and return for another 24-bit word
91                                     ; This is the exit handler that returns execution to normal expanded mode
92                                     ; and jumps to the RESET location.
93
94 P:001C 0502BA          _BOOTEND   MOVEC         #2,0MR      ; Set the operating mode to 2
95                                     ; (and trigger an exit from
96                                     ; bootstrap mode).
97 P:001D 0000B9          ANDI        #$0,CCR          ; Clear SR as if RESET and
98                                     ; introduce delay needed for
99                                     ; Op. Mode change.
100 P:001E 0C0000          JMP          <$              ; Start fetching from PRAM P:$0000
101
```

Freescale DSP56000 Macro Cross Assembler Version 2.00 87-08-23 09:57:46 bootcode.asm Page 4

0 Errors  
0 Warnings

**Figure E-2. Assembler Listing for Bootstrap Program (Sheet 3 of 3)**



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