KMM536512BW/BWG Fast Page Mode
512Kx36 DRAM SIMM Using 256Kx18 DRAM, 5V

GENERAL DESCRIPTION

The Samsung KMM536512BW is a 512K bit x 36 Dynamic RAM high density memory module. The Samsung KMM536512BW consists of four CMOS 256Kx18 bit DRAMs in 40-pin SOJ packages mounted on a 72-pin glass-epoxy substrate. A decoupling capacitor is mounted on the printed circuit board for each DRAM and 25pF capacitor is added for RAS input signal to get better characteristics. The KMM536512BW is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

• Performance Range:

	tRAC	tCAC	tRC
KMM536512BW - 6	60ns	15ns	110ns
KMM536512BW - 7	70ns	20ns	130ns
KMM536512BW - 8	80ns	20ns	150ns

• Fast Page Mode Operation
• $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
• $\overline{RAS}$-only and Hidden refresh capability
• TTL compatible inputs and outputs
• Single +5V±10% power supply
• 512 cycles/8 ms refresh
• JEDEC standard PDPin & pinout
• **PCB : Height(1000mil), single sided component**

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PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	Vss
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	$\overline{RAS1}$
10	Vcc	46	NC
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	NC	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	NC	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	NC	68	PD2
33	$\overline{RAS3}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

PIN NAMES

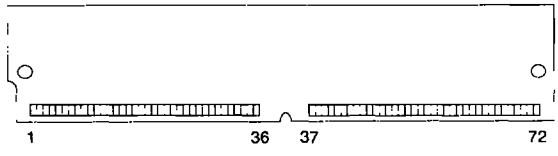
A0 - A8	Address Inputs
DQ0 - DQ35	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 - PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	60NS	70NS	80NS
PD1	NC	NC	NC
PD2	Vss	Vss	Vss
PD3	NC	Vss	NC
PD4	NC	NC	Vss

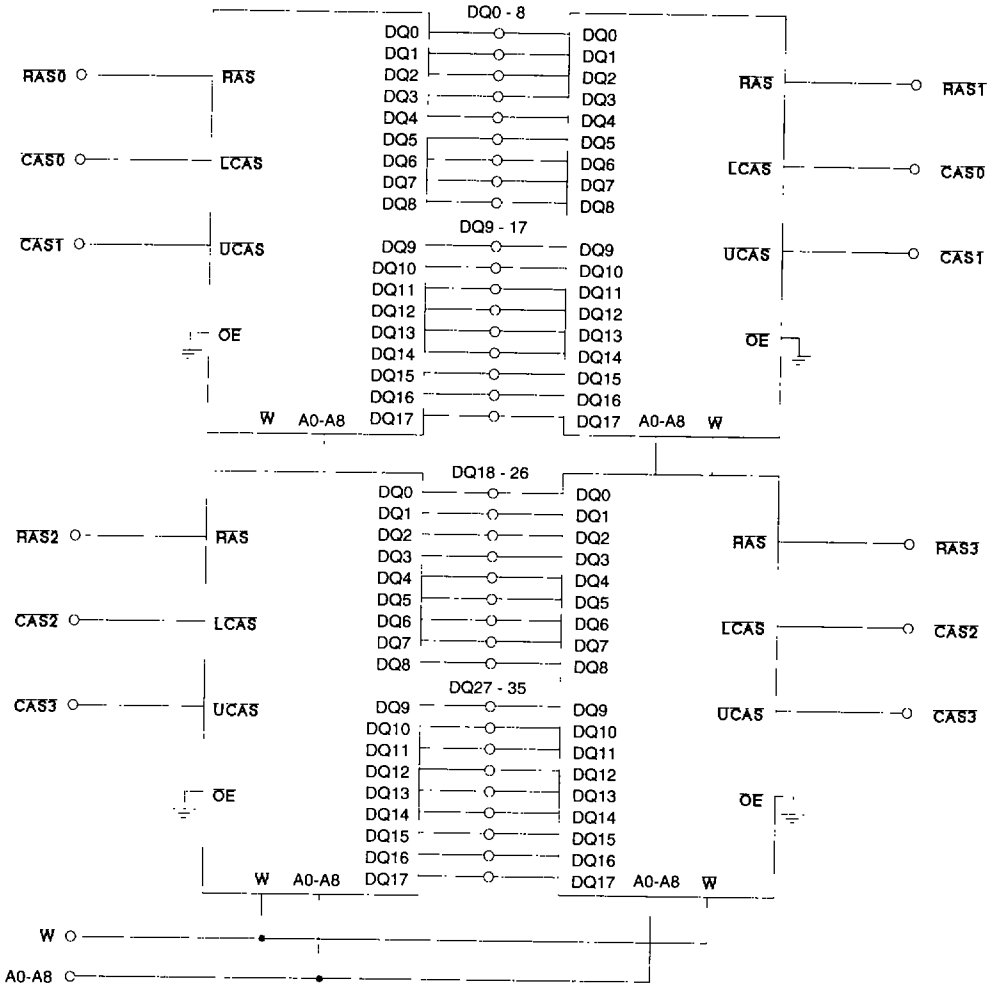
*Pin Connection Changing Available

PIN CONNECTIONS (Front View)



SAMSUNG ELECTRONICS

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	VIN,VOUT	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	Vcc	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	Pd	2.8	W
Short Circuit Output Current	IOS	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta = 0 to 70 °C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	2.4	-	Vcc+1	V
Input Low Voltage	VIL	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Part No	Symbol	Min	Max	Unit
Operating Current * ($\overline{RAS}$, $\overline{LCAS}$ or $\overline{UCAS}$ Address cycling @tRC=min.)	KMM536512BW - 6	ICC1	-	194	mA
	KMM536512BW - 7		-	174	mA
	KMM536512BW - 8		-	164	mA
Standby Current ($\overline{RAS}$=$\overline{LCAS}$=$\overline{UCAS}$=$\overline{W}$=VIH)		ICC2	-	8	mA
$\overline{RAS}$ Only Refresh Current * ($\overline{LCAS}$=$\overline{UCAS}$=VIH, $\overline{RAS}$, Address cycling @tRC=min.)	KMM536512BW - 6	ICC3	-	194	mA
	KMM536512BW - 7		-	174	mA
	KMM536512BW - 8		-	164	mA
Fast Page Mode Current * ($\overline{RAS}$=VIL, $\overline{LCAS}$ or $\overline{UCAS}$, Address cycling @tPC=min.)	KMM536512BW - 6	ICC4	-	124	mA
	KMM536512BW - 7		-	114	mA
	KMM536512BW - 8		-	104	mA
Standby Current ($\overline{RAS}$=$\overline{LCAS}$=$\overline{UCAS}$=$\overline{W}$=Vcc-0.2V)		ICC5	-	4	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC =min.)	KMM536512BW - 6	ICC6	-	194	mA
	KMM536512BW - 7			174	mA
	KMM536512BW - 8			164	mA
Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test = 0 V.)		II(L)	-40	40	µA
Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vcc)		IO(L)	-20	20	µA
Output High Voltage Level (IOH = - 5mA)		VOH	2.4	-	V
Output Low Voltage Level (IOL = 4.2mA)		VOL	-	0.4	V

* NOTE : ICC1,ICC3,ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum two times while $\overline{RAS}$=VIL. In ICC4, address can be changed maximum once within one page mode cycle .

CAPACITANCE (Ta = 25 °C, f=1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance [A0-A8]	CIN1	-	44	pF
Input capacitance [$\overline{W}$]	CIN2	-	48	pF
Input capacitance [$\overline{RAS0}$ - $\overline{RAS3}$]	CIN3	-	22	pF
Input capacitance [$\overline{CAS0}$ - $\overline{CAS3}$]	CIN4	-	29	pF
Input/Output capacitance [DQ0-35]	CDQ1	-	29	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vcc=5.0V±10%. See notes 1,2.)

STANDARD OPERATION	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold referenced to $\overline{RAS}$	tAR	45		55		60		ns	6
Column Address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		10		10		ns	
Write command hold referenced to $\overline{RAS}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	10		15		15		ns	10
Data-in hold referenced to $\overline{RAS}$	tDHR	45		55		60		ns	6
Refresh period	tREF		8		8		8	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ setup time (C-B-R refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time (C-B-R refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	tWRH	10		10		10		ns	
$\overline{CAS}$ precharge(C-B-R counter test)	tCPT	20		25		30		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 **$\overline{RAS}$-only** or **$\overline{CAS}$-before-$\overline{RAS}$ refresh** cycles before proper device operation is achieved.
2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD ≥ tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(MAX)
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenc -ed to VOH or VOL.
8. tWCS is non restrictive operating parameter. It included in the data sheet as electrical characteristic only. If tWCS≥tWCS(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
11. Operation within the tRAD(max) limit insures that tRAC (max) can be met. tRAD(max) is specified as reference point only. If tRAD is greater than the specified tRAD (max) limit, then access time is controlled by tAA.

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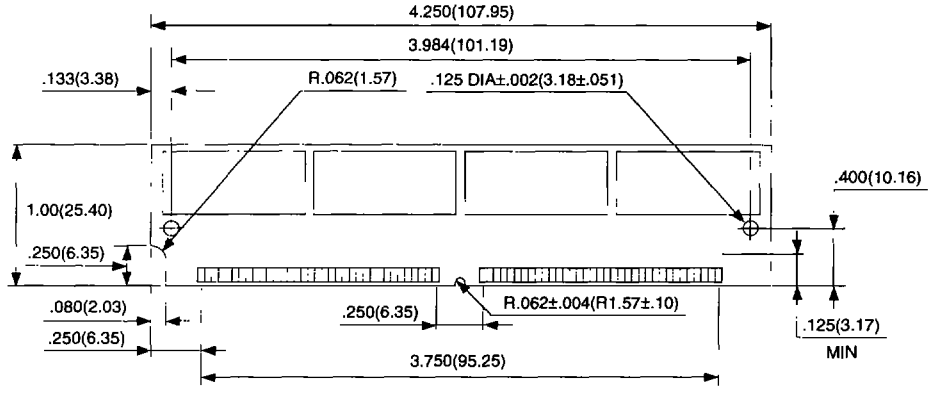
TIMING DIAGRAM

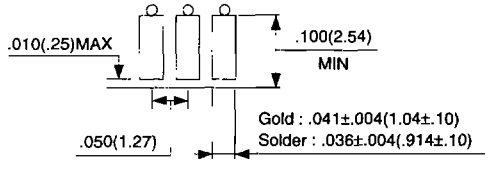
Please refer to attached timing chart (I) !!!

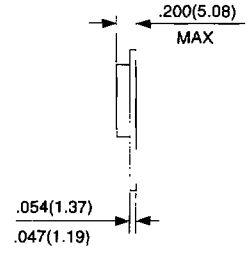
PACKAGE DIMENSIONS (Front View)

Units : Inches (millimeters)



Gold & Solder Plating Lead





Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 256Kx18 DRAM, SOJ.
DRAM Part No. : KM418C256BJ