STL15DN4F5

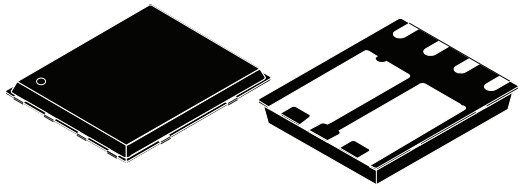
Dual N-channel 40 V, 8 mΩ, 15 A PowerFLAT™(5x6) double island, STripFET™ V Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max.	I_D
STL15DN4F5	40 V	9 mΩ	15 A (1)

1. The value is rated according $R_{thj\text{-}pcb}$

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- Very low switching gate charge
- Low gate drive power losses



PowerFLAT™ (5x6)
Double island

Application

- Switching applications
  - Automotive

Description

The device is a dual N-channel STripFET™ V. This Power MOSFET technology is among the latest improvements, which have been especially tailored to achieve very low on-state resistance providing also one of the best-in-class figure of merit (FOM).

Figure 1. Internal schematic diagram

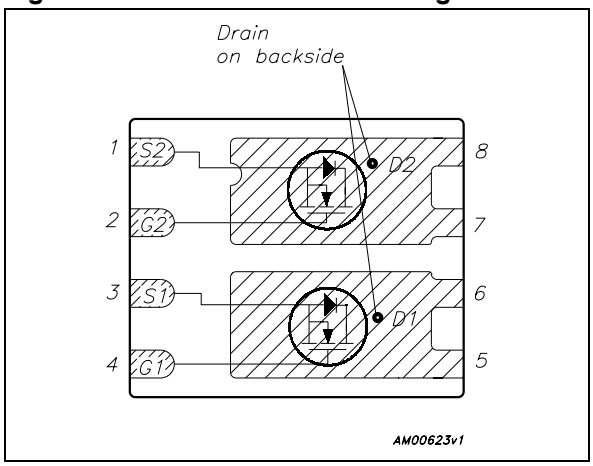


Table 1. Device summary

Order code	Marking	Package	Packaging
STL15DN4F5	15DN4F5	PowerFLAT™(5x6) Double island	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C (silicon limited)	60	A
I_D (2)	Drain current (continuous) at T_C = 25 °C	15	A
I_D (2)	Drain current (continuous) at T_C = 100°C	10	A
I_{DM} (3)	Drain current (pulsed)	60	A
P_{TOT} (1)	Total dissipation at T_C = 25°C	60	W
P_{TOT} (2)	Total dissipation at T_C = 25°C, t < 10 sec	4.3	W
	Derating factor	0.03	W/°C
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. The value is rated according $R_{thj\text{-}c}$
2. The value is rated according $R_{thj\text{-}pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (drain) (steady state)	2.5	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-ambient	35	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec (see *Figure 3*)

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current, (pulse width limited by Tj max.)	7.5	A
E_{AS} (1)	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AV} , V_{DD} = 24 V)	150	mJ

1. Tested at wafer level only.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	40			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 7.5 A		8	9	mΩ

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz V_{GS} = 0	-	1550 230 25	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}= 20 V, I_D = 15 A V_{GS} = 10 V *(see Figure 14)*	-	25 6 5.5	-	nC nC nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 7.5 A,	-	18	-	ns
t_r	Rise time	R_G = 4.7 Ω, V_{GS} = 10 V		45		ns
$t_{d(off)}$	Turn-off delay time	*(see Figure 13)*		32		ns
t_f	Fall time			5		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		15	A
I_{SDM} (1)	Source-drain current (pulsed)		-		60	A
V_{SD} (2)	Forward on voltage	I_{SD} = 15 A, V_{GS} = 0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 15 A,		30		ns
Q_{rr}	Reverse recovery charge	di/dt = 100 A/µs,	-	35		nC
I_{RRM}	Reverse recovery current	V_{DD} = 32 V, Tj = 150 °C		2.2		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

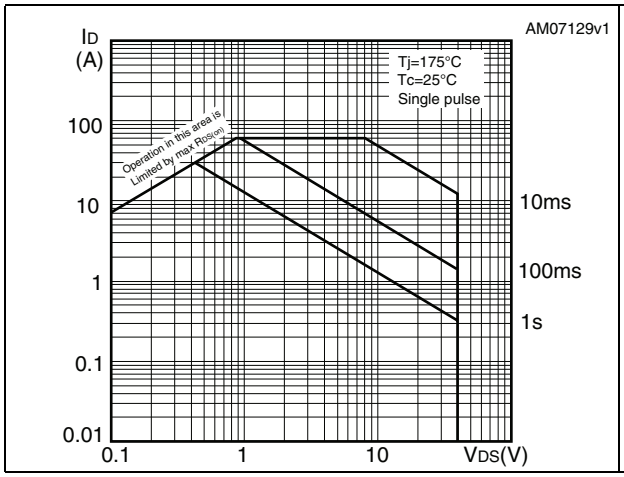


Figure 3. Thermal impedance

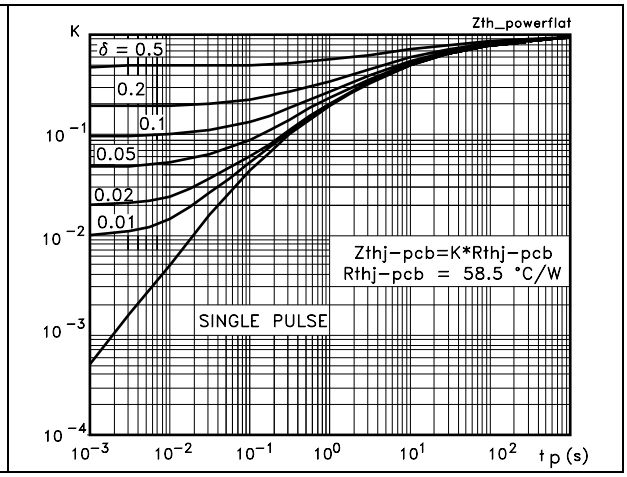


Figure 4. Output characteristics

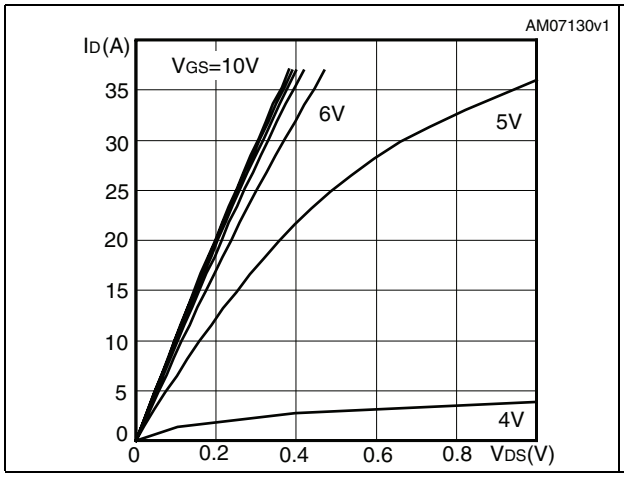


Figure 5. Transfer characteristics

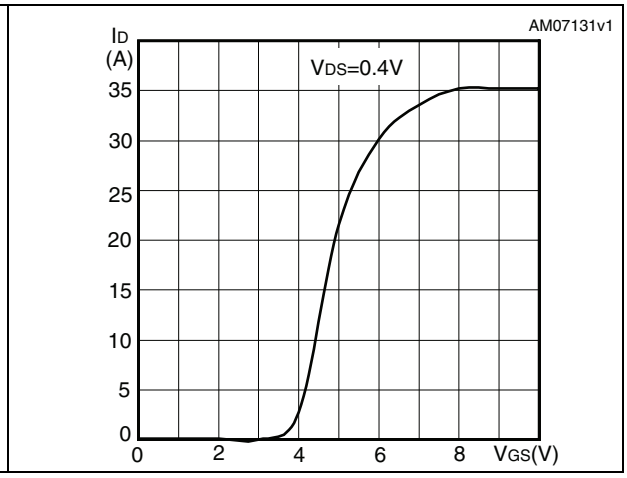


Figure 6. Normalized B_{VDSS} vs temperature

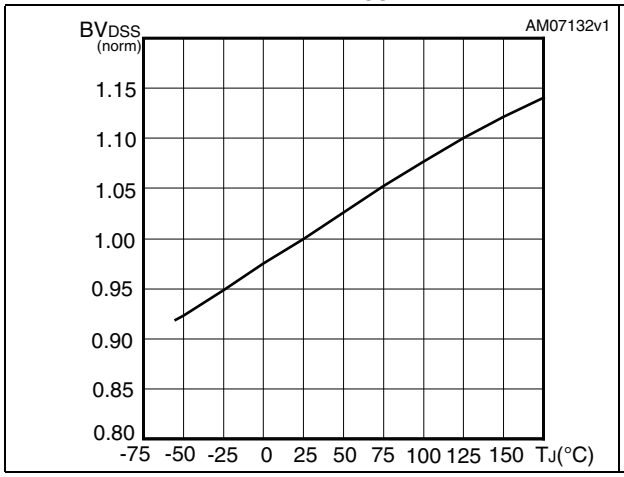


Figure 7. Static drain-source on resistance

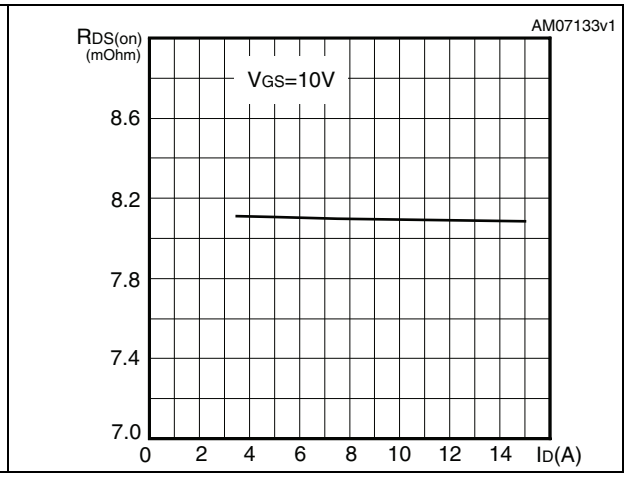


Figure 8. Gate charge vs gate-source voltage

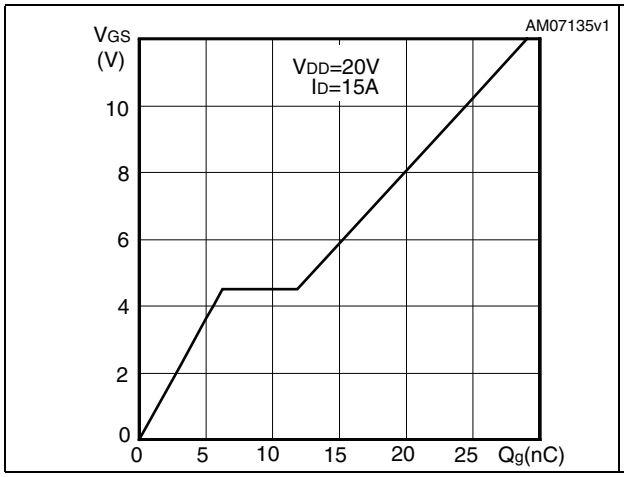


Figure 9. Capacitance variations

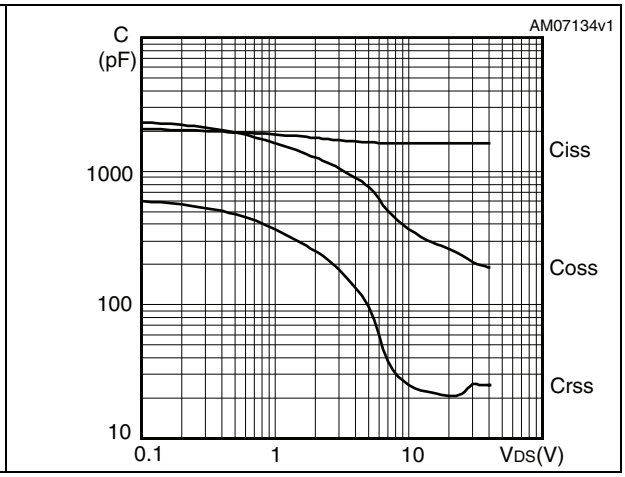


Figure 10. Normalized gate threshold voltage vs temperature

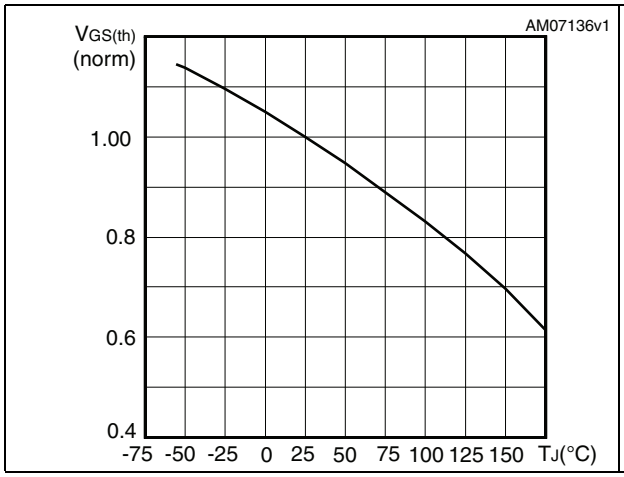


Figure 11. Normalized on resistance vs temperature

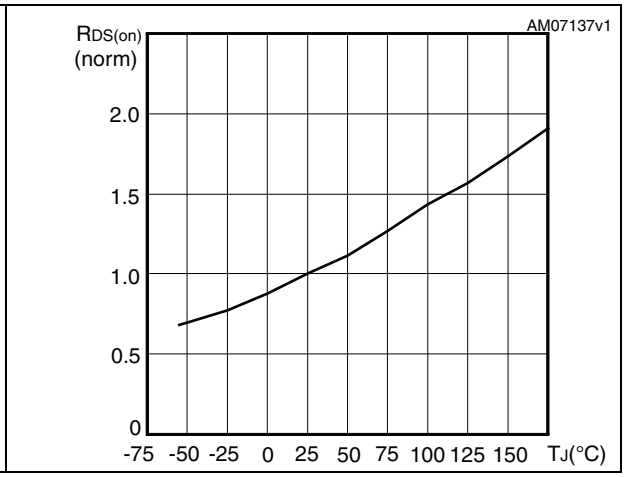
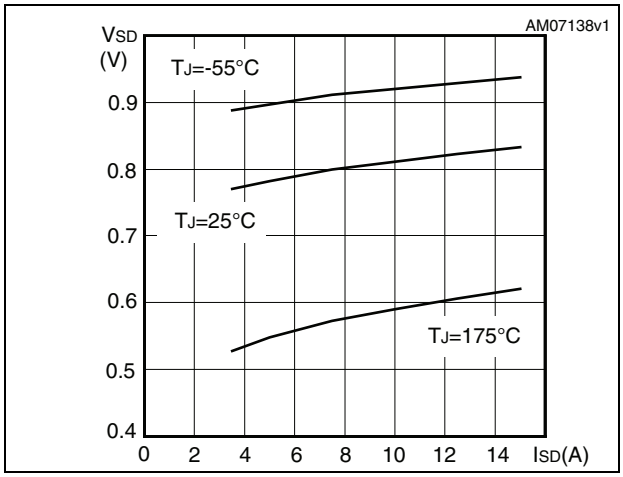


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

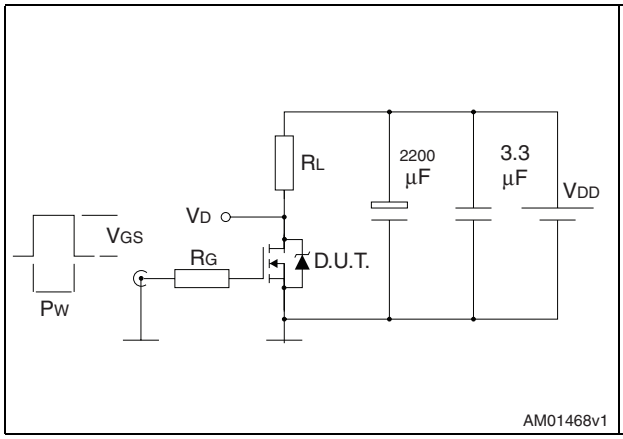


Figure 14. Gate charge test circuit

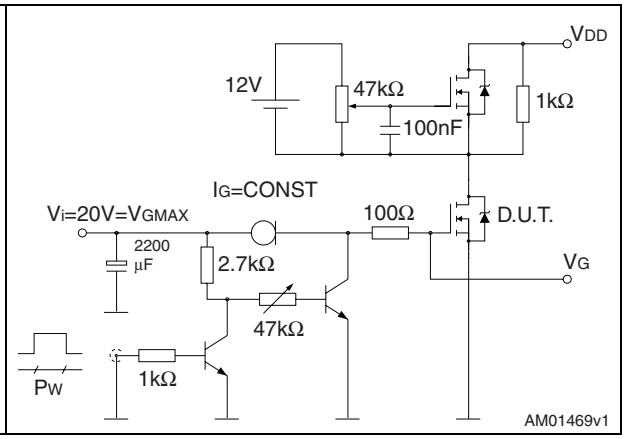


Figure 15. Test circuit for inductive load switching and diode recovery times

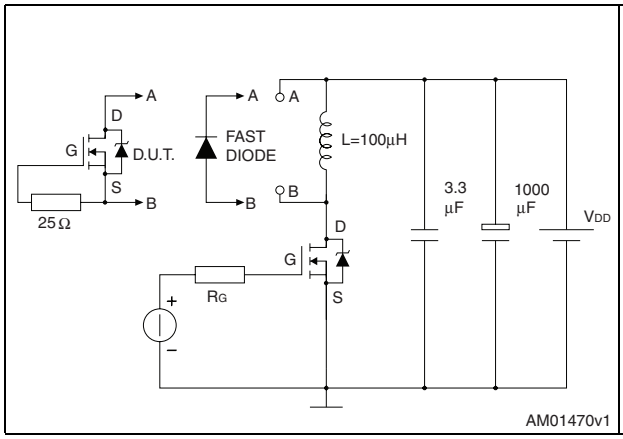


Figure 16. Unclamped inductive load test circuit

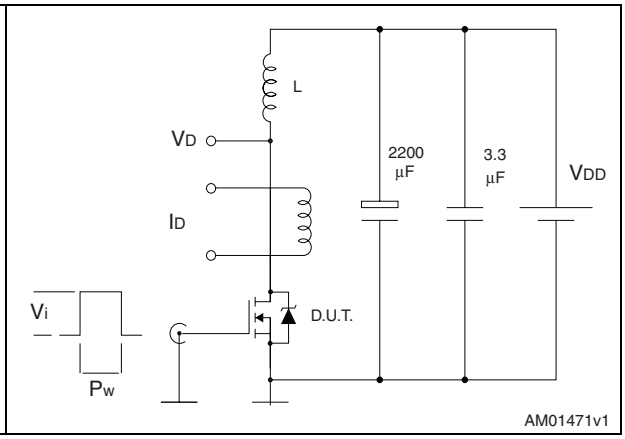


Figure 17. Unclamped inductive waveform

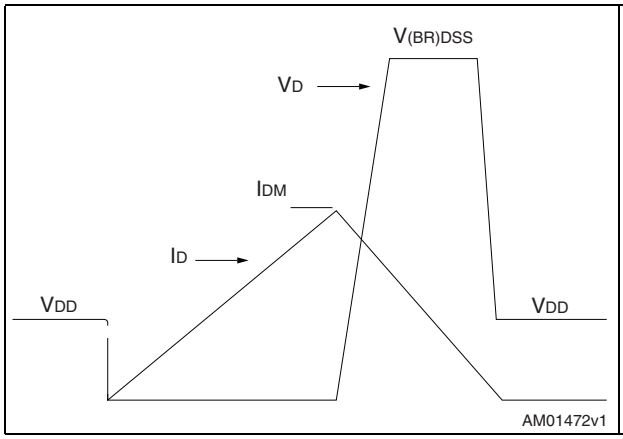
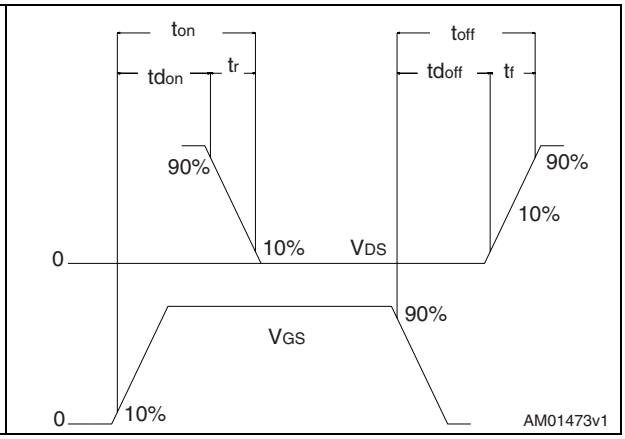


Figure 18. Switching time waveform

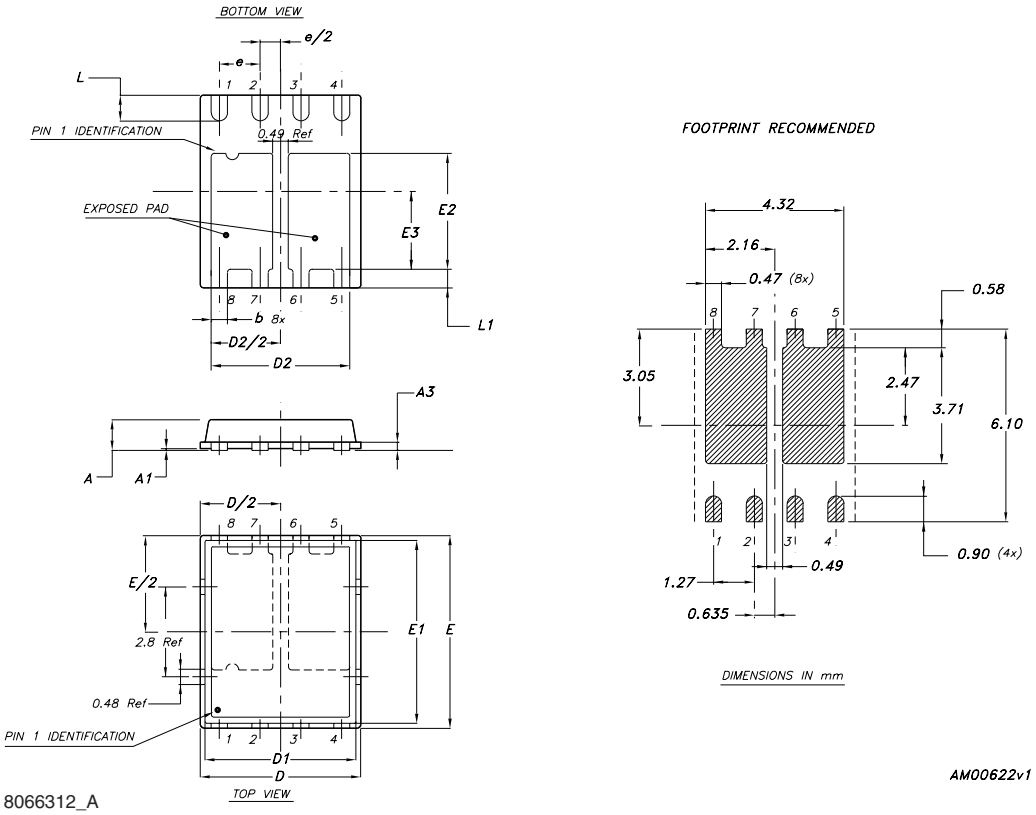


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and products status are available at: www.st.com. ECOPACK is an ST trademark.

PowerFLAT™ (5x6) double island mechanical data

Dim	mm		
	Min	Typ	Max
A	0.80	0.83	0.90
A1		0.02	0.05
A3		0.20	
b	0.35	0.40	0.47
D		5.00	
D1		4.75	
D2	4.11	4.21	4.31
E		6.00	
E1		5.75	
E2	3.51	3.61	3.71
E3	2.32	2.42	2.52
e		1.27	
L	0.70	0.80	0.90
L1	0.48	0.58	0.68



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
02-Sep-2010	1	First release