4.6V 1.2W RF Power Amplifier IC for AMPS
ITT333106BD

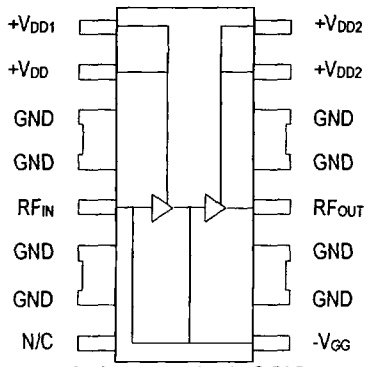
Applications

AMPS Cellular Telephones

Cellular Digital Packet Data (CDPD)

Features

- Class AB Bias
- 750 to 900 MHz Operation
- 50 Ω Input Impedance
- Simple 2 Element Output Match
- Small Size — 16 Pin Narrow Body SOIC Plastic Package
- Self-Aligned MSAG®-Lite MESFET Process
- Guaranteed Stability and Ruggedness



16 pin narrow body SOIC

Typical 4.6 Volt Performance

30.8 dBm Power Output

23.8 dB Power Gain

57% Power Added Efficiency

-35 dBc 2nd Harmonic

-50 dBc 3rd Harmonic

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 1, 2, 15, 16)	V_{DD}	10	Vdc
DC Gate Bias Voltage (Pin 9)	V_{GG}	-5	Vdc
RF Input Power	P_{IN}	15	mW
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-40 to +150	°C

ELECTRICAL CHARACTERISTICS V_{DD}=4.6 V, P_{IN}=+7 dBm, T_S=40 °C (Note 1), Output externally matched to 50 Ω System.

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	f	824	—	849	MHz
Output Power (V_{GG} adjusted for desired output power)	P_{OUT}	1.2	—	—	W
Power Gain (P_{OUT} = 30.8 dBm)	G_P	23.8	—	—	dB
Drain Current (P_{OUT} = 30.8 dBm)	I_{DD}	—	456	510	mA
Harmonics (P_{OUT} = 30 dBm)	$2f_o$	—	-35	-30	dBc
	$3f_o$	—	-50	-45	dBc
Input VSWR (P_{OUT} = 30 dBm), 50 Ω Ref.	—	—	1.2:1	2.0:1	—
Thermal Resistance (Junction of 2nd stage FET to solder point of pin 11)	$R_{TH\ J\text{-}S}$	—	—	21	°C/W
Load Mismatch (V_{DD} = 8.5 V, VSWR = 10:1)	—	No Degradation in Power Output			
Stability (P_{IN}=-3 to +12 dBm, V_{DD}=0-8.5 V, 0 mW < P_{OUT} < 1.2 W, T_S=-40 to +100 °C, Load VSWR = 10:1)	—	All non-harmonically related outputs more than 60 dB below desired signal			

Note 1: T_S is the temperature measured at the soldering point of pin 11, mounted on 60 mil GETEK evaluation board in a free air condition with ambient room temperature T_A=25°C. The electrical data presented herein was taken with the evaluation board shown in Figures 1 & 10, under room temperature conditions , operating at 1.2 W of load power (V_{DD} = 4.6 V), unless otherwise specified.

GaAsTEK
A UNIT OF ITT INDUSTRIES

GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gaastek.com
Tel: 1-540-563-3949
1-888-563-3949 (USA)
Fax: 1-540-563-8616

APPLICATION INFORMATION

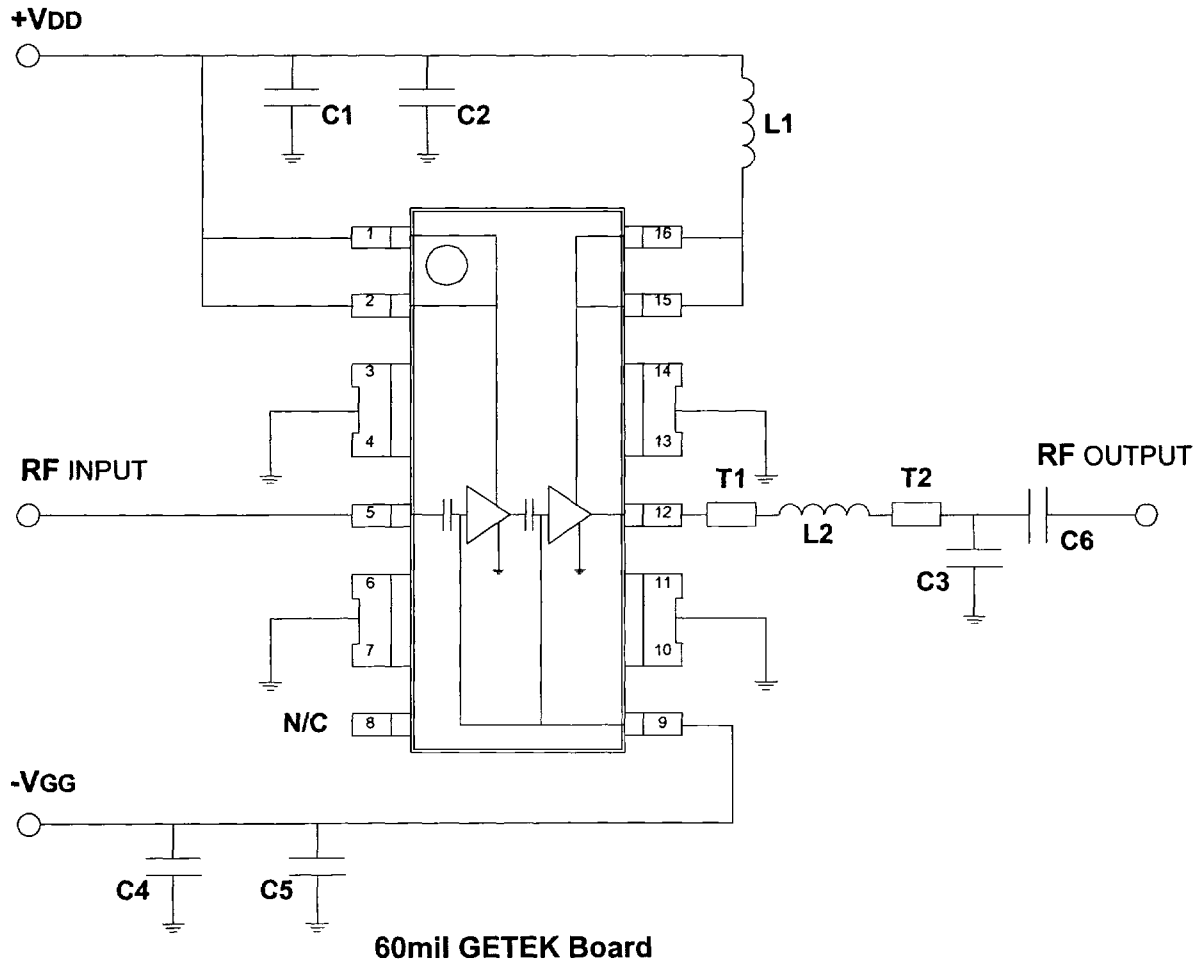


Figure 1. Evaluation Board Schematic

List of components:

C1 = C5 = 0.1µF Kemet multilayer ceramic chip capacitor (C1206C104K5RAC)
C2 = C4 = 4700 pF Kemet multilayer ceramic chip capacitor (C0805C472K5RAC)
C3 = 6.8 pF DLI multilayer ceramic chip capacitor (C11AH6R8B5TXL)
C6 = 100 pF DLI multilayer ceramic chip capacitor (DC Block; C11AH101K5TXL)
L1 = 39 nH Coilcraft chip inductor (1008CS.390XMBB)
L2 = 1.5 nH Toko chip inductor (LL1608-F1N8S)
T1 = 0.10" of 50 Ω grounded coplanar waveguide (60 mil GETEK board)
T2 = 0.12" of 50 Ω grounded coplanar waveguide (60 mil GETEK board)

Component layout and printed circuit board drawing for RF IC evaluation board are shown in Figure 10.

Biasing: Gate bias voltage (V_{GG}) must be applied prior to RF input power and drain bias voltage (V_{DD}). Reverse the sequence when turning the part off — remove the RF input and drain bias before removing gate bias.

GaAsTEK
A UNIT OF ITT INDUSTRIES
GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gaastek.com
Tel: 1-540-563-3949
1-888-563-3949 (USA)
Fax: 1-540-563-8616

TYPICAL CHARACTERISTICS

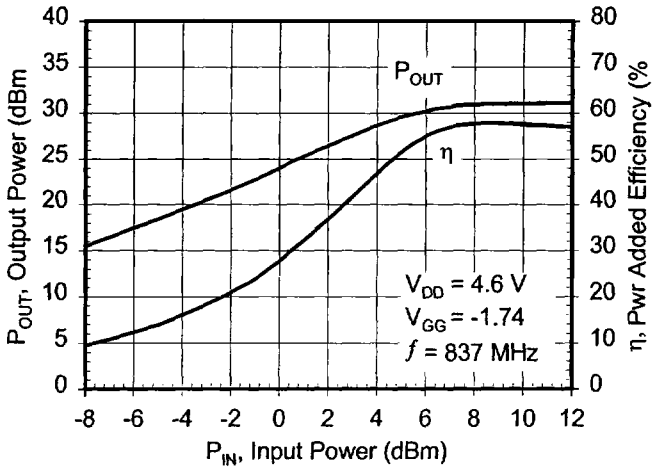


Figure 2. 1.2 Watt output power capability and efficiency vs. Input power

Conditions for Figure 2:
Gate bias (V_{GG}) is set for 1.2 W output power when P_{IN} = 7 dBm.

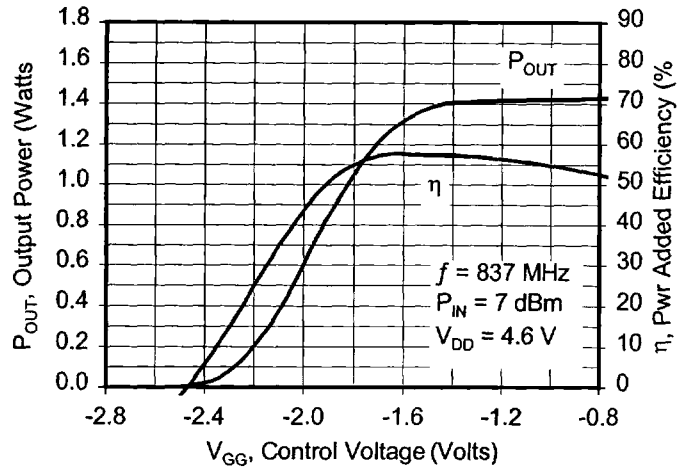


Figure 3. Output power and efficiency vs. control voltage

Conditions for Figure 3:
While keeping supply voltage constant, the output power is controlled by adjusting DC gate bias (V_{GG}).

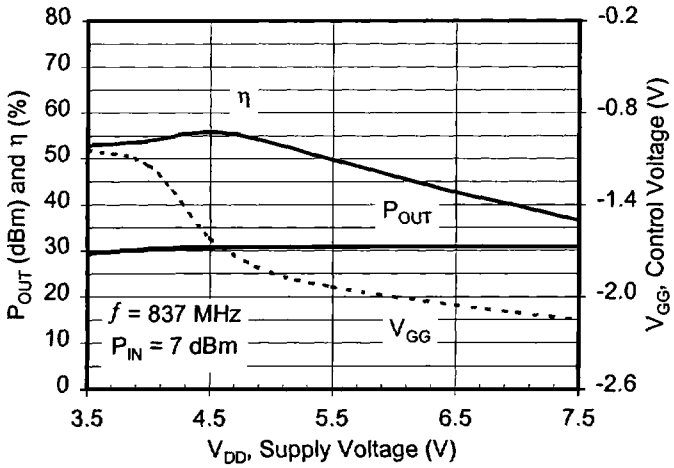


Figure 4. Output power, efficiency, and control voltage vs. supply voltage

Conditions for Figure 4:
Control voltage (V_{GG}) is adjusted for each supply voltage to maintain 1.2 W output power.

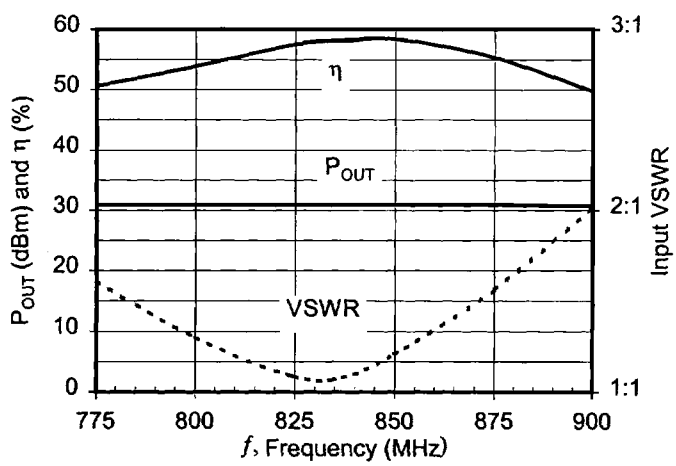


Figure 5. Output power, efficiency, and input VSWR vs. frequency

Conditions for Figure 5:
Control voltage (V_{GG}) is adjusted at each frequency to maintain 1.2 W output power.

GaAsTEK
A UNIT OF ITT INDUSTRIES
GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gaastek.com
Tel: 1-540-563-3949
1-888-563-3949 (USA)
Fax: 1-540-563-8616

TYPICAL CHARACTERISTICS

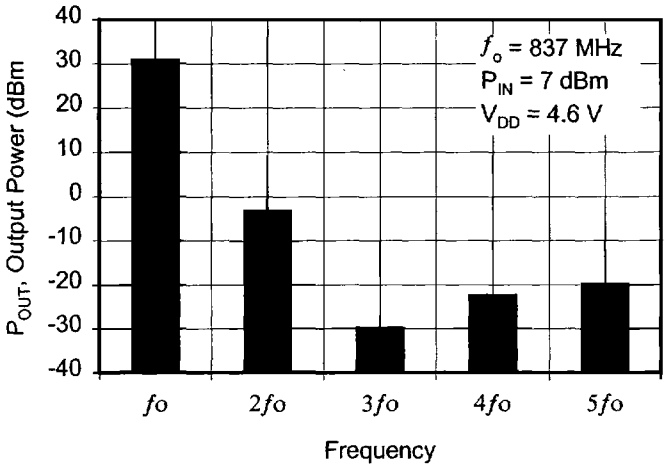


Figure 6. Harmonics

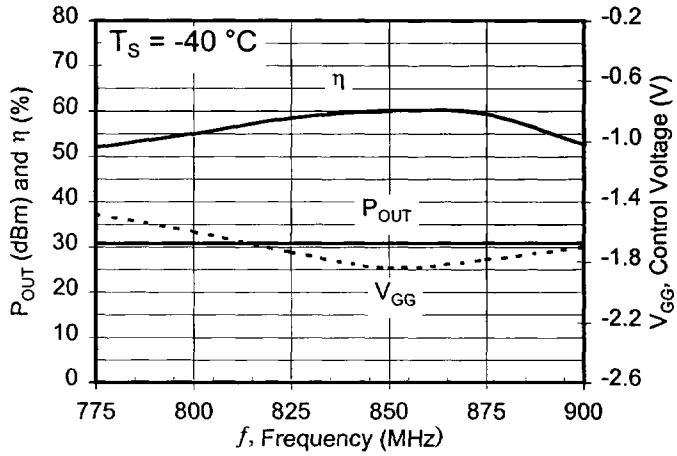


Figure 7. Output power, efficiency, and control voltage vs. frequency for T_S = -40°C

Conditions for Figure 7:
Control voltage (V_{GG}) is adjusted at each frequency to maintain 1.2 W output power.

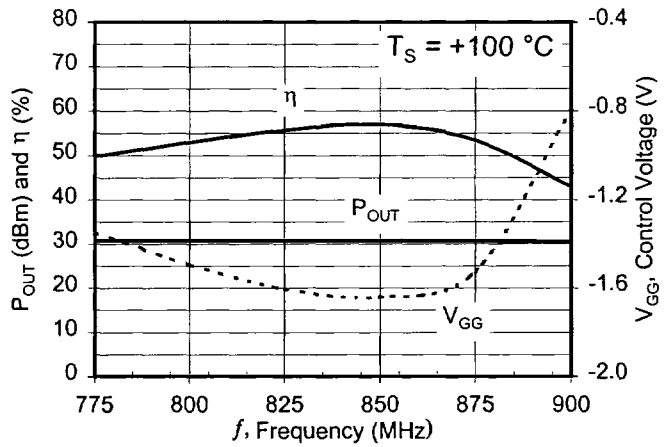


Figure 8. Output power, efficiency, and control voltage vs. frequency for T_S = +100°C

Conditions for Figure 8:
Control voltage (V_{GG}) is adjusted at each frequency to maintain 1.2 W output power.

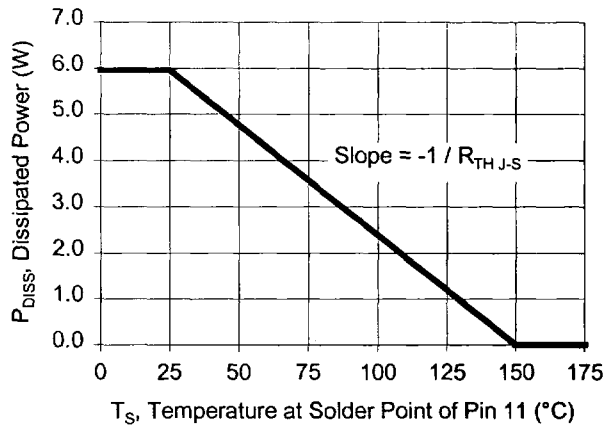


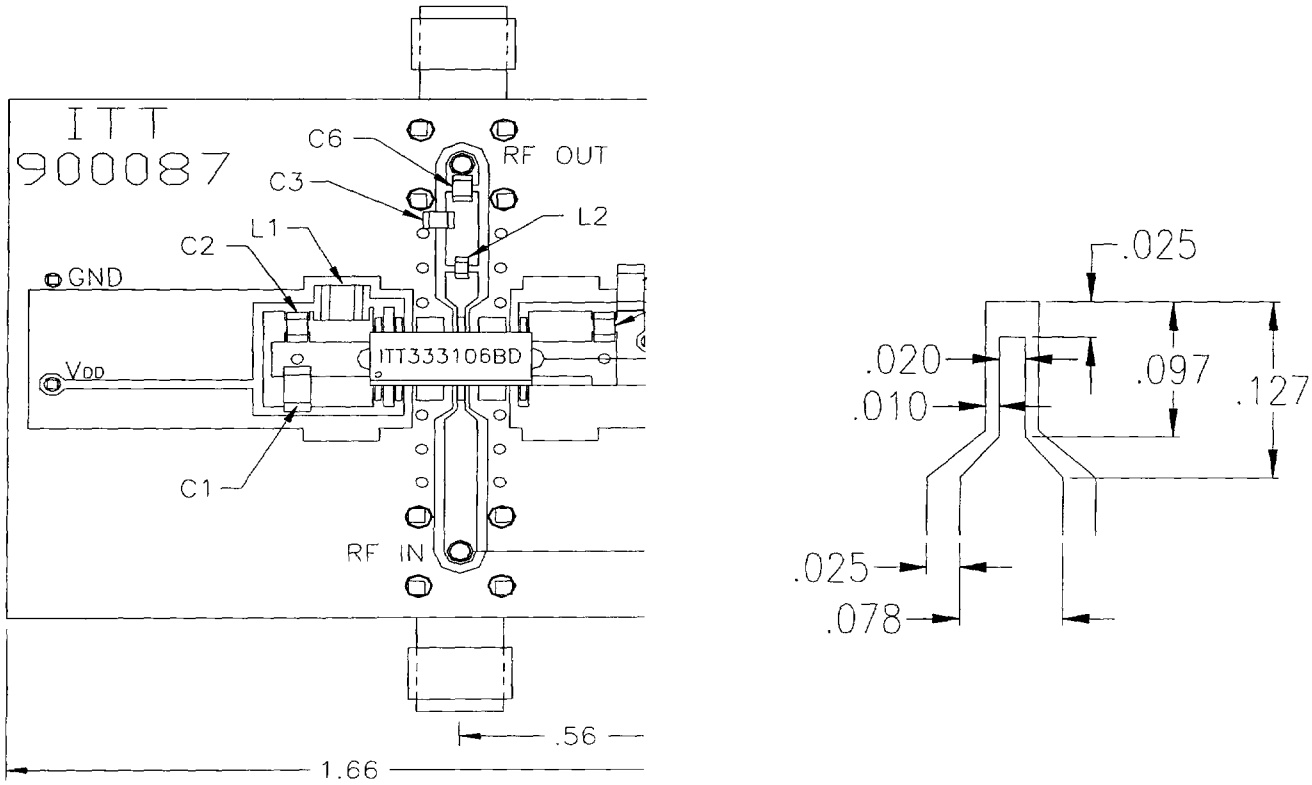
Figure 9. Maximum operating temperature chart

Conditions for Figure 9:

- $P_{DISS} = I_{DD2} * V_{DD} - P_{OUT}$, which refers to the dissipated power in the hottest area of the IC (Stage 2 FET). Stage 1 power dissipation and Stage 2 input power have negligible effect on IC maximum temperature located in Stage 2.
- I_{DD2} is typically 90% of I_{DD}.

GaAsTEK
A UNIT OF ITT INDUSTRIES
GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gaastek.com
Tel: 1-540-563-3949
1-888-563-3949 (USA)
Fax: 1-540-563-8616

MECHANICAL DATA



Top view **50Ω lead transition**

Figure 10. Component layout and printed circuit drawing for evaluation board

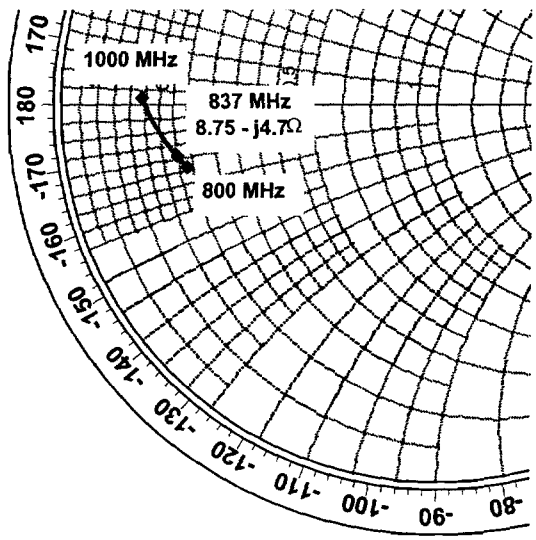


Figure 11. Output match impedance (as seen from pin 12)

GaAsTEK
A UNIT OF ITT INDUSTRIES
GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gaastek.com
Tel: 1-540-563-3949
1-888-563-3949 (USA)
Fax: 1-540-563-8616