Micro Power Systems

MP3306

CMOS
6-Bit High Speed
Analog-to-Digital Converter

FEATURES

- **Sampling Rates from 0.1 to 15 MHz (MSPS)**
- **Interface to any Input Range between GND and V_{DD}**
- **Monotonic; No Missing Codes**
- **Single Power Supply (4 to 6 volt)**
- **Low Power CMOS (100 mW typ.)**
- **ESD Protection: 2000 Volts Minimum**
- **Latch-Up Free**
- **SOIC Package**
- **Replacement for Harris CA3306**
- **Use MP7686 for Better Performance**

BENEFITS

- **High Conversion Speed at Low Power**
- **Most Flexible Input Range of any A/D Available**
- **No Sample/Hold Needed**
- **Easy Ping-Ponging for 30 MSPS System**

3

GENERAL DESCRIPTION

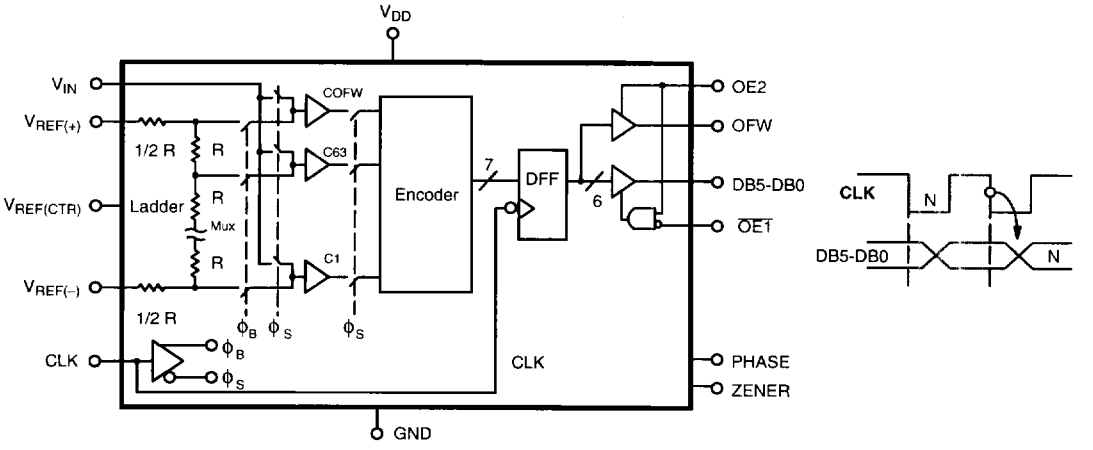
MP3306 is a 6-bit monolithic CMOS parallel flash A/D converter designed for precision 6-bit applications in video, scanning and data acquisition requiring conversion rates to 15 MHz. Differential Linearity error is less than 1/2 LSB at 10 MHz, and power consumption is 100 mW, typical.

The MP3306 has a unique input architecture which eliminates the need for an input track and hold and allows full scale input ranges from about 1 to 5 volts peak-to-peak, referred to ground or offset. The user simply sets $V_{REF(-)}$ and $V_{REF(+)}$ to encompass the desired input range.

MP3306 includes 64 auto-balanced clocked comparators, an encoder, 3-state output buffers, a reference resistor ladder, and associated timing circuitry. An overflow bit (or flag) has been provided to make it possible to achieve 7-bit resolution by connecting two devices in parallel. In normal operation this flag has no effect on the data bits.

Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP3306 is available in a Surface Mount (SOIC) package.

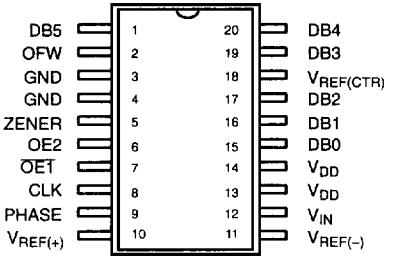
SIMPLIFIED BLOCK AND TIMING DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC	–40 to +85°C	MP3306JS	±1	±1
SOIC	–40 to +85°C	MP3306KS	±1/2	±1/2

PIN CONFIGURATIONS



20 Pin SOIC (0.300", Jedec)
S20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB5	Bit 5 Output (MSB)
2	OFW	Digital Output Overflow
3	GND	Ground
4	GND	Ground
5	ZENER	On Chip Zener Output
6	OE2	Output Enable Control
7	$\overline{OE1}$	Output Enable Control
8	CLK	Clock Input
9	PHASE	Sampling Clock Phase Control
10	$V_{REF(+)}$	Reference Voltage (+) Input

PIN NO.	NAME	DESCRIPTION
11	$V_{REF(-)}$	Reference Voltage (–) Input
12	V_{IN}	Analog Input
13	V_{DD}	Power Supply
14	V_{DD}	Power Supply
15	DB0	Bit 0 Output (LSB)
16	DB1	Bit 1 Output
17	DB2	Bit 2 Output
18	$V_{REF(CTR)}$	R Ladder Mid Point
19	DB3	Bit 3 Output
20	DB4	Bit 4 Output

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: V_{DD} = 5 V, F_S = 15 MHz (50% Duty Cycle), $V_{REF(+)}$ = 4.1, $V_{REF(-)}$ = GND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		6			6		Bits	
Sampling Rate	F_S	0.1		15.0	0.001	15.0	MHz	
ACCURACY (J Grade) (1)								
Differential Non-Linearity	DNL			±1		±2	LSB	
Integral Non-Linearity	INL			±1		±2	LSB	Best Fit Line
(Relative Accuracy)								(Max INL – Min INL) / 2
Zero Scale Error	EZS		±1.7				LSB	
Full Scale Error	EFS		±1.7				LSB	
ACCURACY (K Grade) (1)								
Differential Non-Linearity	DNL			±1/2		±1	LSB	
Integral Non-Linearity	INL			±1/2		±1	LSB	Best Fit Line
Zero Scale Error	EZS		±1.7				LSB	
Full Scale Error	EFS		±1.7				LSB	
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$			4.1			V	
Negative Ref. Voltage	$V_{REF(-)}$	GND			GND		V	
Differential Ref. Voltage (3)	V_{REF}	4.1		V_{DD}-GND		V_{DD}-GND	V	
Ladder Resistance	R_L	200		500	150	600	Ω	
Ladder Temp. Coefficient (2)	R_{TCO}					3000	ppm/°C	
ANALOG INPUT (2)								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Impedance	Z_{IN}		3				MΩ	
Input Capacitance Sample (5)	C_{INA}		30				pF	
Input Capacitance Convert (5)							pF	
Aperture Delay	t_{AP}		20				ns	
Aperture Uncertainty (Jitter)	t_{AJ}		220				ps	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.5			3.5		V	
Logical "0" Voltage	V_{IL}			0.4		0.4	V	
Leakage Currents								V_{IN}=GND to V_{DD}
CLK	I_{IN}	–1		1	–30	30	µA	
OE2		–1		1	–30	30	µA	
$\overline{OE1}$		–1		1	–30	30	µA	
Phase		–1		1	–30	30	µA	
Input Capacitance (2)	C_{IND}		5				pF	
Clock Timing (*See Figure 1.*)								
Clock Period	t_S	66					ns	
"High" Time	t_H	33					ns	
"Low" Time	t_L	33					ns	
Duty Cycle			50				%	

3

ELECTRICAL CHARACTERISTICS TABLE CONT'D

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS								
Logical "1" Voltage	V_{OH}	4.3			4.3		V	I_{LOAD} = −1.0 mA
Logical "0" Voltage	V_{OL}			0.6		0.6	V	I_{LOAD} = 2.0 mA
Tristate Leakage	I_{OZ}	±1			±20		µA	V_{OUT} = GND to V_{DD}
Data Valid Delay (2)	t_{DL}		66				ns	
Data Enable Delay (2)	t_{DEN}		20				ns	
Data Tristate Delay (2)	t_{DHZ}		26				ns	
Output Capacitance (2)	C_O		5				pF	
POWER SUPPLIES								
Operating Voltage	V_{DD}	4	5	6	4	6	V	
Current	I_{DD}		20	30		50	mA	

NOTES

(1) Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width ($V_{REF}/64$) is the DNL error. The INL error is the maximum distance (in LSB's) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (F_S).

(2) Guaranteed. Not tested.

(3) Specified values guarantee functionality. Refer to other parameters for accuracy.

(4) 3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.

(5) See V_{IN} input equivalent circuit. Switched capacitor analog input requires driver with low output resistance.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (1, 2) (T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... +7 V

$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND −0.5 to V_{DD} +0.5 V

V_{IN} ..... GND −0.5 to V_{DD} +0.5 V

Digital Inputs ..... GND −0.5 to V_{DD} +0.5 V

Digital Outputs ..... GND −0.5 to V_{DD} +0.5 V

Storage Temperature ..... −65°C to +150°C

Lead Temperature (Soldering 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

SOIC 900mW

Derates above 75°C ..... 12mW/°C

NOTES:

(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

(2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

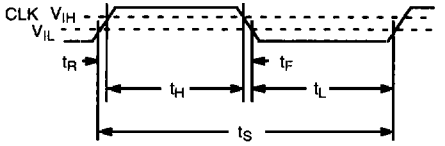


Figure 1. Clock Timing Specification

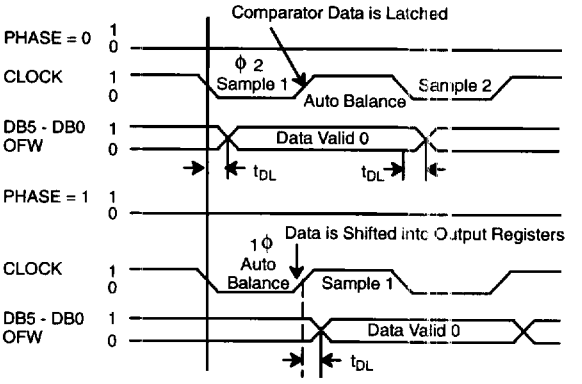


Figure 2. Data Line Enable Delay

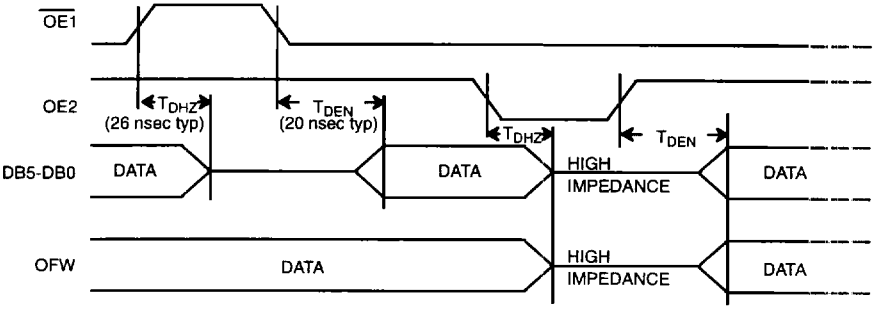


Figure 3. Output Enable and Disable Timing Diagram

$\overline{OE1}$	OE2	DB0 - DB5	OFW
0	1	Valid	Valid
1	1	Tri-State	Valid
X	0	Tri-State	Tri-State

Table 1. Truth Table