

PROTECTION PRODUCTS

Description

The SDC15 transient voltage suppressor (TVS) is designed to protect components which are connected to data and transmission lines from voltage surges caused by electrostatic discharge (**ESD**), electrical fast transients (**EFT**), and **lightning**.

TVS diodes are characterized by their high surge capability, low operating and clamping voltages, and fast response time. This makes them ideal for use as board level protection of sensitive semiconductor components. The dual-junction common-cathode design allows the user to protect one data or power line operating at ± 12 volts. The low profile SOT23 package allows flexibility in the design of "crowded" circuit boards.

The SDC15 TVS will meet the surge requirements of IEC 61000-4-2 (Formerly IEC 801-2), Level 4, "Human Body Model" for air and contact discharge.

Features

- ◆ 300 watts peak pulse power ($t_p = 8/20\mu s$)
- ◆ 40 watts peak pulse power ($t_p = 10/1000\mu s$)
- ◆ Transient protection for data and power lines to **IEC 61000-4-2 (ESD) $\pm 15kV$ (air), $\pm 8kV$ (contact)**
IEC 61000-4-4 (EFT) 40A (5/50ns)
IEC 61000-4-5 (Lightning) 12A (1.2/50 μs)
- ◆ Protects one bidirectional line
- ◆ Low clamping voltage
- ◆ Low leakage current
- ◆ High surge capability
- ◆ Solid-state silicon avalanche technology

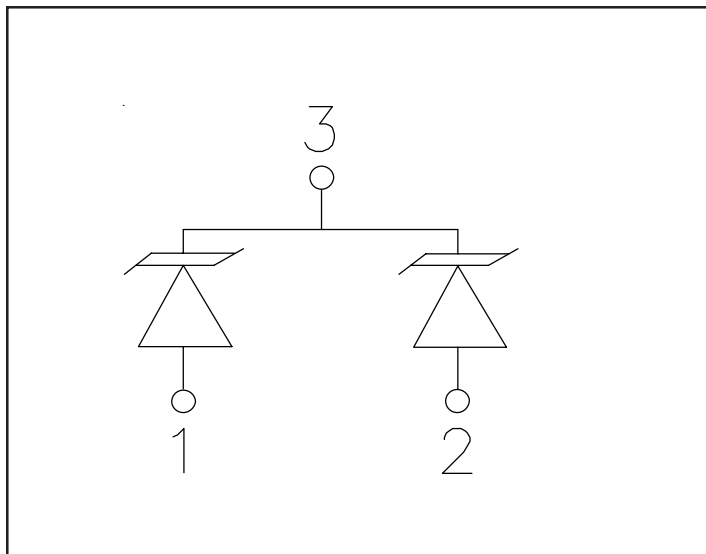
Mechanical Characteristics

- ◆ JEDEC SOT23 package
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : DC15
- ◆ Packaging : Tape and Reel per EIA 481

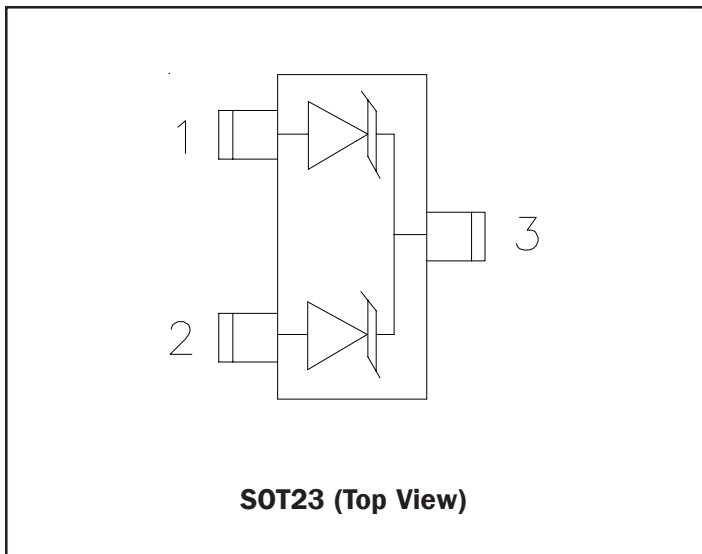
Applications

- ◆ RS-232 Data Lines
- ◆ Portable Electronics
- ◆ Industrial Controls
- ◆ Set-Top Box
- ◆ Servers, Notebook, and Desktop PC
- ◆ 12V DC Supply Protection

Circuit Diagram



Schematic & PIN Configuration



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Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{pk}	300	Watts
Peak Pulse Current ($t_p = 8/20\mu s$)	I_{pp}	10	A
Non-Repetitive Peak Forward Current ($t_p=100\mu s$)	I_{FSMAX}	4	A
Thermal Resistance, Junction to Ambient	θ_{JA}	556	$^{\circ}C/W$
Lead Soldering Temperature	T_L	260 (10 sec.)	$^{\circ}C$
Operating Temperature	T_J	-55 to +125	$^{\circ}C$
Storage Temperature	T_{STG}	-55 to +150	$^{\circ}C$

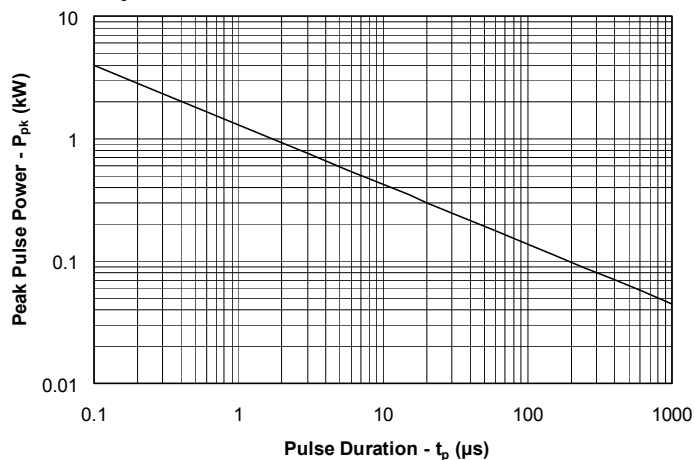
Electrical Characteristics

SDC15						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				12.8	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$, Between Pin 1 and 2 (each direction)	14.3		16.4	V
Reverse Leakage Current	I_R	$V_{RWM} = 12.8V$, $T=25^{\circ}C$ Between Pin 1 and 2 (each direction)			100	nA
Forward Voltage	V_F	$I_F = 100mA$, Pin 1 to 3 and Pin 2 to 3			1.3	V
Temperature Coefficient of VBR	αVBR				12	mV/ $^{\circ}C$
Clamping Voltage	V_C	$I_{pp} = 1.9A$, $t_p = 10/10000\mu s$ Between Pin 1 and 2 (each direction)			21.2	V
Junction Capacitance	C_J	$V_R = 0V$, $f = 1MHz$ Pin 1 to 2			120	pF

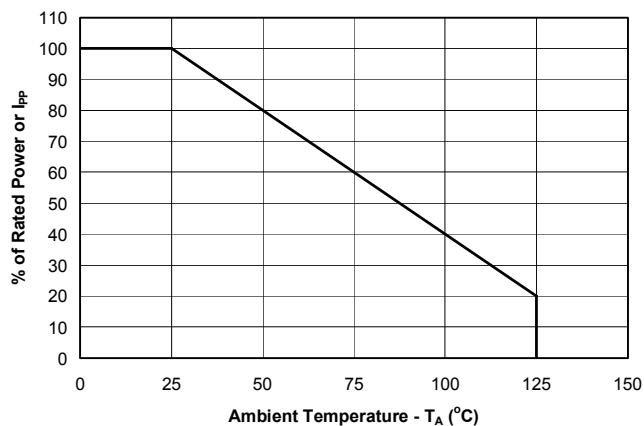
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Typical Characteristics

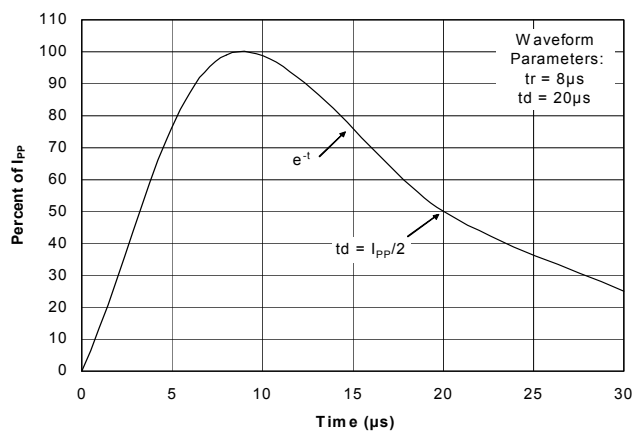
Non-Repetitive Peak Pulse Power vs. Pulse Time



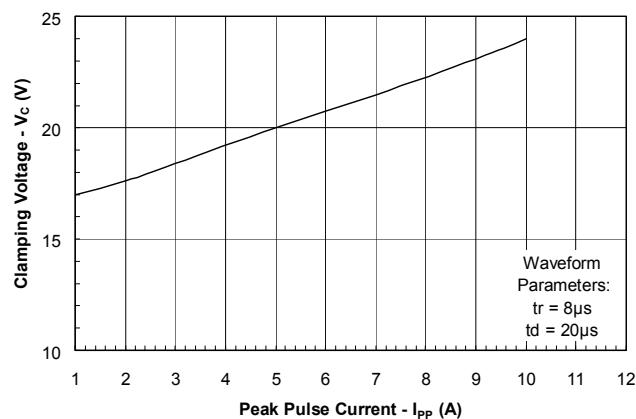
Power Derating Curve



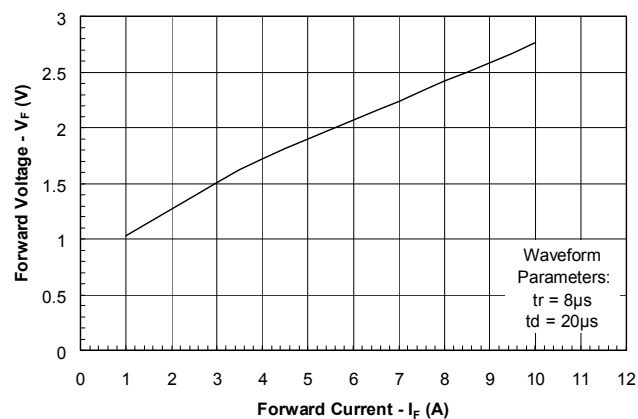
Pulse Waveform



Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



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Applications Information

Device Connection for Protection of One Data Line

The SDC15 is designed to protect one data or I/O line operating at ± 12 volts. Connection options are as follows:

- Common mode protection: Pin 1 is connected to the data line and pin 2 is connected to ground. For best results, this pin should be connected directly to a ground plane on the board. The path length should be kept as short as possible to minimize parasitic inductance. Pin 3 is not connected.
- Differential protection: Pin 1 is connected to one line and pin 2 is connected to the second line. Pin 3 is not connected.

Circuit Board Layout Recommendations for Suppression of ESD.

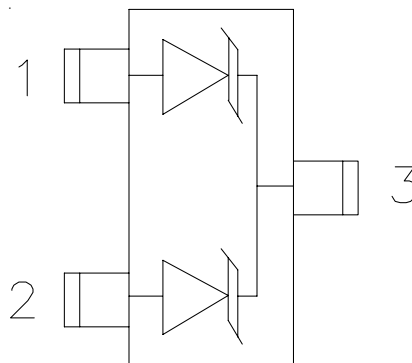
Good circuit board layout is critical for the suppression of fast rise-time transients such as ESD. The following guidelines are recommended:

- Place the SDC15 near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the SDC15 and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

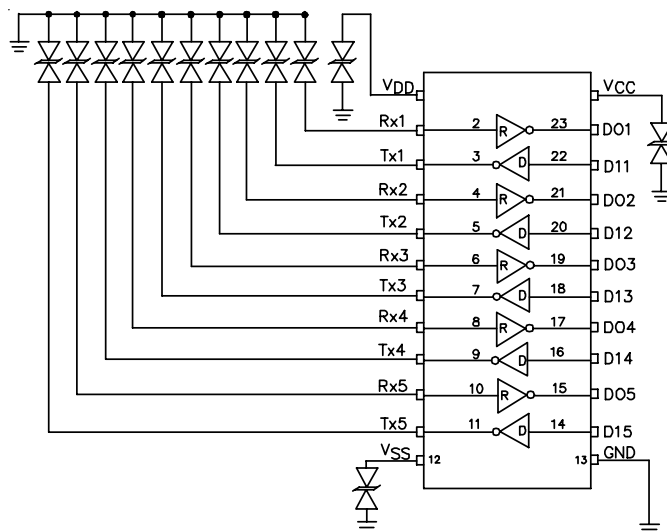
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Device Schematic and Pin Configuration

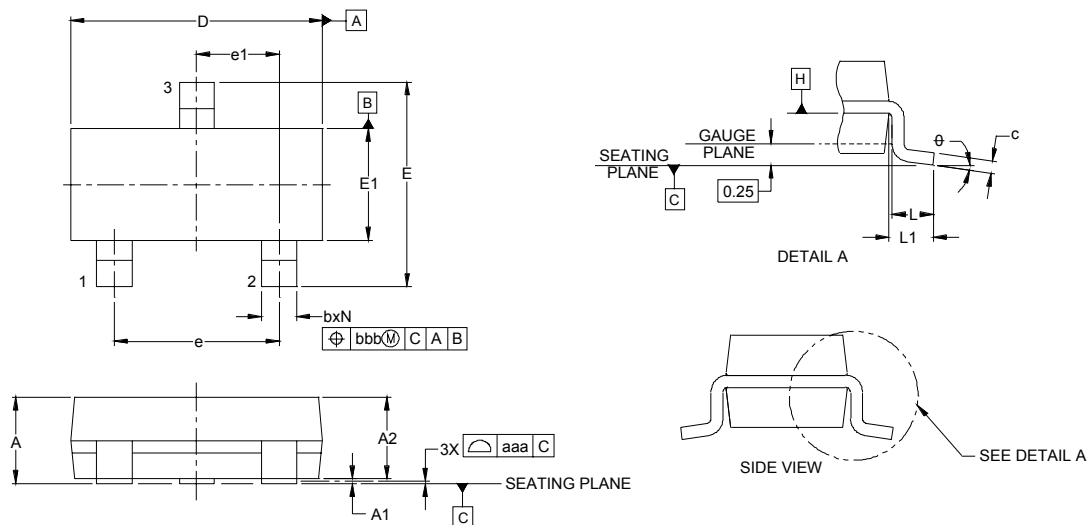


RS-232 Transceiver Protection Example



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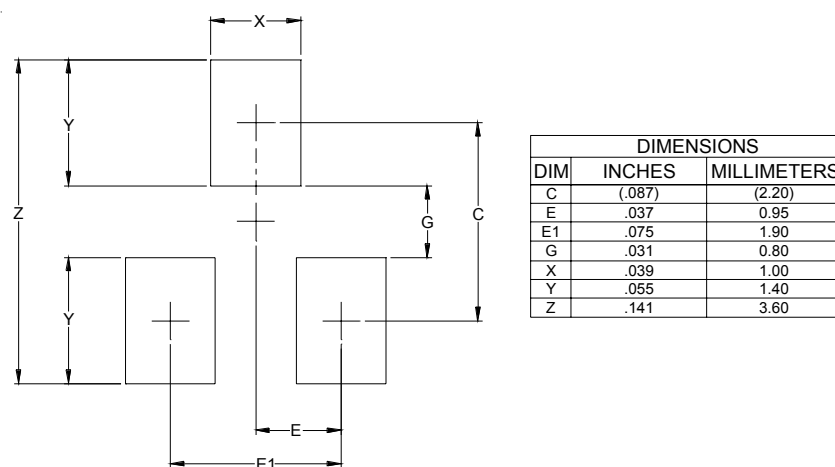
Outline Drawing - SOT23



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **A** AND **B** TO BE DETERMINED AT DATUM PLANE **H**.
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern - SOT23



NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A.

PROTECTION PRODUCTS**Ordering Information**

Part Number	Lead Finish	Qty per Reel	Reel Size
SDC15.TC	SnPb	3,000	7 Inch
SDC15.TCT	Pb Free	3,000	7 Inch

Contact Information for Semtech International AG

Taiwan Branch	Tel: 886-2-2748-3380 Fax: 886-2-2748-3390	Semtech Switzerland GmbH Japan Branch	Tel: 81-3-6408-0950 Fax: 81-3-6408-0951
Korea Branch	Tel: 82-2-527-4377 Fax: 82-2-527-4376	Semtech Limited (U.K.)	Tel: 44-1794-527-600 Fax: 44-1794-527-601
Shanghai Office	Tel: 86-21-6391-0830 Fax: 86-21-6391-0831	Semtech France SARL	Tel: 33-(0)169-28-22-00 Fax: 33-(0)169-28-12-98
Semtech International AG is a wholly-owned subsidiary of Semtech Corporation, which has its headquarters in the U.S.A.		Semtech Germany GmbH	Tel: 49-(0)8161-140-123 Fax: 49-(0)8161-140-124