DN74LS193

Synchronous 4-bit Binary Up / Down Dual Clock Counters (with Reset)

■ Description

DN74LS193 is a synchronous hexadecimal (4-bit binary) up/down counter with direct-coupled reset input and set input.

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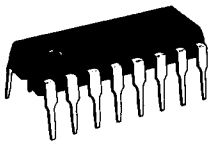
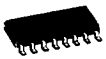


16-pin plastic DIL package

P-5

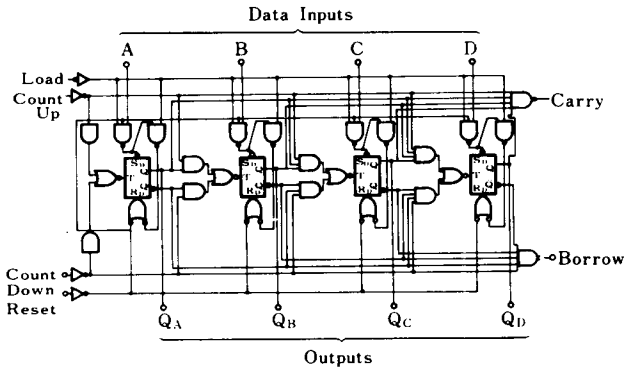


16-pin Panaflat package (SO-16D)

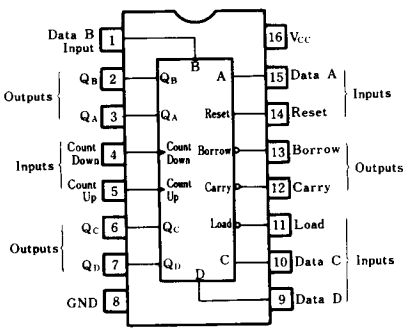
■ Features

- Exclusive clock input for up count and down count
- Asynchronous set input
- Direct-coupled reset input
- Easy cascade connection
- High-speed counting (f_{max} = 32MHz typical)
- Wide operating temperature range (Ta = −20 to +75°C)

■ Logic diagram



Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}			−400	μA
Output current	I_{OL}			8	mA
Operating temperature range	Topr	−20	25	75	℃
Clock frequency	fclock	0		25	MHz
Pulse width	t_W	20			ns
Set-up time (reset)	t_{su} (Reset)	20			ns
Set-up time	t_{su}	20			ns
Hold time	t_h	5			ns
Enable time	tenable	40			ns

■ DC characteristics (Ta = −20 ~ +75℃)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OH}	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −400μA		2.7	3.4		V
	V_{OL1}	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V	I_{OL} = 4mA		0.25	0.4	V
	V_{OL2}		I_{OL} = 8mA		0.35	0.5	V
Input current	I_{IH}	V_{CC} = 5.25V, V_I = 2.7V				20	μA
	I_{IL}	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
	I_I	V_{CC} = 5.25V, V_I = 7V				0.1	mA
Output short circuit current**	I_{OS}	V_{CC} = 5.25V, V_O = 0V		−15		−100	mA
Input clamp voltage	V_{IK}	V_{CC} = 4.75V, I_I = −18mA				−1.5	V
Supply current***	I_{CC}	V_{CC} = 5.25V			19	34	mA

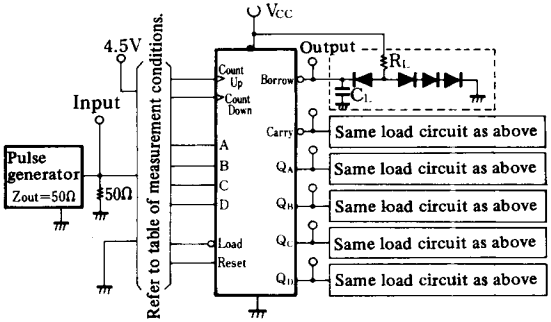
* When constant at V_{CC} = 5V, Ta = 25°C.
** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 sec.
*** Measured with all outputs open, reset and load inputs grounded, and 4.5V applied to all other inputs.

■ Switching characteristics (V_{CC} = 5V, Ta = 25℃)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}			C_L = 15pF, R_L = 2kΩ	25	32		MHz
Propagation delay time	t_{PLH}	Count Up	Carry			17	26	ns
	t_{PHL}					18	24	ns
	t_{PLH}	Count Down	Borrow			16	24	ns
	t_{PHL}					15	24	ns
	t_{PLH}	Either Count	Q			27	38	ns
	t_{PHL}					30	47	ns
	t_{PLH}	Load	Q			24	40	ns
	t_{PHL}					25	40	ns
	t_{PHL}	Reset	Q			23	35	ns

※ Switching parameter measurement information

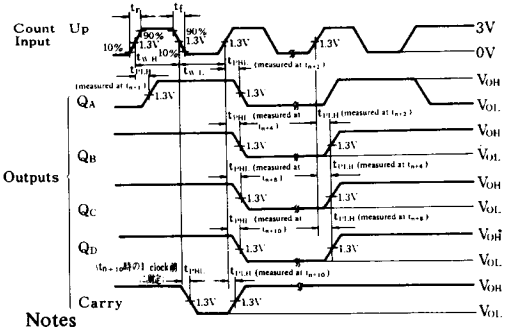
1. Measurement circuit



1. Number of pulse generators increased as needed.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

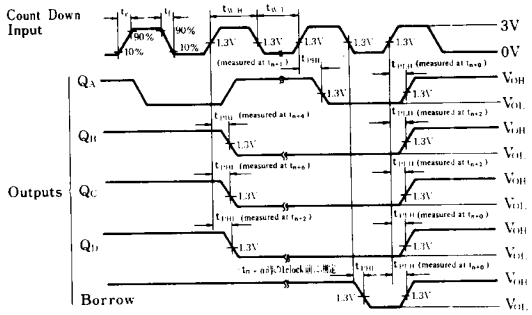
2. Waveforms

Waveforms-1 . f_{max}, t_{PLH}, t_{PHL} (Count Up時)



Notes
1. Input waveform: $t_r \leqq 15$ns, $t_f \leqq 5$ns, PRR = 1MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5$ns.
3. t_n is the bit time when all outputs are LOW.

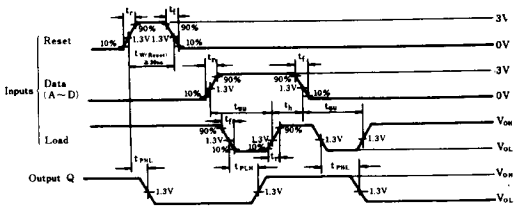
Waveforms-2 f_{max}, t_{PLH}, t_{PHL} (Count Down時)



Notes

1. Input waveform: $t_r \leqq 7$ ns, $t_f \leqq 7$ns, PRR = 1 MHz, duty cycle = 50%.
2. When measuring f_{max}, t_r and $t_f \leqq 2.5$ns.
3. t_n is the bit time when all outputs are HIGH.

Waveforms-3 t_{PLH}, t_{PHL} (Load, Reset → Q)



Notes

1. Input waveform: $t_r \leqq 7$ns, $t_f \leqq 7$ns

3. Table of measurement conditions

Parameter	Mode	Inputs					Outputs		
		Reset	Load	Count up	Count down	$D_A \sim D_D$	$Q_A \sim Q_D$	Carry	Borron
f_{max}	Count up	GND	4.5V	IN	4.5V	GND	OUT	OUT	
	Count down	GND	4.5V	4.5V	IN	GND	OUT		OUT
t_{PLH} t_{PHL}	Count up	GND	4.5V	IN	4.0V	GND	OUT	OUT	
	Count down	GND	4.5V	4.5V	N	GND	OUT		OUT
	Load	GND	IN	GND	GND	IN	OUT		
	Reset	IN	IN*	GND	GND	4.5V	OUT		

* Applied for initialization.

■ Input pulse conditions

t_W = min 20ns (Count up/Count down/Load/Reset)
t_S = min 20ns (Data to Load)
t_h = min 0ns (Data to Load)
t_r = min 40ns (Load/Reset to Count up/Count down)

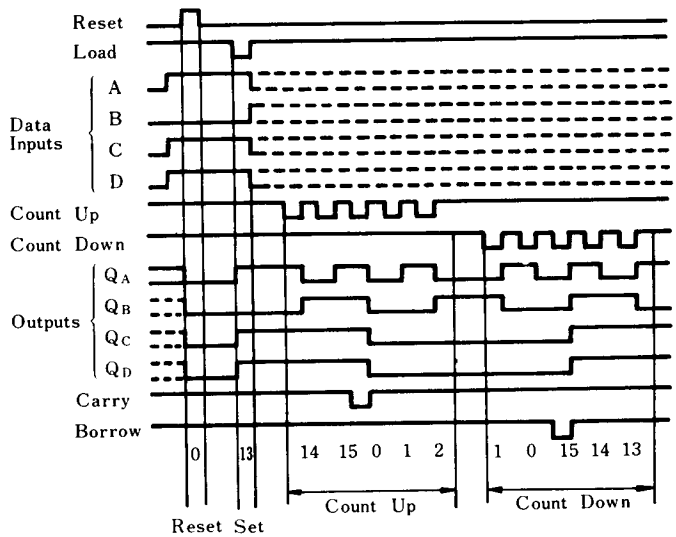
■ Truth tables

Operation mode	Inputs								Outputs					
	Reset	Lood	Count Up	Count Down	D_A	D_B	D_C	D_D	Q_A	Q_B	Q_C	Q_D	Carry	Borrow
Reset	H	×	×	L	×	×	×	×	L	L	L	L	H	L
	H	×	×	H	×	×	×	×	L	L	L	L	H	H
Load	L	L	×	L	L	L	L	L	L	L	L	L	H	L
	L	L	×	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	×	H	H	H	H	H	H	H	H	L	H
	L	L	H	×	H	H	H	H	H	H	H	H	H	H
Count up	L	H	↑	H	×	×	×	×	Count up				H [1]	H
Count down	L	H	H	↑	×	×	×	×	Count down				H	H [2]

1) Carry = Count up, $Q_A \cdot \overline{Q_B} \cdot \overline{Q_C} \cdot \overline{Q_D}$
2) Borrow = Count down, $\overline{Q_A} \cdot \overline{Q_B} \cdot \overline{Q_C} \cdot \overline{Q_D}$

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. ↑ : Change from LOW to HIGH.

■ Timing chart



Notes
1. Reset takes preference over load, data, and count inputs.
2. During the count up the count down input is HIGH, and during the count down the count up input is HIGH.