# WED3EL7216S, DDR SRAM, 2.5v CORE/ 2.5V IO  *Advanced\**

## FEATURES

- Core Supply Voltage = 2.5v +/- 0.2v
- IO Supply Voltage = 2.5v +/- 0.2v
- Bidirectional data strobe (DQS)
- Internal, pipelined, double data rate architecture
- Differential Clock Inputs
- Positive edge; Command execution
- DLL for alignment of DQ and DQS transitions
- Four internal banks for concurrent operation
- Data Mask (DM) for masking write data
- Programmable IOL/IOH
- Programmable Burst length: 2,4, or 8
- Auto Precharge option
- Auto Refresh and Self Refresh Modes

## GENERAL DESCRIPTION

The White Electronic Designs DDR SDRAM (x72/80) is a synchronous dynamic random-access memory supporting data transfer on each of the clock edges within a single cycle, and is configured internally as a quad bank architecture which supports concurrent operations.

The double data rate (DDR) architecture is referenced to as a 2n-pre-fetch architecture with an interface designed to transfer two data words per clock cycle. A single Read or Write access consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one half clock cycle data transfers at the I/O pins.

The WED3EL7216S devices contain differential clock inputs; the crossing of CK going through its voltage transition to a high true, and CK\ going through its voltage transition to a low true references a positive edge. Commands as well as Address(s) and Control(s) are registered on positive edges, Data is registered on both edges as well as Output Data is referenced on both edges of the Clock.

Read and Write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations, as defined by the programmable burst command.

## INITIALIZATION

DDR SDRAMs must be initialized via properly powering up. Operation and use of this device outside of established procedure(s) may result in undefined operation. Power must be first applied to Vcc and VccQ simultaneously and then Vref (and System Vtt) must be applied after VccQ in order to avoid device latch-up. Vref may be applied any time after VccQ but is normally expected at coincidence with Vtt. Except for CKE (clock enable) inputs are not recognized as valid until after Vref is applied. CKE is an SSTL_2 input but will detect an LVCMOS Low level after Vcc is applied. Maintaining an LVCMOS Low level on CLE during power-up is required to ensure that the DQ and DQS outputs will be in the HIGH-Z state where they will remain until driven in a normal READ operation. Once the POWER SUPPLY, and REFERENCE VOLTAGE is STABLE, the DDR SDRAM device requires 200us delay prior to execution of a COMMAND sequence. Once the 200us delay requirement has been meet, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a LOAD MODE REGISTER command is to be issued for the extended mode register (enabling the DLL) followed by another LOAD MODE REGISTER command to be issued to reset the DLL and program the operating parameters. Two hundred (200) clock cycles are required between the DLL reset and any READ command. A PRECHARGE ALL command should then be applied, placing the device in the all banks idle state.

Once in the Idle state, two AUTO REFRESH cycles must be performed. Additionally, a LOAD MODE REGISTER command for the mode register with the reset DLL bit deactivated is required. Following these requirements, the DDR SDRAM is ready for NORMAL OPERATION.

## PROGRAMMABLE IOH/IOL

The normal full drive strength for all outputs are specified to be SSTL class 2. The WED3EL7216 supports an option for reduced drive. This option is intended for the support of the lighter load and or point-to-point environments. The command and placement of this device into reduced drive mode will place the output drive at ~54% of the SSTL-2.

## DESELECT

The DESELECT command prevents new commands from being executed by the WED3EL7216S devices.

## NO OPERATION (NOP)

The NOP command is used to instruct the selected DDR SDRAM device to perform idle or wait states. During these states, the DDR SDRAM device is unable to register new commands, operations already in progress are not affected.

## LOAD MODE REGISTER

The MODE REGISTERS are loaded via inputs A0-A11. The LOAD MODE REGISTER command can only be issued when all DDR SDRAM internal banks are idle.

## ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, ant the address provided on inputs A0-A11 selects the row. The row remains active for accesses until a PRECHARGE command is issued. A PRECHARGE command must be issued before opening a different row in the same bank.

## READ

The READ command is used to initiate a BURST READ access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ax. Addressed location of the array will drive its contents onto the DQ's or the device
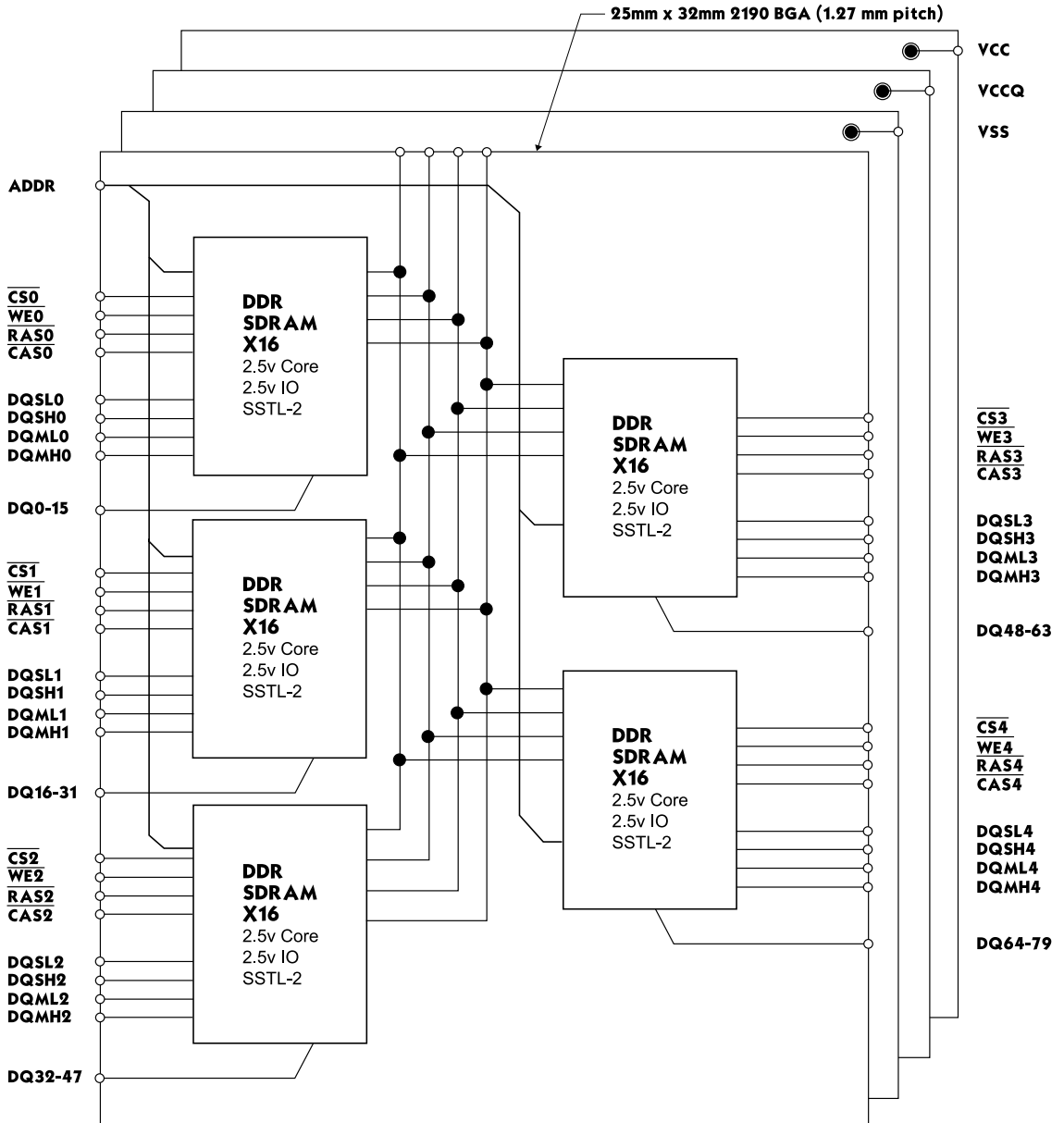
## WRITE

The WRITE command is used to initiate a burst write. Input data appearing on the DQ's will be written into the address location of the array.

## PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the PRECHARGE command is issued.

WHITE ELECTRONIC DESIGNS

## FUNCTIONAL BLOCK DIAGRAM

25mm x 32mm 2190 BGA (1.27 mm pitch)

VCC

VCCQ

VSS

ADDR

$\overline{CS0}$
$\overline{WE0}$
$\overline{RAS0}$
$\overline{CAS0}$

DQSL0
DQSH0
DQML0
DQMH0

DQ0-15

**DDR SDRAM X16**
2.5v Core
2.5v IO
SSTL-2

$\overline{CS1}$
$\overline{WE1}$
$\overline{RAS1}$
$\overline{CAS1}$

DQSL1
DQSH1
DQML1
DQMH1

DQ16-31

**DDR SDRAM X16**
2.5v Core
2.5v IO
SSTL-2

$\overline{CS2}$
$\overline{WE2}$
$\overline{RAS2}$
$\overline{CAS2}$

DQSL2
DQSH2
DQML2
DQMH2

DQ32-47

**DDR SDRAM X16**
2.5v Core
2.5v IO
SSTL-2

**DDR SDRAM X16**
2.5v Core
2.5v IO
SSTL-2

$\overline{CS3}$
$\overline{WE3}$
$\overline{RAS3}$
$\overline{CAS3}$

DQSL3
DQSH3
DQML3
DQMH3

DQ48-63

**DDR SDRAM X16**
2.5v Core
2.5v IO
SSTL-2

$\overline{CS4}$
$\overline{WE4}$
$\overline{RAS4}$
$\overline{CAS4}$

DQSL4
DQSH4
DQML4
DQMH4

DQ64-79

## PIN CONFIGURATION

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | | DQ0 | DQ14 | DQ15 | Vss | Vss | A9 | A10 | A11 | A8 | VccQ | VccQ | DQ16 | DQ17 | DQ31 | Vss |
| B | DQ1 | DQ2 | DQ12 | DQ13 | Vss | Vss | A0 | A7 | A6 | A1 | Vcc | Vcc | DQ18 | DQ19 | DQ29 | DQ30 |
| C | DQ3 | DQ4 | DQ10 | DQ11 | Vcc | Vcc | A2 | A5 | A4 | A3 | Vss | Vss | DQ20 | DQ21 | DQ27 | DQ28 |
| D | DQ6 | DQ5 | DQ8 | DQ9 | VccQ | VccQ | A12/NC | DNU | DNU | DNU | Vss | Vss | DQ22 | DQ23 | DQ26 | DQ25 |
| E | DQ7 | DQML0 | Vcc | DQMH0 | DQSH3 | DQSL0 | DQSH0 | BA0 | BA1 | DQSL1 | DQSH1 | VREF | DQML1 | Vss | NC | DQ24 |
| F | CAS0 | WE0 | Vcc | CLK0 | DQSL3 | | | | | | | RAS1 | WE1 | Vss | DQMH1 | CLK1 |
| G | CS0 | RAS0 | Vcc | CKE0 | CLK0 | | | | | | | CAS | CS1 | Vss | CLK | CKE1 |
| H | Vss | Vss | Vcc | VccQ | Vss | | | | | | | Vcc | Vss | Vss | VccQ | Vcc |
| J | Vss | Vss | Vcc | VccQ | Vss | | | | | | | Vcc | Vss | Vss | VccQ | Vcc |
| K | CLK3 | CKE3 | Vcc | CS3 | DQSL4 | | | | | | | CLK2 | CKE2 | Vss | RAS2 | CS2 |
| L | NC | CLK3 | Vcc | CAS3 | RAS3 | | | | | | | DQSL2 | CLK2 | Vss | WE2 | CAS2 |
| M | DQ56 | DQMH3 | Vcc | WE3 | DQML3 | CKE4 | DQMH4 | CLK4 | CAS4 | WE4 | RAS4 | CS4 | DQMH2 | Vss | DQML2 | DQ39 |
| N | DQ57 | DQ58 | DQ55 | DQ54 | DQSH4 | CLK4 | DQ73 | DQ72 | DQ71 | DQ70 | DQML4 | DQSH2 | DQ41 | DQ40 | DQ37 | DQ38 |
| P | DQ60 | DQ59 | DQ53 | DQ52 | Vss | Vss | DQ75 | DQ74 | DQ69 | DQ68 | Vcc | Vcc | DQ43 | DQ42 | DQ36 | DQ35 |
| R | DQ62 | DQ61 | DQ51 | DQ50 | Vcc | Vcc | DQ77 | DQ76 | DQ67 | DQ66 | Vss | Vss | DQ45 | DQ44 | DQ34 | DQ33 |
| T | Vss | DQ63 | DQ49 | DQ48 | VccQ | VccQ | DQ79 | DQ78 | DQ65 | DQ64 | Vss | Vss | DQ47 | DQ46 | DQ32 | Vcc |

## PIN DESCRIPTIONS

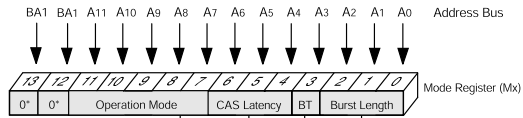| BGA LOCATIONS | SYMBOL | DESCRIPTION |
|---|---|---|
| F4, F16, G5, G15, K1, K12, L2, L13, N6, M8 | CKx, CKx\ | Clock: CKx and CKx\ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CKx and negative edge of CKx\. Output data (DQ's and DQS) is referenced to the crossings of the differential clock inputs |
| G4, G16, K2, K13 M6 | CKEx | Clock Enable: CKE controls the clock inputs. CKE high enables, CKE Low disables the clock input pins. Driving CKE Low pro-vides PRECHARGE POWER-DOWN and SELF REFRESH operations, or ACTIVE POWER-DOWN. CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry CKE is Asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers are disabled during POWER-DOWN Input buffers are disabled during SELF REFRESH. CKE is an SSTL-2 input but will detect an LVCMOS LOW level after VCC is applied |
| G1, G13, K4, K16 M12 | CSx\ | Chip Select: CSx\ enables the COMMAND register(s) of each of the five (5) contained words. All commands are masked when CSx\ is registered HIGH. CSx\ provides for external bank selection on systems with multiple banks. CSx\ is considered part of the COMMAND CODE. |
| F4, F16, G5, G15, K1, K12, L2, L13, N7, M9 | RASx\, CASx\ WEx\ | Command Inputs: RASx, CASx, and WEx\ define the command being entered |
| G4, G16, K2, K14 M7 | DQMLx, DQMHx | Input Data Mask. DM is an input mask signal for write data. Input data is masked when DQMLx or Hx is sampled HIGH at time of a WRITE access. DM is sampled on both edges of DQSLx and DQSHx |
| E8, E9 | BA0, BA1 | Bank Address Inputs: BA0, BA1 define which bank an ACTIVE READ, WRITE, or PRECHARGE command is being applied |
| A7, A8, A9, A10, B7 B8, B9, B10, C7, C8 C9, C10, D7 | A0-A11, A12 | Address Input : Provide the row address for Active commands, and the column address and auto precharge bit (A10) for READ/WRITE commands to select one location out of the memory array int the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank or all banks. The address inputs also provide the op-code during a MODE REGISTER SET command. |

## PIN DESCRIPTIONS

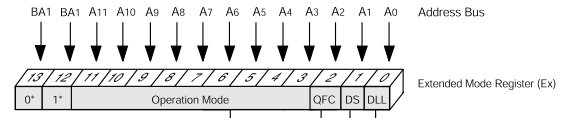| BGA LOCATIONS | SYMBOL | DESCRIPTION |
|---|---|---|
| A2, A3, A4, A13, A14 B1, B2, B3, B4, B13 B14, B15, B16, C1, C2,C3,C4,C13,C14, C15,C16,D1,D2,D3, D4,D13,D14,D15,D16 E1,E16,M1,M16,N1 N2,N3,N4,N13,N14, N15,N16,P1,P2,P3, P4,P13,P14,P15,P16 R1,R2,R3,R4,R13, R14,R15,R16,T2,T3, T4,T13,T14,T15,N7, N8,N9,N10,P7,P8,P9 P10,R7,R8,R9,R10 T7,T8,T9,T10 | DQ0-79 | Dat a I/O |
| E6, E7, E10, E11, F5, K5,L12,N5,N12,E5 | DQSLX, DQSHX | Data Strobe: Output with read data, input with write data. DQS is edge-aligned wit h read dat a, cent ered in writ e dat a. It is used to capture data. |
| B11,B12,C5,C6,E3, F3,G3,H3,H12,H16, J3,J12,J16,K3,L3,M3 P11,P12,R5,R6,T16 | VCC | Core Power Supply |
| A11,A12,D5,D6,H4, H15,J4,J15,T5,T6 | VCCQ | I/O Power Supply |
| A5,A6,A16,B5,B6, C11,C12,D11,D12, E14,F14,G14,H1,H2, H5,H13,H14,J1,J2,J5 J13,J14,K14,L14 P5,P6,R11,R12,T1, T11,T12, M14 | VSS | Ground (Digital) |
| E12 | VREF | SSTL-2 Reference Voltage |

# MODE REGISTER DEFINITION

Address Bus: BA1 BA1 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

Mode Register (Mx): 13 12 11 10 9 8 7 6 5 4 3 2 1 0

| 0* | 0* | Operation Mode | CAS Latency | BT | Burst Length |

|  | Burst Length | |
| --- | --- | --- |
| M2 M1 M0 | M3 = 0 | M3 = 1 |
| 0  0  0 | Reserved | Reserved |
| 0  0  1 | 2 | 2 |
| 0  1  0 | 4 | 4 |
| 0  1  1 | 8 | 8 |
| 1  0  0 | Reserved | Reserved |
| 1  0  1 | Reserved | Reserved |
| 1  1  0 | Reserved | Reserved |
| 1  1  1 | Reserved | Reserved |

| M3 | Burst Type |
| --- | --- |
| 0 | Sequential |
| 1 | Interleaved |

| M6 M5 M4 | CAS Latency |
| --- | --- |
| 0  0  0 | Reserved |
| 0  0  1 | Reserved |
| 0  1  0 | 2 |
| 0  1  1 | Reserved |
| 1  0  0 | Reserved |
| 1  0  1 | Reserved |
| 1  1  0 | 2.5 |
| 1  1  1 | Reserved |

| M11 | M10 | M9 | M8 | M7 | M6 - M0 | Operating Mode |
| --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | Valid | Normal Operation |
| 0 | 0 | 0 | 1 | 0 | Valid | Normal Operation / Reset DLL |
| - | - | - | - | - | - | All Other States Reserved |

# EXTENDED MODE REGISTER DEFINITION

Address Bus: BA1 BA1 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

Extended Mode Register (Ex): 13 12 11 10 9 8 7 6 5 4 3 2 1 0

| 0* | 1* | Operation Mode | QFC | DS | DLL |

| E0 | DLL |
| --- | --- |
| 0 | Enable |
| 1 | Disable |

| E1 | Drive Strength |
| --- | --- |
| 0 | Normal |
| 1 | Reduced |

| E1 | Drive Strength |
| --- | --- |
| 0 | Normal |
| 1 | Reduced |

| E11 | E10 | E9 | E8 | E7 | E6 | E5 | E4 | E3 | E2 - E0 | Operating Mode |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Valid | Normal Operation |
| - | - | - | - | - | - | - | - | - | - | All Other States Reserved |

## RECOMMENDED IO CONSIDERATION(S)
## X72 DESIGNS

DQ64
DQ65
DQ66
DQ67
DQ68      To System IO
DQ69
DQ70
DQ71

DQ72
DQ73
DQ74
DQ75
DQ76
DQ77
DQ78
DQ79

## X80 DESIGNS

DQ64
DQ65
DQ66
DQ67
DQ68      To System IO
DQ69
DQ70
DQ71

DQ72
DQ73
DQ74
DQ75      To System IO
DQ76
DQ77
DQ78
DQ79

WHITE ELECTRONIC DESIGNS

## MECHANICAL

# WHITE ELECTRONIC DESIGNS
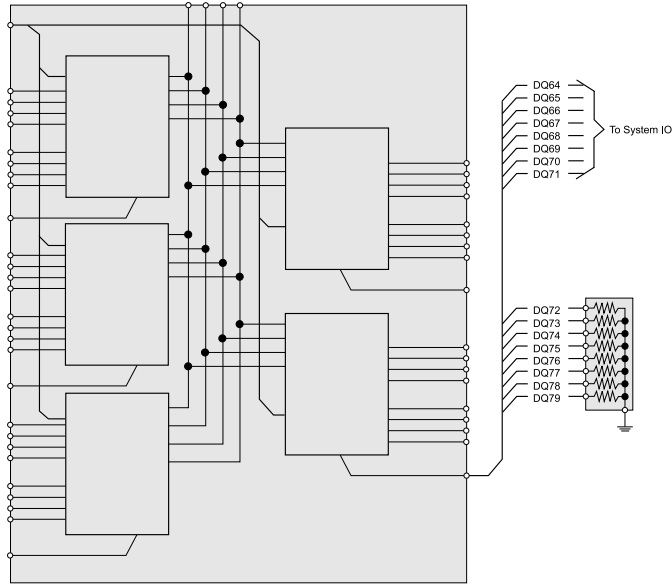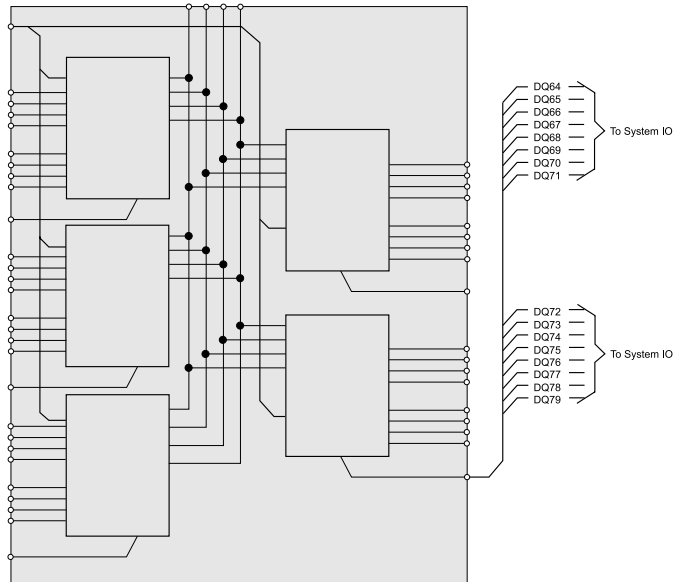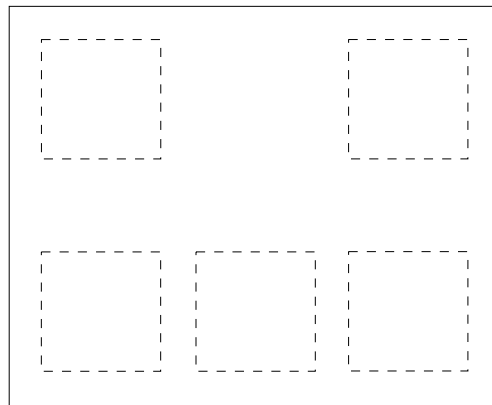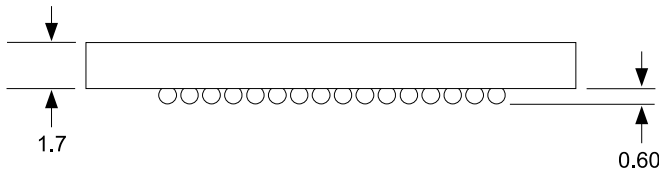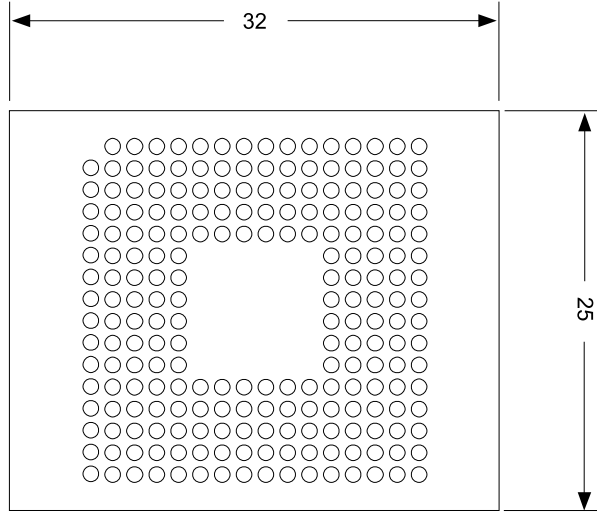
## POWER DISSIPATION PROJECTIONS

| DESCRIPTIONS | CONDITIONS | SYMBOL | TYP | MAX | | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|
| | | | | 7 | 75 | 8 | | |
| **Operating Supply Current** | All inputs Vil or Vih; Cycle time tKHKH (min) Outputs open | IDD | TBD | 800 | 825 | 775 | mA | 1 |
| **Standby Current** | tKHKH = tKHKH (min) Device in NOP state All Addresses / Data Static | ISB1 | TBD | 250 | 220 | 190 | mA | |

*Note(s): Power calculated with Outputs unloaded*

## CAPACITANCE

| DESCRIPTIONS | CONDITIONS | SYM | TYP | UNITS | NOTES |
|---|---|---|---|---|---|
| Address; A0-A21 | | Ca | 10 | pF | |
| Input/Output and IO Cntl: DQS, DQSLx, DQSHx DQMLx, DQMHx | TA = 25 C; f = 1Mhz | Cl,Co | 5 | pF | |
| Clocks; CLKx, CLKx\ | | Cck | 10 | pF | |
| Clock Enable(s): CKEx | | Ccnt. | 5 | pF | |

*Note(s): Power calculated with Outputs unloaded*

# AC ELECTRICAL CHARACTERISTICS

| Parameter | | Symbol | 7 | 7 | 75 | 75 | 8 | 8 |
|---|---|---|---|---|---|---|---|---|
| Access window of DQs from CLKx / CLKx\ | | tAC | -0.75 | 0.75 | -0.75 | 0.75 | -0.80 | 0.80 |
| CLKx high level width | | tCH | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 |
| CLKx low level width | CL=2.5 | tCL | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 |
| Clock Cycle Time | CL = 2 | tCK | 7.50 | 13.00 | 7.50 | 13.00 | 8.00 | 13.00 |
| | | tCK | 7.50 | 13.00 | 10.00 | 13.00 | 10.00 | 13.00 |
| DQ and DM input hold time relative to DQS | | tDH | 0.50 | | 0.50 | | 0.60 | |
| DQ and DM input setup time relative to DQS | | tDS | 0.50 | | 0.50 | | 0.60 | |
| DQ and DM input pulse width | | tDIPW | 1.75 | | 1.75 | | 2.00 | |
| Access window of DQS frm CLKx / CLKx\ | | tDQSCK | -0.75 | 0.75 | -0.75 | 0.75 | -0.80 | 0.80 |
| DQS input high pulse width | | tDQSH | 0.35 | | 0.35 | | 0.35 | |
| DQS input low pulse width | | tDQSL | 0.35 | | 0.35 | | 0.35 | |
| DQS-DQ skew, DQS to last DQ valid, per group, per access | | tDQSQ | | 0.50 | | 0.50 | | 0.60 |
| Wrtie command to first DQS latching transition | | tDQSS | 0.75 | 1.25 | 0.75 | 1.25 | 0.75 | 1.25 |
| DQS falling edge to CLKx rising - setup time | | tDSS | 0.20 | | 0.20 | | 0.20 | |
| DQS falling edge to CLKX rising - hold time | | tDSH | 0.20 | | 0.20 | | 0.20 | |
| Half clock period | | tHP | tCH,tCL | | tCH,tCL | | tCH,tCL | |
| Data-out high impedance window from CLK/CLK\ | | tHZ | | 0.75 | | 0.75 | | 0.80 |
| Data-out low impedance window from CLK/CLK\ | | tLZ | -0.75 | | -0.75 | | -0.80 | |
| Address and control input hold time | | tIH | 0.90 | | 0.90 | | 1.10 | |
| Address and control input setup time | | tIS | 1.00 | | 1.00 | | 1.10 | |
| Load Mode Register | | tMRD | 15.00 | | 15.00 | | 16.00 | |
| DQ-DQS hold, DQS to first DQ to go non-valid | | tQH | tHP - tQHS | | tHP - tQHS | | tHP - tQHS | |
| Data hold skew factor | | tQHS | | 0.75 | | 0.75 | | 1.00 |
| ACTIVE to PRECHARGE command | | tRAS | 40.00 | 120K | 40.00 | 120K | 40.00 | 120K |
| ACTIVE to READ with AUTO PRECHARGE command | | tRAP | | | tRAS (min) - (burst length x tCLK/e) | | | |
| ACTIVE to ACTIVE/AUTO REFRESH command period | | tRC | 65.00 | | 65.00 | | 70.00 | |
| AUTO REFRESH command period | | tRFC | 75.00 | | 75.00 | | 80.00 | |
| ACTIVE to READ or WRITE | | tRCD | 20.00 | | 20.00 | | 20.00 | |
| PRECHARGE command period | | tRP | 20.00 | | 20.00 | | 20.00 | |
| DQS read preamble | | tRPRE | 0.90 | 1.10 | 0.90 | 1.10 | 0.90 | 1.10 |
| DQS read postamble | | tRPST | 0.40 | 0.60 | 0.40 | 0.60 | 0.40 | 0.60 |
| ACTIVE bank to ACTIVE bank b command | | tRRD | 15.00 | | 15.00 | | 15.00 | |
| DQS write preamble | | tWPRE | 0.25 | | 0.25 | | 0.25 | |
| DQS write preamble setup time | | tWPRES | 0.00 | | 0.00 | | 0.00 | |
| Half clock period | | tWPST | 0.40 | 0.60 | 0.40 | 0.60 | 0.40 | 0.60 |
| Data-out high impedance window from CLK/CLK\ | | tWR | 15.00 | | 15.00 | | 15.00 | |
| Data-out low impedance window from CLK/CLK\ | | tREFC | | 140.60 | | 140.60 | | 140.60 |
| Address and control input hold time | | tXSNR | 75.00 | | 75.00 | | 80.00 | |
| Address and control input setup time | | tXSRD | 200.00 | | 200.00 | | 200.00 | |

## ORDERING INFORMATION

| PART NUMBER | CONFIGURATION | TECHNOLOGY | FREQUENCY | VCC | TEMP |
|---|---|---|---|---|---|
| WED3EL7216S7ES | 16M x 72 | SDRAM; DDR | 133/266 Mhz | 2.5 | ENG. SAMPLES |
| WED3EL7216S75ES | 16M x 72 | SDRAM; DDR | 133/266 Mhz | 2.5 | ENG. SAMPLES |
| WED3EL7216S8ES | 16M x 72 | SDRAM; DDR | 100/200 Mhz | 2.5 | ENG. SAMPLES |
| WED3EL7216S7BC | 16M x 72 | SDRAM; DDR | 133/266 Mhz | 2.5 | 0C - 70C |
| WED3EL7216S75BC | 16M x 72 | SDRAM; DDR | 133/266 Mhz | 2.5 | 0C - 70C |
| WED3EL7216S8BC | 16M x 72 | SDRAM; DDR | 100/200 Mhz | 2.5 | 0C - 70C |