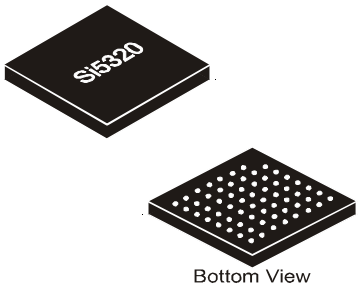
Si5320-XC3

SONET/SDH Precision Clock Multiplier IC

Features

- Ultra-low-jitter clock output with jitter generation as low as 0.3 ps_{rms}
- No external components (other than a resistor and standard bypassing)
- Input clock ranges at 19, 39, 78, 155, 311, and 622 MHz
- Digitally-controlled output phase adjust
- Output clock ranges at 19, 155, or 622 MHz
- Digital hold for loss of input clock
- Support for forward and reverse FEC clock scaling
- Selectable loop bandwidth
- Loss-of-signal alarm output
- Low power
- Small size (9x9 mm)



Ordering Information:

See page 36.

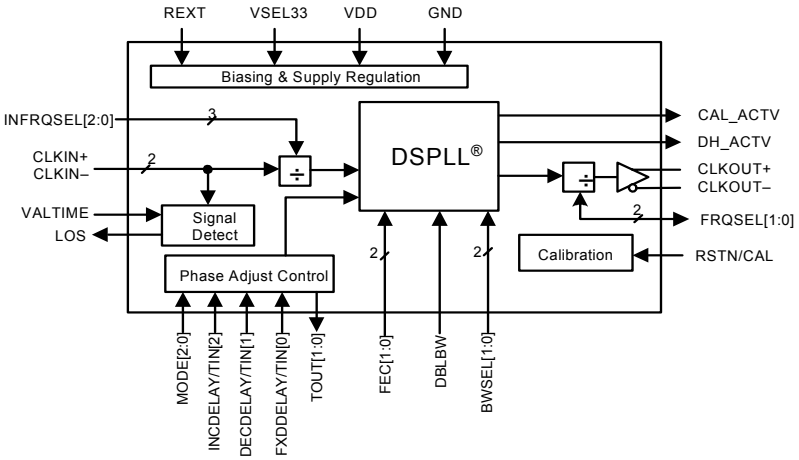
Applications

- SONET/SDH line/port cards
- Optical modules
- Core switches
- Digital cross connects
- Terabit routers

Description

The Si5320 is a precision clock multiplier designed to exceed the requirements of high-speed communication systems including OC-192/OC-48 and 10 GbE. This device phase locks to an input clock in the 19, 39, 78, 155, 311, or 622 MHz frequency range and generates a frequency-multiplied clock output that can be configured for operation in the 19, 155, or 622 MHz range. Silicon Laboratories' DSPLL® technology delivers all PLL functionality with unparalleled performance while eliminating external loop filter components, providing programmable loop parameters and simplifying design. FEC rates are supported with selectable 255/238 or 238/255 scaling of the clock multiplication ratios. The Si5320 establishes a new standard in performance and integration for ultra-low-jitter clock generation. It operates from a single 3.3 V supply.

Functional Block Diagram



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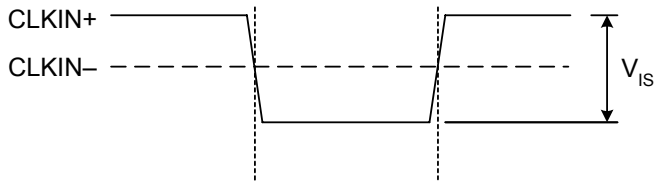
1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Ambient Temperature	T_A		–40[2]	25	85	°C
Si5320 Supply Voltage[3] When Using 3.3 V Supply	V_{DD33}		2.97	3.3	3.63	V

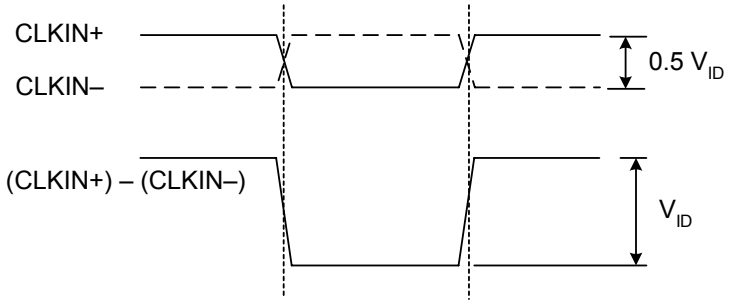
Notes:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. The Si5320 is guaranteed to operate and meet all electrical specifications over an ambient temperature of –40° to 85° C.
3. The Si5320 specifications are guaranteed when using the recommended application circuit (including component tolerance) shown in the "2. Typical Application Schematic (3.3 V Supply)" on page 17.



A. Operation with Single-Ended Clock Input

Note: When using single-ended clock sources, the unused clock input on the Si5320 must be ac-coupled to ground.



B. Operation with Differential Clock Input

Note: Transmission line termination, when required, must be provided externally.

Figure 1. CLKIN Voltage Characteristics

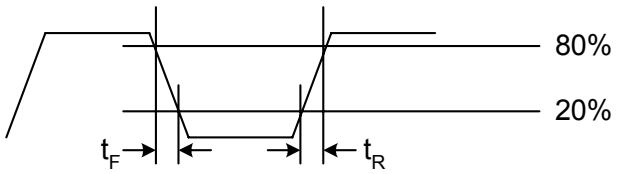


Figure 2. Rise/Fall Time Measurement

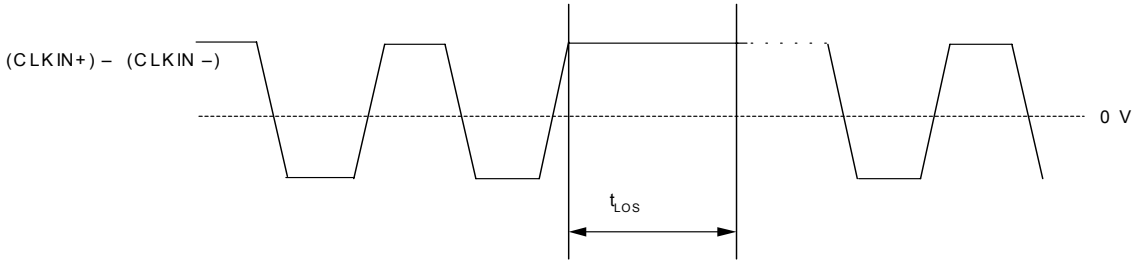


Figure 3. Transitionless Period on CLKIN for Detecting a LOS Condition

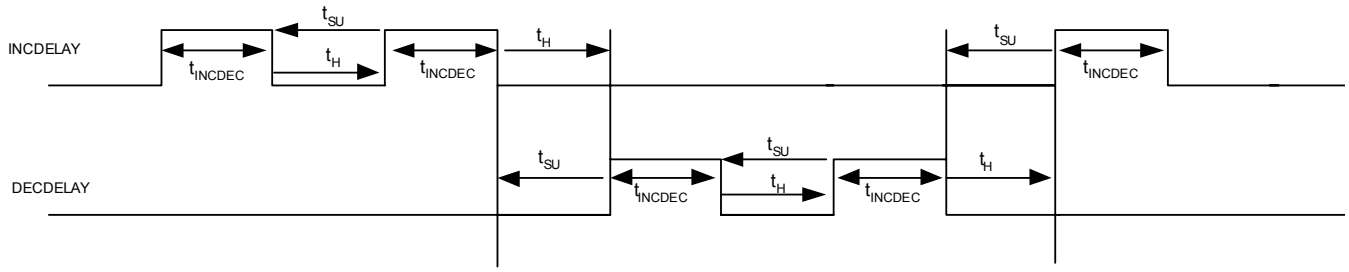


Figure 4. Output Phase Adjust Timing Diagrams (Pin Control)

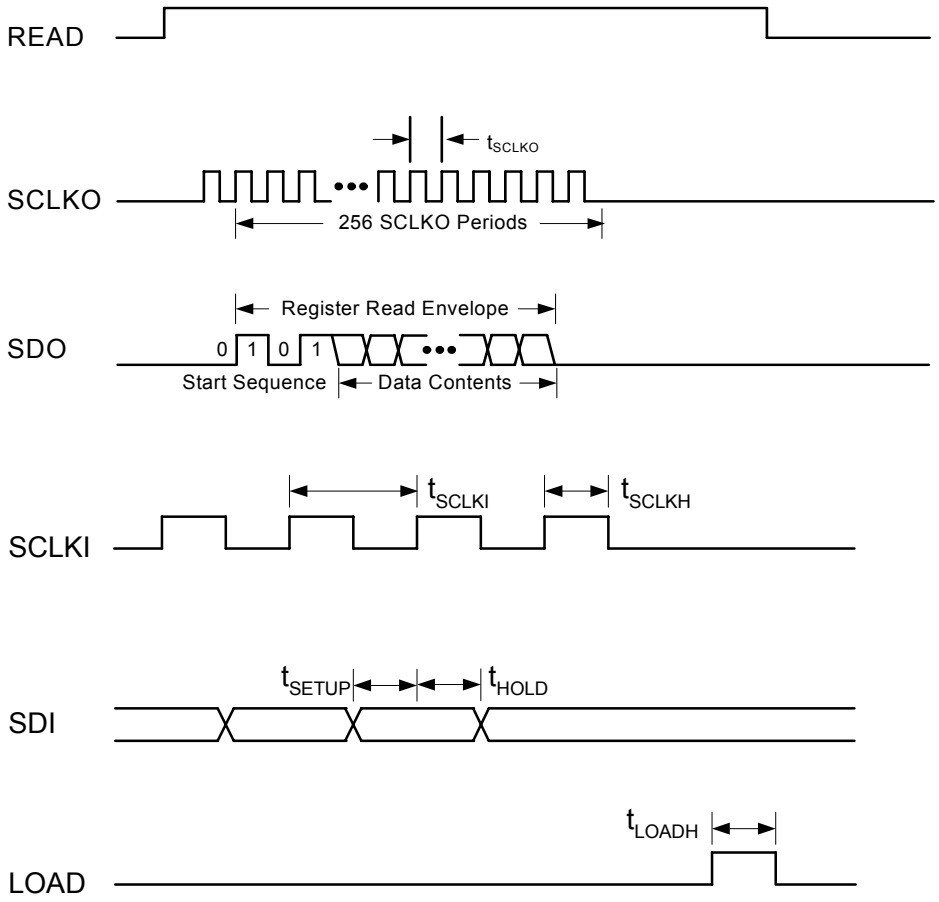


Figure 5. Output Phase Adjust Timing Diagrams (Register Control)

Table 2. DC Characteristics, V_{DD} = 3.3 V

(V_{DD33} = 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current 1	I_{DD}	Clock in = 622.08 MHz Clock out = 19.44 MHz	—	141	155	mA
Supply Current 2	I_{DD}	Clock in = 19.44 MHz Clock out = 622.08 MHz	—	135	145	mA
Power Dissipation Using 3.3 V Supply Clock Output	P_D	Clock in = 19.44 MHz Clock out = 622.08 MHz	—	445	479	mW
Common Mode Input Voltage[1,2,3] (CLKIN)	V_{ICM}		1.0	1.5	2.0	V
Single-Ended Input Voltage[2,3,4] (CLKIN)	V_{IS}	See Figure 1A	200	—	500[4]	mV_{PP}
Differential Input Voltage Swing[2,3,4] (CLKIN)	V_{ID}	See Figure 1B	200	—	500[4]	mV_{PP}
Input Impedance (CLKIN+, CLKIN–)	R_{IN}		—	80	—	kΩ
Differential Output Voltage Swing (CLKOUT)	V_{OD}	100 Ω Load Line-to-Line	816	906	1100	mV_{PP}
Output Common Mode Voltage (CLKOUT)	V_{OCM}	100 Ω Load Line-to-Line	1.4	1.8	2.2	V
Output Short to GND (CLKOUT)	$I_{SC(–)}$		–60	—	—	mA
Output Short to V_{DD25} (CLKOUT)	$I_{SC(+)}$		—	15	—	mA
Input Voltage Low (LVTTL Inputs)	V_{IL}		—	—	0.8	V
Input Voltage High (LVTTL Inputs)	V_{IH}		2.0	—	—	V
Input Low Current (LVTTL Inputs)	I_{IL}		—	—	50	µA
Input High Current (LVTTL Inputs)	I_{IH}		—	—	50	µA
Internal Pulldowns (All LVTTL Inputs)	I_{pd}		—	—	50	µA
Input Impedance (LVTTL Inputs)	R_{IN}		50	—	—	kΩ
Output Voltage Low (LVTTL Outputs)	V_{OL}	I_O = .5 mA	—	—	0.4	V
Output Voltage High (LVTTL Outputs)	V_{OH}	I_O = .5 mA	2.0	—	—	V

Notes:

1. The Si5320 device provides weak 1.5 V internal biasing that enables ac-coupled operation.
2. Clock inputs may be driven differentially or single-endedly. When driven single-endedly, the unused input should be ac-coupled to ground.
3. Transmission line termination, when required, must be provided externally.
4. Although the Si5320 device can operate with input clock swings as high as 1500 mV_{PP}, Silicon Laboratories recommends maintaining the input clock amplitude below 500 mV_{PP} for optimal performance.

Table 3. AC Characteristics
(V_{DD33} = 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Clock Frequency (CLKIN) FEC[1:0] = 00 (non FEC)	f_{CLKIN}	No FEC Scaling				
INFRQSEL[2:0] = 001			19.436	—	21.685	MHz
INFRQSEL[2:0] = 010			38.872	—	43.369	
INFRQSEL[2:0] = 011			77.744	—	86.738	
INFRQSEL[2:0] = 100			155.48	—	173.48	
INFRQSEL[2:0] = 101			310.97	—	346.95	
INFRQSEL[2:0] = 110			621.95	—	693.90	
Input Clock Frequency (CLKIN) FEC[1:0] = 01 (forward FEC)	f_{CLKIN}	255/238 FEC Scaling				
INFRQSEL[2:0] = 001			18.142	—	20.239	MHz
INFRQSEL[2:0] = 010			36.284	—	40.478	
INFRQSEL[2:0] = 011			72.568	—	80.955	
INFRQSEL[2:0] = 100			145.13	—	161.91	
INFRQSEL[2:0] = 101			290.27	—	323.82	
INFRQSEL[2:0] = 110			580.54	—	647.64	
Input Clock Frequency (CLKIN) FEC[1:0] = 10 (reverse FEC)	f_{CLKIN}	238/255 FEC Scaling				
INFRQSEL[2:0] = 001			20.826	—	23.234	MHz
INFRQSEL[2:0] = 010			41.652	—	46.465	
INFRQSEL[2:0] = 011			83.305	—	92.934	
INFRQSEL[2:0] = 100			166.61	—	185.87	
INFRQSEL[2:0] = 101			333.22	—	371.74	
INFRQSEL[2:0] = 110			666.44	—	743.47	
Input Clock Rise Time (CLKIN)	t_R	Figure 2	—	—	11	ns
Input Clock Fall Time (CLKIN)	t_F	Figure 2	—	—	11	ns
Input Clock Duty Cycle	C_{DUTY_IN}		40	50	60	%
CLKOUT Frequency Range* FRQSEL[1:0] = 00 (no output)			—	—	—	
FRQSEL[1:0] = 01	f_{O_19}		19.436	—	21.685	MHz
FRQSEL[1:0] = 10	f_{O_155}		155.48	—	173.48	
FRQSEL[1:0] = 11	f_{O_622}		621.95	—	693.90	
CLKOUT Rise Time	t_R	Figure 2; single-ended; after 3 cm of 50 Ω FR4 stripline	—	213	260	ps
CLKOUT Fall Time	t_F	Figure 2; single-ended; after 3 cm of 50 Ω FR4 stripline	—	191	260	ps
Output Clock Duty Cycle	C_{DUTY_OUT}	Differential: (CLKOUT+) – (CLKOUT–)	48	—	52	%

***Note:** The Si5320 provides a 1/32, 1/16, 1/8, 1/4, 1/2, 1, 2, 4, 8, 16, or 32x clock frequency multiplication function with an option for additional frequency scaling by a factor of 255/238 or 238/255 for FEC rate compatibility.

Table 3. AC Characteristics (Continued)
(V_{DD33} = 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RSTN/CAL Pulse Width	t_{RSTN}		20	—	—	ns
Transitionless Period Required on CLKIN for Detecting a LOS Condition. INFRQSEL[2:0] = 001 INFRQSEL[2:0] = 010 INFRQSEL[2:0] = 011 INFRQSEL[2:0] = 100 INFRQSEL[2:0] = 101 INFRQSEL[2:0] = 110	t_{LOS}	Figure 3	 $^{24}/_{fo\_622}$ $^{16}/_{fo\_622}$ $^{12}/_{fo\_622}$ $^{10}/_{fo\_622}$ $^{9}/_{fo\_622}$ $^{9}/_{fo\_622}$	 — — — — — —	 $^{32}/_{fo\_622}$ $^{32}/_{fo\_622}$ $^{32}/_{fo\_622}$ $^{32}/_{fo\_622}$ $^{32}/_{fo\_622}$ $^{32}/_{fo\_622}$	s
Recovery Time for Clearing an LOS Condition VALTIME = 0 VALTIME = 1	t_{VAL}	Measured from when a valid reference clock is applied until the LOS flag clears	 0.09 12.0	 — —	 0.22 14.1	s
INCDELAY/DECDELAY Pulse Width	t_{INCDEC}	Figure 4	1	—	—	µs
INCDELAY/DECDELAY Setup Time	t_{SU}	Figure 4	1	—	—	µs
INCDELAY/DECDELAY Hold Time	t_H	Figure 4	1	—	—	µs
Register Read Out READ Clock High	t_{READH}		1	—	—	µs
Register Read Out Serial Clock (SCLKO) Frequency	$1/t_{SCLKO}$		—	—	4.86	MHz
Register Read Out Clock High to Output Valid	t_{CHOV}		10	—	—	ns
Output Phase INC/DEC Serial Clock (SCLKI) Frequency	$1/t_{SCLKI}$		—	—	1.5	MHz
Output Phase INC/DEC Serial Clock (SCLKI) Clock High	t_{SCLKH}		300	—	—	ns
Output Phase INC/DEC Serial Data (SDI) Setup Time	t_{SETUP}		300	—	—	ns
Output Phase INC/DEC Serial Data (SDI) Hold Time	t_{HOLD}		300	—	—	ns
Output Phase INC/DEC Parallel Load (LOAD) Clock High	t_{LOADH}		300	—	—	ns

***Note:** The Si5320 provides a 1/32, 1/16, 1/8, 1/4, 1/2, 1, 2, 4, 8, 16, or 32x clock frequency multiplication function with an option for additional frequency scaling by a factor of 255/238 or 238/255 for FEC rate compatibility.

Table 3. AC Characteristics (Continued)
(V_{DD33} = 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Phase INC/DEC Coarse Adjust Delay Increment/ Decrement (f_{O_622} = 622.08 MHz)	t_{CDELAY}		—	$2/f_{0\_622}$	—	ns
Output Phase INC/DEC Fine Adjust Delay Increment/Decrement	t_{FDELAY}		—	$1/16 \times f_{0\_622}$	—	ps
***Note:** The Si5320 provides a 1/32, 1/16, 1/8, 1/4, 1/2, 1, 2, 4, 8, 16, or 32x clock frequency multiplication function with an option for additional frequency scaling by a factor of 255/238 or 238/255 for FEC rate compatibility.						

Table 4. AC Characteristics (PLL Performance Characteristics)
(V_{DD33} = 3.3 V ±10%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wander/Jitter at 800 Hz Bandwidth (BWSEL[1:0] = 10 and DBLBW = 0)						
Jitter Tolerance (see Figure 8)	$J_{TOL(PP)}$	f = 8 Hz	1000	—	—	ns
		f = 80 Hz	100	—	—	ns
		f = 800 Hz	10	—	—	ns
CLKOUT RMS Jitter Generation FEC[1:0] = 00	$J_{GEN(rms)}$	12 kHz to 20 MHz	—	0.87	1.2	ps
		50 kHz to 80 MHz	—	0.26	0.35	ps
CLKOUT RMS Jitter Generation FEC[1:0 = 01, 10	$J_{GEN(rms)}$	12 kHz to 20 MHz	—	0.85	1.2	ps
		50 kHz to 80 MHz	—	0.26	0.35	ps
CLKOUT Peak-Peak Jitter Generation FEC[1:0 = 00	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	7.3	10.0	ps
		50 kHz to 80 MHz	—	3.7	5.0	ps
CLKOUT Peak-Peak Jitter Generation FEC[1:0 = 01, 10	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	7.2	10.0	ps
		50 kHz to 80 MHz	—	3.8	5.0	ps
Jitter Transfer Bandwidth (see Figure 7)	F_{BW}	BW = 800 Hz	—	800	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 800 Hz	—	0.0	0.05	dB

Notes:
1. Higher PLL bandwidth settings provide smaller clock output wander with temperature gradient.
2. For reliable device operation, temperature gradients should be limited to 10 °C/min.
3. Telcordia GR-1244-CORE requirements specify maximum phase transient slope during clock rearrangement in terms of nanoseconds per millisecond. The equivalent ps/μs unit is used here since the maximum phase transient magnitude for the Si5320 (tPT_MTIE) never reaches one nanosecond.

Table 4. AC Characteristics (PLL Performance Characteristics) (Continued)
(V_{DD33} = 3.3 V ±10%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wander/Jitter at 1600 Hz Bandwidth (BWSEL[1:0] = 10 and DBLBW = 1)						
Jitter Tolerance (see Figure 8)		f = 16 Hz	500	—	—	ns
		f = 160 Hz	50	—	—	ns
		f = 1600 Hz	5	—	—	ns
CLKOUT RMS Jitter Generation FEC[1:0] = 00	$J_{GEN(rms)}$	12 kHz to 20 MHz	—	0.78	1.2	ps
		50 kHz to 80 MHz	—	0.25	0.35	ps
CLKOUT Peak-Peak Jitter Generation FEC[1:0] = 00	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	7.0	9.0	ps
		50 kHz to 80 MHz	—	3.8	5.0	ps
Jitter Transfer Bandwidth (see Figure 7)	F_{BW}	BW = 1600 Hz	—	1600	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 1600 Hz	—	0.00	0.05	dB
Wander/Jitter at 1600 Hz Bandwidth (BWSEL[1:0] = 01 and DBLBW = 0)						
Jitter Tolerance (see Figure 8)	$J_{TOL(PP)}$	f = 16 Hz	1000	—	—	ns
		f = 160 Hz	100	—	—	ns
		f = 1600 Hz	10	—	—	ns
CLKOUT RMS Jitter Generation FEC[1:0] = 00	$J_{GEN(RMS)}$	12 kHz to 20 MHz	—	0.82	1.0	ps
		50 kHz to 80 MHz	—	0.26	0.35	ps
CLKOUT RMS Jitter Generation FEC[1:0] = 01, 10	$J_{GEN(RMS)}$	12 kHz to 20 MHz	—	0.79	1.0	ps
		50 kHz to 80 MHz	—	0.26	0.35	ps
CLKOUT Peak-Peak Jitter Generation FEC[1:0] = 00	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	7.3	10.0	ps
		50 kHz to 80 MHz	—	3.8	5.0	ps
CLKOUT Peak-Peak Jitter Generation FEC[1:0] = 01, 10	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	7.1	10.0	ps
		50 kHz to 80 MHz	—	4.3	5.0	ps
Jitter Transfer Bandwidth (see Figure 11)	F_{BW}	BW = 1600 Hz	—	1600	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 1600 Hz	—	0.0	0.1	dB

Notes:
1. Higher PLL bandwidth settings provide smaller clock output wander with temperature gradient.
2. For reliable device operation, temperature gradients should be limited to 10 °C/min.
3. Telcordia GR-1244-CORE requirements specify maximum phase transient slope during clock rearrangement in terms of nanoseconds per millisecond. The equivalent ps/μs unit is used here since the maximum phase transient magnitude for the Si5320 (tPT_MTIE) never reaches one nanosecond.

Table 4. AC Characteristics (PLL Performance Characteristics) (Continued)
(V_{DD33} = 3.3 V ±10%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wander/Jitter at 3200 Hz Bandwidth (BWSEL[1:0] = 01 and DBLBW = 1)						
Jitter Tolerance (see Figure 8)		f = 32 Hz	500	—	—	ns
		f = 320 Hz	50	—	—	ns
		f = 3200 Hz	5	—	—	ns
CLKOUT RMS Jitter Generation FEC[1:0] = 00	$J_{GEN(RMS)}$	12 kHz to 20 MHz	—	0.72	0.9	ps
		50 kHz to 80 MHz	—	0.24	0.3	ps
CLKOUT Peak-Peak Jitter Generation FEC[1:0] = 00	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	6.8	10.0	ps
		50 kHz to 80 MHz	—	3.7	5.0	ps
Jitter Transfer Bandwidth (see Figure 7)	F_{BW}	BW = 3200 Hz	—	3200	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 3200 Hz	—	0.05	0.1	dB
Wander/Jitter at 3200 Hz Bandwidth (BWSEL[1:0] = 00 and DBLBW = 0)						
Jitter Tolerance (see Figure 8)	$J_{TOL(PP)}$	f = 32 Hz	1000	—	—	ns
		f = 320 Hz	100	—	—	ns
		f = 3200 Hz	10	—	—	ns
CLKOUT RMS Jitter Generation FEC[1:0] = 00	$J_{GEN(rms)}$	12 kHz to 20 MHz	—	0.86	1.2	ps
		50 kHz to 80 MHz	—	0.29	0.4	ps
CLKOUT RMS Jitter Generation FEC[1:0] = 01, 10	$J_{GEN(rms)}$	12 kHz to 20 MHz	—	0.79	1.2	ps
		50 kHz to 80 MHz	—	0.28	0.4	ps
CLKOUT Peak-Peak Jitter Generation FEC[1:0] = 00	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	7.7	10.0	ps
		50 kHz to 80 MHz	—	3.9	5.0	ps
CLKOUT Peak-Peak Jitter Generation FEC[1:0] = 01, 10	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	7.2	10.0	ps
		50 kHz to 80 MHz	—	4.0	5.0	ps
Jitter Transfer Bandwidth (see Figure 7)	F_{BW}	BW = 3200 Hz	—	3200	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 3200 Hz	—	0.05	0.1	dB

Notes:
1. Higher PLL bandwidth settings provide smaller clock output wander with temperature gradient.
2. For reliable device operation, temperature gradients should be limited to 10 °C/min.
3. Telcordia GR-1244-CORE requirements specify maximum phase transient slope during clock rearrangement in terms of nanoseconds per millisecond. The equivalent ps/μs unit is used here since the maximum phase transient magnitude for the Si5320 (tPT_MTIE) never reaches one nanosecond.

Table 4. AC Characteristics (PLL Performance Characteristics) (Continued)
(V_{DD33} = 3.3 V ±10%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wander/Jitter at 6400 Hz Bandwidth (BWSEL[1:0] = 00 and DBLBW = 1)						
Jitter Tolerance (see Figure 8)		f = 64 Hz	500	—	—	ns
		f = 640 Hz	50	—	—	ns
		f = 6400 Hz	5	—	—	ns
CLKOUT RMS Jitter Generation FEC[1:0] = 00	$J_{GEN(rms)}$	12 kHz to 20 MHz	—	0.7	1.0	ps
		50 kHz to 80 MHz	—	0.25	0.3	ps
CLKOUT Peak-Peak Jitter Generation FEC[1:0] = 00	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	6.6	9.0	ps
		50 kHz to 80 MHz	—	3.8	5.0	ps
Jitter Transfer Bandwidth (see Figure 7)	F_{BW}	BW = 6400 Hz	—	6400	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 6400 Hz	—	0.05	0.1	dB
Wander/Jitter at 6400 Hz Bandwidth (BWSEL[1:0] = 11 and DBLBW = 0)						
Jitter Tolerance (see Figure 8) (1/1 Scaling)	$J_{TOL(PP)}$	f = 64 Hz	1000	—	—	ns
		f = 640 Hz	100	—	—	ns
		f = 6400 Hz	10	—	—	ns
CLKOUT RMS Jitter Generation FEC[1:0] = 00 (1/1 Scaling)	$J_{GEN(rms)}$	12 kHz to 20 MHz	—	1.0	1.4	ps
		50 kHz to 80 MHz	—	0.38	0.5	ps
CLKOUT RMS Jitter Generation FEC[1:0] = 01, 10 (255/238, 238/255 scaling)	$J_{GEN(rms)}$	12 kHz to 20 MHz	—	0.94	1.4	ps
		50 kHz to 80 MHz	—	0.41	0.6	ps
CLKOUT Peak-Peak Jitter Generation FEC[1:0] = 00 (1/1 Scaling)	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	9.4	12.0	ps
		50 kHz to 80 MHz	—	4.7	5.5	ps
CLKOUT Peak-Peak Jitter Generation FEC[1:0] = 01, 10 (255/238, 238/255 scaling)	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	8.3	12.0	ps
		50 kHz to 80 MHz	—	4.6	5.5	ps
Jitter Transfer Bandwidth (see Figure 7)	F_{BW}	BW = 6400 Hz	—	6400	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 6400 Hz	—	0.05	0.1	dB

Notes:
1. Higher PLL bandwidth settings provide smaller clock output wander with temperature gradient.
2. For reliable device operation, temperature gradients should be limited to 10 °C/min.
3. Telcordia GR-1244-CORE requirements specify maximum phase transient slope during clock rearrangement in terms of nanoseconds per millisecond. The equivalent ps/μs unit is used here since the maximum phase transient magnitude for the Si5320 (tPT_MTIE) never reaches one nanosecond.

Table 4. AC Characteristics (PLL Performance Characteristics) (Continued)
(V_{DD33} = 3.3 V ±10%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wander/Jitter at 12800 Hz Bandwidth (BWSEL[1:0] = 11 and DBLBW = 1)						
Jitter Tolerance (see Figure 8)		f = 128 Hz	500	—	—	ns
		f = 1280 Hz	50	—	—	ns
		f = 12800 Hz	5	—	—	ns
CLKOUT RMS Jitter Generation FEC[1:0] = 00 (1/1 Scaling)	$J_{GEN(rms)}$	12 kHz to 20 MHz	—	0.74	1.0	ps
		50 kHz to 80 MHz	—	0.30	0.4	ps
CLKOUT Peak-Peak Jitter Generation FEC[1:0] = 00 (1/1 Scaling)	$J_{GEN(PP)}$	12 kHz to 20 MHz	—	6.9	9.0	ps
		50 kHz to 80 MHz	—	4.0	5.0	ps
Jitter Transfer Bandwidth (see Figure 7)	F_{BW}	BW = 12,800 Hz	—	12800	—	Hz
Wander/Jitter Transfer Peaking	J_P	< 12,800 Hz	—	0.05	0.1	dB
Acquisition Time	T_{AQ}	RSTN/CAL high to CAL_ACTV low, with valid clock input and VALTIME = 0	—	300	350	ms
Clock Output Wander with Temperature Gradient [1,2]	C_{CO_TG}	Stable Input Clock; Temperature Gradient <10 °C/min; 800 Hz Loop BW	—	—	50	ps/ °C/ min
Initial Frequency Accuracy in Digital Hold Mode (first 100 ms with supply voltage and temperature held constant)	C_{DH_FA}	Stable Input Clock Selected until entering Digital Hold	—	—	10	ppm
Clock Output Frequency Accuracy Over Temperature in Digital Hold Mode	C_{DH_T}	Constant Supply Voltage	—	16.7	40	ppm /°C
Clock Output Frequency Accuracy Over Supply Voltage in Digital Hold Mode	C_{DH_V33}	Constant Temperature	—	—	250	ppm /V

Notes:
1. Higher PLL bandwidth settings provide smaller clock output wander with temperature gradient.
2. For reliable device operation, temperature gradients should be limited to 10 °C/min.
3. Telcordia GR-1244-CORE requirements specify maximum phase transient slope during clock rearrangement in terms of nanoseconds per millisecond. The equivalent ps/μs unit is used here since the maximum phase transient magnitude for the Si5320 (tPT_MTIE) never reaches one nanosecond.

Table 4. AC Characteristics (PLL Performance Characteristics) (Continued)
(V_{DD33} = 3.3 V ±10%, TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock Output Phase Step[3] (See Figure 9)	t_{PT_MTIE}	When hitlessly recovering from Digital Hold mode 1/1	— –200	 0	 200	 ps
Clock Output Phase Step Slope[3] (See Figure 9) BWSEL[1:0] = 11, FEC[1:0] = 00, DBLBW = 0 BWSEL[1:0] = 00, FEC[1:0] = 00, DBLBW = 0 BWSEL[1:0] = 01, FEC[1:0] = 00, DBLBW = 0 BWSEL[1:0] = 10, FEC[1:0] = 00, DBLBW = 0	m_{PT}	When hitlessly recovering from Digital Hold mode 6400 Hz, No Scaling 3200 Hz, No Scaling 1600 Hz, No Scaling 800 Hz, No Scaling	 — — — —	 — — — —	 10 5 2.5 1.25	 ps/µs

Notes:
1. Higher PLL bandwidth settings provide smaller clock output wander with temperature gradient.
2. For reliable device operation, temperature gradients should be limited to 10 °C/min.
3. Telcordia GR-1244-CORE requirements specify maximum phase transient slope during clock rearrangement in terms of nanoseconds per millisecond. The equivalent ps/µs unit is used here since the maximum phase transient magnitude for the Si5320 (tPT_MTIE) never reaches one nanosecond.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
3.3 V DC Supply Voltage	V_{DD33}	–0.5 to 3.7	V
LVTTL Input Voltage	V_{DIG}	–0.3 to (V_{DD33} + 0.3)	V
Maximum Current any output PIN		±50	mA
Operating Junction Temperature	T_{JCT}	–55 to 150	°C
Storage Temperature Range	T_{STG}	–55 to 150	°C
ESD HBM Tolerance (100 pf, 1.5 kΩ)		1.0	kV

Note: Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	46	°C/W

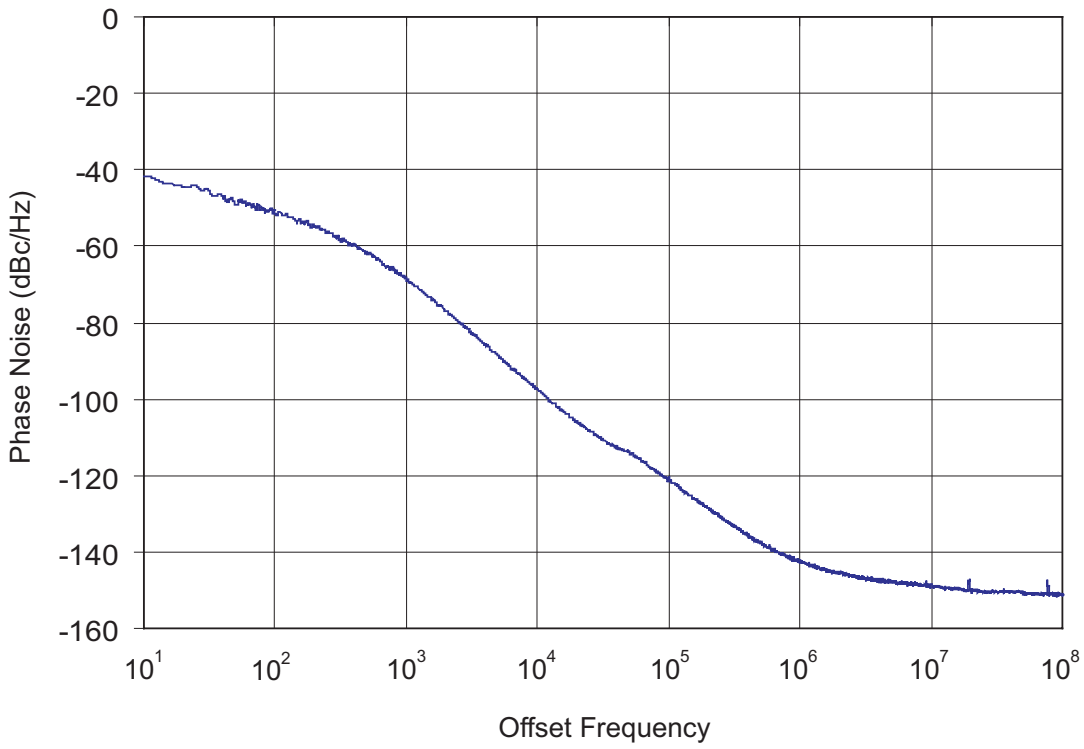
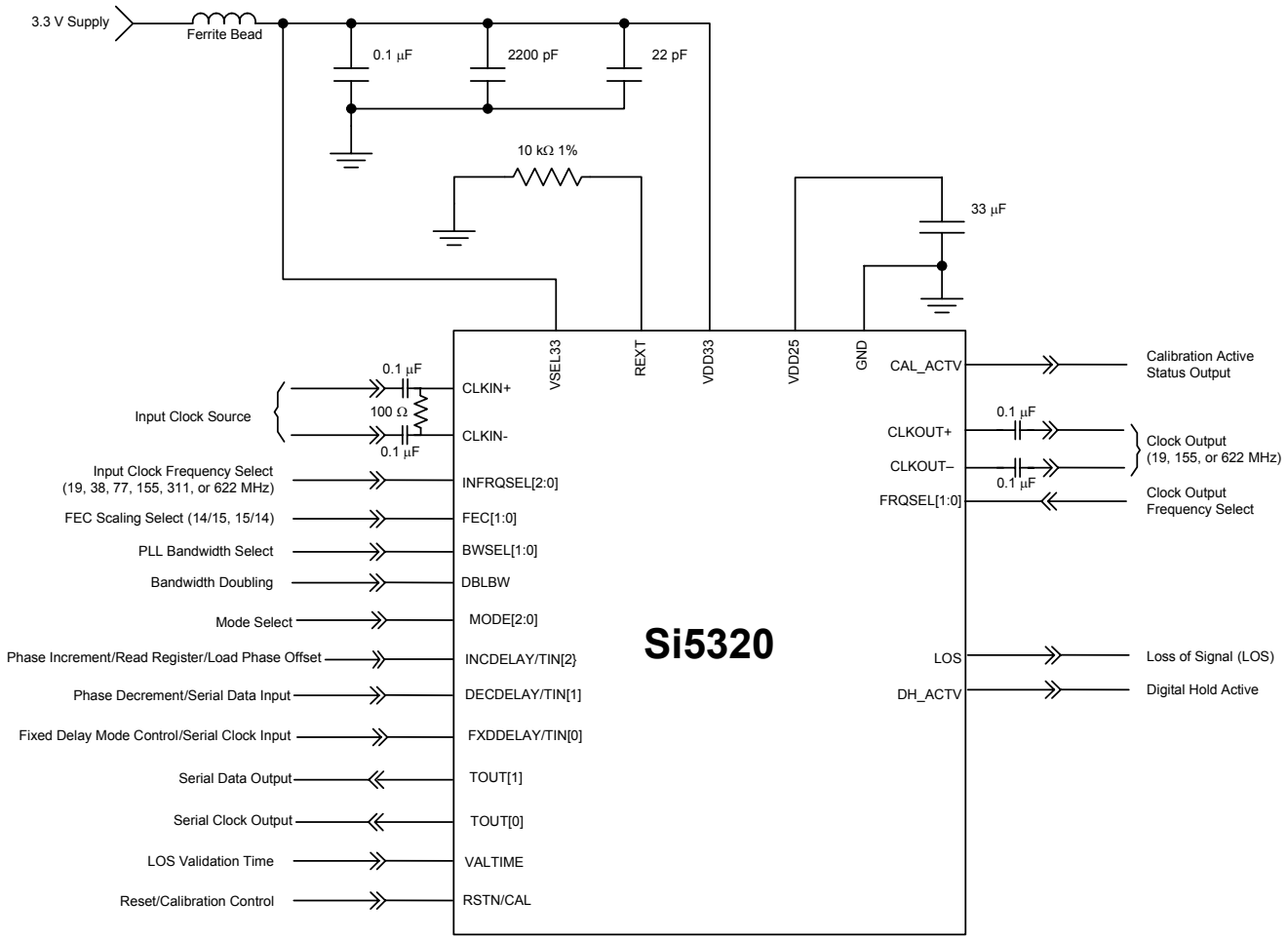


Figure 6. Typical Si5320 Phase Noise (CLKIN = 155.52 MHz, CLKOUT = 622.08 MHz, and Loop BW = 800 Hz)

2. Typical Application Schematic (3.3 V Supply)



3. Functional Description

The Si5320 is a high-performance precision clock multiplication and clock generation device. This device accepts a clock input in the 19, 38, 77, 155, 311, or 622 MHz range, attenuates significant amounts of jitter, and multiplies the input clock frequency to generate a clock output in the 19, 155, or 622 MHz range. Additional optional scaling by a factor of either 255/238 (15/14) or 238/255 (14/15) is provided for compatibility with systems that provide or require clocks that are scaled for forward error correction (FEC) rates. Typical applications for the Si5320 in SONET/SDH systems would be the generation and/or cleaning of 19.44, 155.52, or 622.08 MHz clocks from 19.44, 38.88, 77.76, 155.52, 311.04, or 622.08 MHz clock sources.

The Si5320 employs Silicon Laboratories DSPLL® technology to provide excellent jitter performance while minimizing the external component count and maximizing flexibility and ease-of-use. The Si5320's DSPLL phase locks to the input clock signal, attenuates jitter, and multiplies the clock frequency to generate the device's SONET/SDH-compliant clock output. The DSPLL loop bandwidth is user-selectable, allowing the Si5320's jitter performance to be optimized for different applications. The Si5320 can produce a clock output with jitter generation as low as 0.3 ps_{rms} (see Table 4), making the device an ideal solution for clock multiplication in SONET/SDH (including OC-48 and OC-192) and Gigabit Ethernet systems.

The Si5320 monitors the clock input signal for loss-of-signal, and provides a loss-of-signal (LOS) alarm when missing pulses are detected. The Si5320 provides a digital hold capability to continue generation of a stable output clock when the input reference is lost.

3.1. DSPLL®

The Si5320's phase-locked loop (PLL) uses Silicon Laboratories' DSPLL technology to eliminate jitter, noise, and the need for external loop filter components found in traditional PLL implementations. This is achieved by using a digital signal processing (DSP) algorithm to replace the loop filter commonly found in analog PLL designs. This algorithm processes the phase detector error term and generates a digital control value to adjust the frequency of the voltage-controlled oscillator (VCO). The technology produces clocks with less jitter than is generated using traditional methods. See Figure 6 for an example phase noise plot. In addition, because external loop filter components are not required, sensitive noise entry points are eliminated, making the DSPLL less susceptible to board-level noise sources.

This digital technology also allows for highly-stable and consistent operation over all process, temperature, and voltage variations. The benefits are smaller, lower power, cleaner, more reliable, and easier-to-use clock circuits.

3.1.1. Selectable Loop Filter Bandwidth

The digital nature of the DSPLL loop filter allows control of the loop filter parameters without the need to change external components. The Si5320 provides the user with up to eight user-selectable loop bandwidth settings for different system requirements. The base loop bandwidth is selected using the BWSEL [1:0] along with DBLBW = 0 pins. When DBLBW is driven high, the bandwidth selected on the BWSEL[1:0] pins is doubled. (See Table 7.)

When DBLBW is asserted, the Si5320 shows improved jitter generation performance. DBLBW function is defined only when hitless recovery and FEC scaling are disabled. Therefore, when DBLBW is high, the user must also drive FXDDELAY high and FEC[1:0] to 00 for proper operation.

3.2. Clock Input and Output Rate Selection

The Si5320 provides a 1/32x, 1/16x, 1/8x, 1/4x, 1/2x, 1x, 2x, 4x, 8x, 16x, or 32x clock frequency multiplication function with an option for additional frequency scaling by a factor of 255/238 or 238/255 for FEC rate compatibility. Output rates vary in accordance with the input clock rate. The multiplication factor is configured by selecting the input and output clock frequency ranges for the device.

The Si5320 accepts an input clock in the 19, 38, 77, 155, 311, or 622 MHz frequency range. The input frequency range is selected using the INFRQSEL[2:0] pins. The INFRQSEL[2:0] settings and associated output clock rates are given in Table 8.

The Si5320's DSPLL phase locks to the clock input signal to generate an internal VCO frequency that is a multiple of the input clock frequency. The internal VCO frequency is divided down to produce a clock output in the 19, 155, or 622 MHz frequency range. The clock output range is selected using the Frequency Select (FRQSEL[1:0]) pins. The FRQSEL[1:0] settings and associated output clock rates are given in Table 9.

The Si5320 clock input frequencies are variable within the range specified in Table 3 on page 8. The output rates scale accordingly. When a 19.44 MHz input clock is used with no FEC scaling enabled, the clock output frequency is 19.44, 155.52, or 622.08 MHz.

Table 7. Loop Bandwidth Settings

Loop Bandwidth	BWSEL1	BWSEL0	DBLBW*
12800 Hz	1	1	1
6400 Hz	1	1	0
6400 Hz	0	0	1
3200 Hz	0	0	0
3200 Hz	0	1	1
1600 Hz	0	1	0
1600 Hz	1	0	1
800 Hz	1	0	0

***Note:** When DBLBW = 1, FXDDELAY must be asserted and FEC scaling must be disabled.

Table 8. Nominal Clock Input Frequencies

Input Clock Frequency Range	INFRQSEL2	INFRQSEL1	INFRQSEL0
Reserved	1	1	1
622 MHz	1	1	0
311 MHz	1	0	1
155 MHz	1	0	0
77 MHz	0	1	1
38 MHz	0	1	0
19 MHz	0	0	1
Reserved	0	0	0

Table 9. Nominal Clock Output Frequencies

Output Clock Frequency Range	FRQSEL1	FRQSEL0
622 MHz	1	1
155 MHz	1	0
19 MHz	0	1
Driver Powerdown	0	0

Table 10. FEC Frequency Scalings

FEC Frequency Scaling	FEC1	FEC0
1/1	0	0
255/238	0	1
238/255	1	0
Reserved	1	1

3.2.1. FEC Rate Conversion

The Si5320 provides a 1/32x, 1/16x, 1/8x, 1/4x, 1/2x, 1x, 2x, 4x, 8x, 16x, or 32x clock frequency multiplication function with an option for additional frequency scaling by a factor of 255/238 or 238/255 for FEC rate compatibility. The multiplication factor is configured by selecting the input and output clock frequency ranges for the device. The additional frequency scaling by a factor of either 255/238 or 238/255 for FEC compatibility is selected using the FEC[1:0] control inputs. (See Table 10.)

For example, a 622.08 MHz output clock (a non-FEC rate) can be generated from a 19.44 MHz input clock (a non-FEC rate) by setting INFRQSEL[2:0] = 001 (19.44 MHz range), setting FRQSEL [1:0] = 11 (32x multiplication), and setting FEC[1:0] = 00 (no FEC scaling).

A 666.51 MHz output clock (a FEC rate) can be generated from a 19.44 MHz input clock (a non-FEC rate) by setting INFRQSEL[2:0] = 001 (19.44 MHz range), setting FRQSEL [1:0] = 11 (32x multiplication), and setting FEC[1:0] = 01 (255/238 FEC scaling). Finally, a 622.08 MHz output clock (a non-FEC rate) can be generated from a 20.83 MHz input clock (a FEC rate) by setting INFRQSEL[2:0] = 001 (19.44 MHz range), setting FRQSEL [1:0] = 11 (32x multiplication), and setting FEC[1:0] = 10 (238/255 FEC scaling).

3.3. PLL Performance

The Si5320 PLL is designed to provide extremely low jitter generation, high jitter tolerance, and a well-controlled jitter transfer function with low peaking and a high degree of jitter attenuation.

3.3.1. Jitter Generation

Jitter generation is defined as the amount of jitter produced at the output of the device with a jitter free input clock. Generated jitter arises from sources within the VCO and other PLL components. Jitter generation is also a function of the PLL bandwidth setting. Higher loop bandwidth settings may result in lower jitter generation, but may also result in less attenuation of jitter on the input clock signal.

3.3.2. Jitter Transfer

Jitter transfer is defined as the ratio of output signal jitter to input signal jitter for a specified jitter frequency. The jitter transfer characteristic determines the amount of input clock jitter that passes to the outputs. The DSPLL technology used in the Si5320 provides tightly-controlled jitter transfer curves because the PLL gain parameters are determined by digital circuits that do not vary over supply voltage, process, and temperature. In a system application, a well-controlled transfer curve

minimizes the output clock jitter variation from board to board, providing more consistent system level jitter performance.

The jitter transfer characteristic is a function of the BWSEL[1:0] setting. (See Table 7.) Lower bandwidth selection settings result in more jitter attenuation of the incoming clock but may result in higher jitter generation. Table 4 on page 10 gives the 3 dB bandwidth and peaking values for specified BWSEL settings. Figure 7 shows the jitter transfer curve mask.

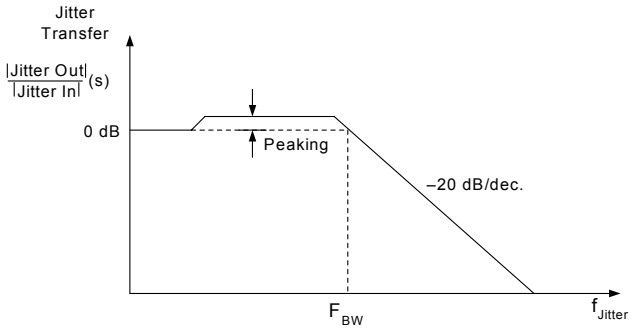


Figure 7. PLL Jitter Transfer Mask/Template

3.3.3. Jitter Tolerance

Jitter tolerance for the Si5320 is defined as the maximum peak-to-peak sinusoidal jitter that can be present on the incoming clock. The tolerance is a function of the jitter frequency, because tolerance improves for lower input jitter frequency. See Figure 8.

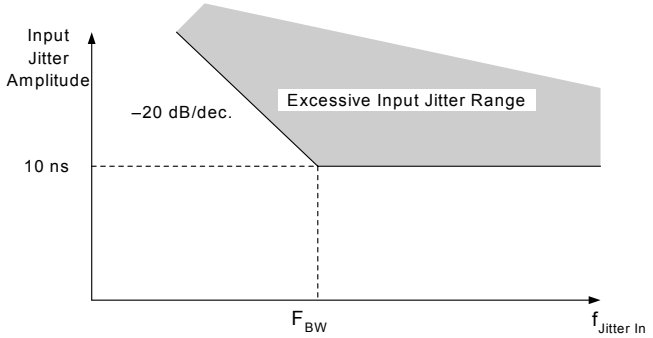


Figure 8. Jitter Tolerance Mask/Template

3.4. Digital Hold of the PLL

When no valid input clock is available, the Si5320 digitally holds the internal oscillator to its last frequency value. This provides a stable clock to the system until an input clock is again valid. This clock maintains very stable operation in the presence of constant voltage and temperature. The frequency accuracy specifications for digital hold mode are given in Table 4 on page 10.

3.5. Hitless Recovery from Digital Hold

When the Si5320 device is locked to a valid input clock, a loss of the input clock causes the device to automatically switch to digital hold mode. When the input clock signal returns, the device performs a "hitless" transition from digital hold mode back to the selected input clock. That is, the device performs "phase build-out" to absorb the phase difference between the internal VCO clock operating in digital hold mode and the new/returned input clock. The maximum phase step size seen at the clock output during this transition and the maximum slope for this phase step are given in Table 4 on page 10.

This feature can be disabled by asserting the FXDDELAY pin. When the FXDDELAY pin is high, the output clock is phase and frequency locked with a known phase relationship to the input clock. Consequently, any abrupt phase change on the input clock propagates through the device, and the output slews at the selected loop bandwidth until the original phase relationship is restored.

Note: When the DBLBW is asserted, hitless recovery must also be disabled by driving FXDDELAY high for proper operation.

When the device is in output phase adjust mode, the state of FXDDELAY cannot be changed. Upon entry into phase adjust mode, the device remembers the last valid state of FXDDELAY, and this setting is fixed while the device is in output phase adjust mode.

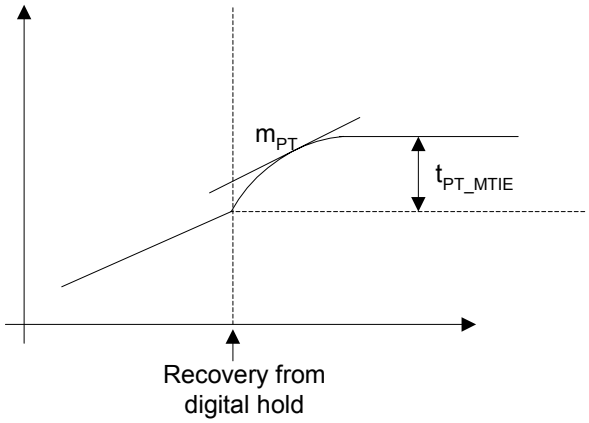


Figure 9. Recovery from Digital Hold

3.6. Output Phase Adjust Mode (Pin Control)

The INCDELAY and DECDELAY pins adjust the phase of the Si5320 clock output. Adjustment is accomplished by driving a pulse (a transition from low to high and then back to low) into one of these pins as the other pin is

held at a logic low level.

Each pulse on the INCDELAY pin adds a fixed delay to the Si5320 clock output. The amount of delay time is equal to twice the period of a 622 MHz output clock ($t_{DELAY} = 2/f_{O\_622}$).

Each pulse on the DECDELAY pin removes a fixed amount of delay from the Si5320 clock output. The fixed delay time is equal to twice the period of the 622 MHz output clock ($t_{DELAY} = 2/f_{O\_622}$).

The frequency of the 622 MHz output clock (f_{O_622}) is nominally 32x the frequency of the input clock. The frequency of the 622 MHz output clock (f_{O_622}) is scaled according to the setting of the FEC[1:0] pins.

When the phase of the Si5320 clock output is adjusted using the INCDELAY and/or DECDELAY pins, the output clock will typically begin to move within 2 µs. However, it will move to its new phase setting at a rate of change that is determined by the setting of the BWSEL[1:0] pins.

Note: INCDELAY and DECDELAY are ignored when the Si5320 operates in digital hold (DH) mode.

3.7. Output Phase Adjust Mode (Register Control)

The Si5320 can be placed in a special mode to externally adjust the device output clock phase. This mode of operation can be used to manually increment or decrement the output clock phase using internal device registers.

The Si5320 has two output phase adjust options: coarse phase adjust and fine phase adjust. Coarse phase adjust allows the clock output phase to be incremented or decremented in 3.22 ns steps, based on an output clock frequency of 622.08 MHz (step size = 2/f_{CLKOUT}), by forcing the PLL feedback divider circuitry to spit or swallow clock cycles. Fine phase adjust is done by externally setting the value of the offset DAC in the phase detector. Fine phase adjust allows the clock output phase to be incremented or decremented in 100 ps steps, based on an output clock frequency of 622.08 MHz (step size = 1/(16 x f_{CLKOUT})). Coarse phase adjust and fine phase adjust can be used together or separately.

In this mode of operation, the state of FXDDELAY cannot be changed. Instead, the device remembers the last valid state of FXDDELAY and uses this setting for the entire time the device is in output phase adjust mode. For example, if FXDDELAY is tied low when the device enters output phase adjust mode, hitless recovery from digital hold is enabled during output phase adjust mode. If FXDDELAY is tied high when the device enters output phase adjust mode, hitless recovery from digital hold is disabled during output phase adjust mode. In either case, the output phase can be adjusted.

In the fine phase adjust mode, it takes two steps to manually adjust the device output clock phase. The first step, Register Read Out, is used to acquire the current phase detector value. The second step, Output Phase Increment/Decrement, is used to manually increment or decrement the DAC value, and write it back to the Si5320 to achieve the desired phase adjust. The MODE [2:0] pins determine whether the device is being used to read the phase detector DAC value or increment/ decrement the output phase. Table 11 lists the device control pins and associated functions when the device is in output phase adjust mode.

Table 11. Output Phase Adjust Control Pins

Device Pin	I/O	Location	Normal Operation	Register Read Out	Output Phase INC/DEC
MODE[2]	I	B6	0	1	0
MODE[1]	I	B7	0	1	0
MODE[0]	I	C8	0	0	1
INCDELAY/t_{IN}[2]	I	B2	INCDELAY	READ	LOAD
DECDELAY/t_{IN}[1]	I	B3	DECDELAY	N/A	SDI
FXDDELAY/t_{IN}[0]	I	B4	FXDDELAY	ENVSEL	SCLKI
t_{OUT}[1]	O	A5	0	SDO	N/A
t_{OUT}[0]	O	A6	0	SCLKO	N/A

3.7.1. Register Read Out

To read the phase detector DAC value, the MODE [2:0] pins must be set to 110.

When configured to read this register value, the device operates normally except that a high level on the READ input signal causes the values of many of the internal digital registers to be periodically copied into parallel shadow registers. After a brief delay, the values in the shadow registers are serially shifted out through the serial data output pin, SDO, and synchronized to the serial clock output, SCLKO. The register read envelope is bounded by a four-bit preamble 0101. As long as READ remains high, the internal registers are re-sampled and shifted out once every 256 cycles of SCLKO. The complete I/O data format and timing for register readout is shown in Figure 5 on page 6.

During register read out, the SCLKO and SDO pins drive out a low value except when driving out the register read envelope. Once a readout sequence commences, the entire register read envelope is shifted out, regardless of any changes on READ. The ENVSEL signal should be set high to read the phase detector DAC value.

The 119-bit READ register chain is defined as follows:

Reserved[21:0]	pdDAC[6:0]	Reserved[89:0]

The data contents of the register read envelope are shifted out from left to right.

3.7.2. Output Phase Increment/Decrement

MODE [2:0] pins are set to 001 to write back the desired DAC codes. Serial clock and data inputs (SCLKI and SDI) are used to serially program a 27-bit chain of phase adjust registers. A parallel load signal (LOAD) is then used to drive the serially-programmed values into the phase offset (auto-zeroing) DAC and into the pulse spitting/swallowing circuitry. This allows external control of the phase offset DAC for fine output phase adjust and external control of the pulse spitting/swallowing circuitry for coarse phase adjust of the Si5320 output phase. Timing constraints for programming the Si5320 phase adjust registers and for loading in the new values are shown in Figure 5 on page 6. The 27-bit phase adjust register chain is defined as follows:

pdDAC[6:0]	spit	swallow	Reserved[17:0]

The register bits pdDAC[6:0] provide output phase increments as small as 100 ps. The spit and swallow register bits provide coarse control of the Si5320 output phase, nominally 3.22 ns for a 622.08 MHz output clock.

This register chain is filled from left to right. The first bit to be serially shifted in is pdDAC[6], then pdDAC[5], then pdDAC[4], etc. A rising edge on SCLKI is required to program each bit into the output phase adjust register. It takes 27 rising edges of SCLKI to fully program the phase adjust register chain. The last 18 bits in the output phase adjust register are reserved by the Si5320 and must be set to 1000000_1_1_1000000_1_1.

A rising edge on the LOAD signal will load the programmed values directly into the phase offset (auto-zeroing) DAC. If either the spit or swallow register bits are programmed high, a rising edge on LOAD will cause the associated circuitry to spit or swallow a single 311 MHz (3.22 ns) pulse. To spit or swallow several pulses in a row, apply several consecutive pulses of LOAD. If both the spit and swallow register bits are programmed high, neither spit nor swallow functions will be performed. Table 12 shows the valid settings for the spit and swallow bits.

Table 12. Spit and Swallow Register Bit Configuration (f_{O_622} = 622 MHz)

Spit	Swallow	Outcome
0	0	No phase adjust occurs
1	0	3.22 ns phase decrement
0	1	3.22 ns phase increment
1	1	No phase adjust occurs

The Si5320-XC3 has a special production test mode. This mode is entered when the mode select lines are set to MODE[2:0] = 111. If this happens during operation, the part is not guaranteed to meet data sheet specifications. Furthermore, because no application can guarantee that the state of all three mode select lines will switch simultaneously, the mode select lines should be changed one bit at a time. This process will ensure that the device never enters the state MODE[2:0]=111. Because the Si5320 samples the state of the mode select lines approximately every 210 ns, a delay of approximately 500 ns between states is recommended to ensure the device samples each state correctly.

An example of how this might be done is as follows:

To change from normal operation to the register read mode, the following sequence should be used: MODE[2:0] = 000, 100, 110.

To change from register read to the register write mode, use this sequence: MODE[2:0] = 110, 100, 000, 001.

While it is unlikely for any problems caused by this timing to occur, it is possible to inadvertently enter the mode 111 unless this procedure is followed.

The following steps illustrate a hypothetical output phase decrement sequence:

1. Read the current device phase detector DAC values by setting MODE[2:0] to 110, setting ENVSEL high for the duration of the register read cycle, and pulsing READ high. Following the 4-bit preamble 0101, the device will return the contents of the 119-bit READ register. The following example assumes the phase detector DAC value is 1000000. A read of the READ register would return:
   1000000_xxxx_1000000_xxxx_1000000_xxx...
2. Perform a coarse phase decrement on the device clock outputs. Set MODE[2:0] to 001 and use the serial clock input (SCLKI) and serial data input (SDI) to load the following values into the phase adjust register chain:
   1000000_1_0_1000000_0_0_1000000_0_0

Note: The Reserved[17:0] bits must always be set to 1000000_0_0_1000000_0_0 during output phase adjust mode. This example assumes the previous value of the phase detector DAC is 1000000.

   Apply a single pulse to the parallel load pin (LOAD). This will cause the Si5320 phase detector to remove a fixed delay from the device clock outputs. The amount of delay removed from the clock outputs is equal to twice the period of a 622 MHz nominal clock ($t_{DELAY} = 2/f_{O\_622}$), or 3.22 ns.
3. Read the current device phase detector DAC values by setting MODE[2:0] to 110, setting ENVSEL high for the duration of the register read cycle, and pulsing READ high. Following the 4-bit preamble 0101, the device will return the contents of the 119-bit READ register. The following example assumes the phase detector DAC value is 1000000. A read of the READ register would return:
   1000000_xxxx_1000000_xxxx_1000000_xxx...
4. Perform a fine phase decrement on the device clock outputs. Set MODE[2:0] to 001 and use the serial clock input (SCLKI) and serial data input (SDI) to load the following values into the phase adjust register chain:
   1000001_0_0_1000000_0_0_1000000_0_0
   Apply a single pulse to the parallel load pin (LOAD). This will cause the Si5320 phase detector to remove a fixed amount of delay from the device clock outputs. The amount of delay removed from the clock outputs is equal to 1/16th the period of a 622 MHz nominal clock ($t_{DELAY} = 1/(16 \times f_{O\_622})$), or 100 ps.

The following steps illustrate a hypothetical output phase increment sequence:

1. Read the current device phase detector DAC values by setting MODE[2:0] to 110, setting ENVSEL high for the duration of the register read cycle, and pulsing READ high. Following the 4-bit preamble 0101, the device will return the contents of the 119-bit READ register. The following example assumes the phase detector DAC value is 1000000. A read of the READ register would return:
   1000000_xxxx_1000000_xxxx_1000000_xxx...
2. Perform a coarse phase increment on the device clock outputs. Set MODE[2:0] to 001 and use the serial clock input (SCLKI) and serial data input (SDI) to load the following values into the phase adjust register chain:
   1000000_0_1_1000000_0_0_1000000_0_0
   Apply a single pulse to the parallel load pin (LOAD). This will cause the Si5320 phase detector to add a fixed amount of delay to the device clock outputs. The amount of delay added to the clock outputs is equal to twice the period of a 622 MHz nominal clock ($t_{DELAY} = 2/f_{O\_622}$), or 3.22 ns.
3. Read the current device phase detector DAC values by setting MODE[2:0] to 110, setting ENVSEL high for the duration of the register read cycle, and pulsing READ high. Following the 4-bit preamble 0101, the device will return the contents of the 119-bit READ register. The following example assumes the phase detector DAC value is 1000000. A read of the READ register would return:
   1000000_xxxx_1000000_xxxx_1000000_xxx...
4. Perform a fine phase increment on the device clock outputs. Set MODE[2:0] to 001 and use the serial clock input (SCLKI) and serial data input (SDI) to load the following values into the phase adjust register chain:
   0111111_0_0_1000000_0_0_1000000_0_0
   Apply a single pulse to the parallel load pin (LOAD). This will cause the Si5320 phase detector to add a fixed delay to the device clock outputs. The amount of delay added to the clock outputs is equal to 1/16th the period of a 622 MHz nominal clock ($t_{DELAY} = 1/(16 \times f_{O\_622})$), or 100 ps.

For a coarse phase increment or decrement, the amount of delay time added or subtracted to the clock output is equal to twice the period of a nominal 622.08 MHz output clock, or 3.22 ns ($2xT_{622.08} = 3.22$ ns). For a fine phase increment or decrement, the amount of delay time added or subtracted to the clock output is equal to 1/16th the period of a nominal 622 MHz output clock or 100 ps ($1/16 \times T_{622.08} = 100$ ps). The frequency of f_{O_622} is scaled according to the setting of the FEC[1:0] pins.

When the phase of the Si5320 clock output is adjusted using the output phase adjust mode, the output clock

will typically begin to move within 2 µs. However, it will move to its new phase setting at a rate of change that is determined by the setting of the BWSEL[1:0] pins.

3.8. Loss-of-Signal Alarm

The Si5320 has loss-of-signal (LOS) circuitry that constantly monitors the CLKIN input clock for missing pulses. The LOS circuitry sets a LOS output alarm signal when missing pulses are detected.

The LOS circuitry operates as follows. Regardless of the selected input clock frequency range, the LOS circuitry divides down the input clock into the 19 MHz range. The LOS circuitry then over-samples this divided-down input clock to search for extended periods of time without input clock transitions. If the LOS circuitry detects four consecutive samples of the divided-down input clock that are the same state (i.e., 1111 or 0000), a LOS condition is declared, the Si5320 goes into digital hold mode, and the LOS output alarm signal is set high. The LOS sampling circuitry runs at a frequency of $f_{O\_622/8}$, where f_{O_622} is the output clock frequency when the FRQSEL[1:0] pins are set to 11. Table 3 on page 8 lists the minimum and maximum transitionless time periods required for declaring a LOS on the input clock (t_{LOS}).

Once the LOS alarm is asserted, it is held high until the input clock is validated over a time period designated by the VALTIME pin. When VALTIME is low, the validation time period is about 100 ms. When VALTIME is high, the validation time period is about 13 s. If another LOS condition is detected on the input clock during the validation time (i.e., if another set of 1111 or 0000 samples are detected), the LOS alarm remains asserted, and the validation time starts over. When the LOS alarm is finally released, the Si5320 exits digital hold mode and locks to the input clock. The LOS alarm is automatically set high at power-on and at every low-to-high transition of the RSTN/CAL pin. In these cases, the Si5320 undergoes a self-calibration before releasing the LOS alarm and locking to the input clock.

The Si5320 also provides an output indicating the digital hold status of the device, DH_ACTV. The Si5320 only enters the digital hold mode upon the loss of the input clock. When this occurs, the LOS alarm will also be active. Therefore, applications that require monitoring of the status of the Si5320 need only monitor the CAL_ACTV and either the LOS or DH_ACTV outputs to know the state of the device.

3.9. Reset

The Si5320 provides a Reset/Calibration pin, RSTN/CAL, which resets the device and disables the outputs. When the RSTN/CAL pin is driven low, the internal circuitry enters into the reset mode, and all LVTTL outputs are forced into a high-impedance state. Also, the CLKOUT+ and CLKOUT– pins are forced to a nominal CML logic LOW and HIGH respectively (see Figure 10). This feature is useful for in-circuit test applications. A low-to-high transition on RSTN/CAL initializes all digital logic to a known condition and initiates self-calibration of the DSPLL. Upon completion of self-calibration, the DSPLL begins to lock to the clock input signal.

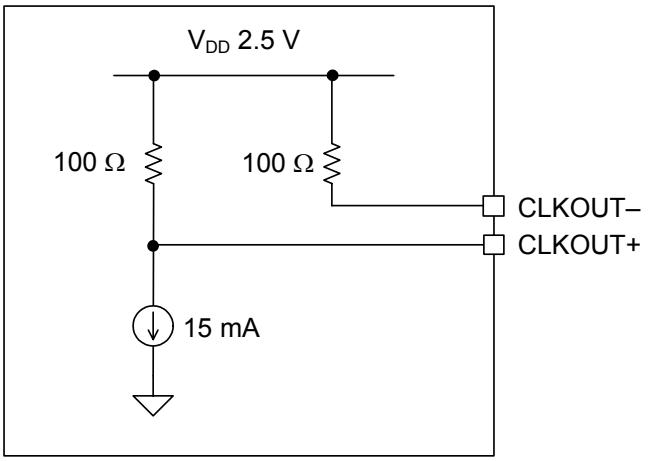


Figure 10. CLKOUT± Equivalent Circuit, RSTN/CAL Asserted LOW

3.10. PLL Self-Calibration

The Si5320 achieves optimal jitter performance by using self-calibration circuitry to set the VCO center frequency and loop gain parameters within the DSPLL. Internal circuitry generates self calibration automatically on powerup or after a loss of power condition. Self-calibration can also be manually initiated by a low-to-high transition on the RSTN/CAL input.

A self-calibration should be initiated after changing the state of the FEC[1:0] inputs.

Whether manually initiated or automatically initiated at powerup, the self-calibration process requires the presence of a valid input clock.

If self-calibration is initiated without a valid clock present, the device waits for a valid clock before completing self-calibration. The Si5320 clock output is set to the lower end of the operating frequency range while the device is waiting for a valid clock. After the clock input is validated, the calibration process runs to completion; the device locks to the clock input, and the clock output shifts to its target frequency. Subsequent losses of the input clock signal do not require re-calibration. If the clock input is lost following self-

calibration, the device enters digital hold mode. When the input clock returns, the device re-locks to the input clock without performing a self-calibration. During the calibration process, the output clock frequency is indeterminate and may jump as high as 5% above the final locked value.

3.11. Bias Generation Circuitry

The Si5320 makes use of an external resistor to set internal bias currents. The external resistor allows precise generation of bias currents, which significantly reduces power consumption and variation as compared to traditional implementations that use an internal resistor. The bias generation circuitry requires a 10 kΩ (1%) resistor connected between REXT and GND.

3.12. Differential Input Circuitry

The Si5320 provides a differential input for the clock input, CLKIN. This input is internally biased to a voltage of V_{ICM} (see Table 2 on page 7) and may be driven by a differential or single-ended driver circuit. For differential transmission lines, the termination resistor is connected externally as shown.

3.13. Differential Output Circuitry

The Si5320 utilizes a current mode logic (CML) architecture to drive the differential clock output, CLKOUT.

For single-ended output operation, simply connect to either CLKOUT+ or CLKOUT– and leave the unused signal unconnected.

3.14. Power Supply Connections

The Si5320 incorporates an on-chip voltage regulator. The voltage regulator requires an external compensation circuit of one resistor and one capacitor to ensure stability over all operating conditions.

Internally, the Si5320 V_{DD33} pins are connected to the on-chip voltage regulator input, and the V_{DD33} pins also supply power to the device's LVTTL I/O circuitry. The V_{DD25} pins supply power to the core DSPLL circuitry and are also used for connection of the external compensation circuit.

The regulator's compensation circuit is actually a resistor and a capacitor in series between the V_{DD25} node and ground. (See "2. Typical Application Schematic (3.3 V Supply)" on page 17.) Typically, the resistor is incorporated into the capacitor's equivalent series resistance (ESR). The target RC time constant for this combination is 15 to 50 µs. The capacitor used in the Si5320 evaluation board is a 33 µF tantalum capacitor with an ESR of 0.8 Ω. This gives an RC time constant of 26.4 µs. The Venkel part number, TA6R3TCR336KBR, is an example of a capacitor that meets these specs.

To get optimal performance from the Si5320 device, the power supply noise spectrum must comply with the plot in Figure 11. This plot shows the power supply noise tolerance mask for the Si5320. The customer should provide a 3.3 V supply that does not have noise density in excess of the amount shown in the diagram. However, the diagram cannot be used as spur criteria for a power supply that contains single tone noise.

3.15. Design and Layout Guidelines

Precision clock circuits are susceptible to board noise and EMI. To take precautions against unacceptable levels of board noise and EMI affecting performance of the Si5320, consider the following:

- Power the device from 3.3 V since the internal regulator provides at least 40 dB of isolation to the V_{DD25} pins (which power the PLL circuitry).
- Use an isolated local plane to connect the V_{DD25} pins. Avoid running signal traces over or below this plane without a ground plane in between.
- Route all I/O traces between ground planes as much as possible
- Maintain an input clock amplitude in the 200 mV_{PP} to 500 mV_{PP} differential range.
- Excessive high-frequency harmonics of the input clock should be minimized. The use of filters on the input clock signal can be used to remove high-frequency harmonics.

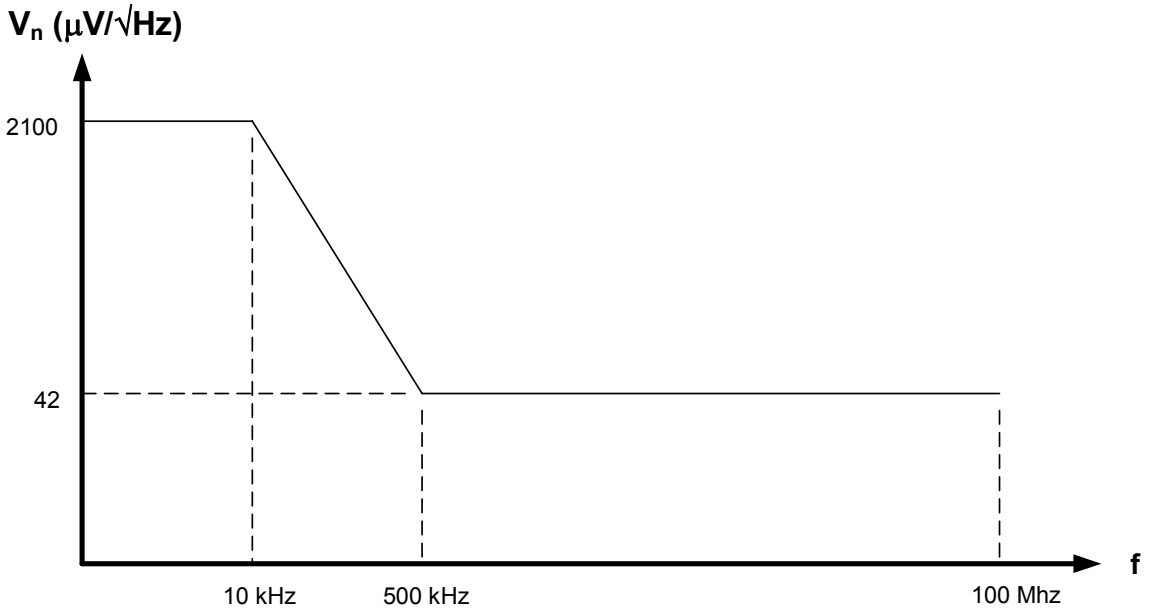
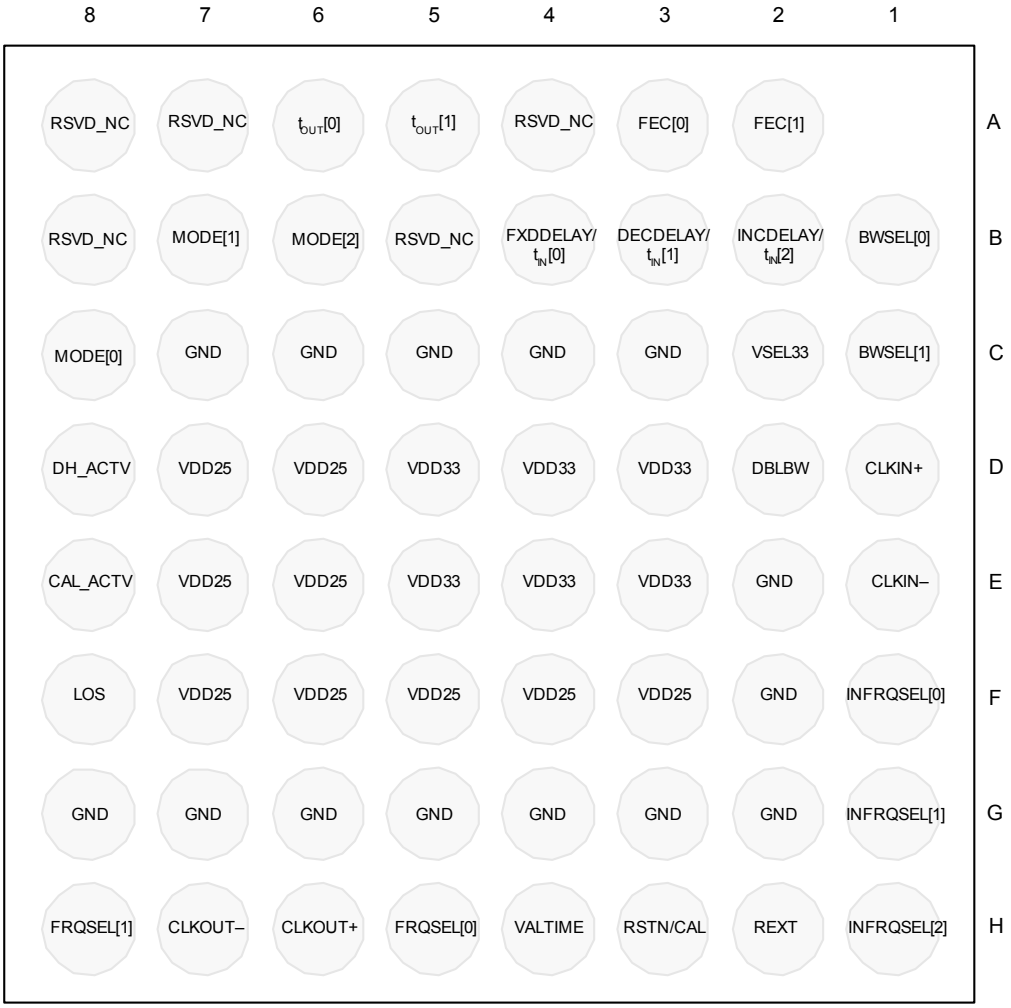


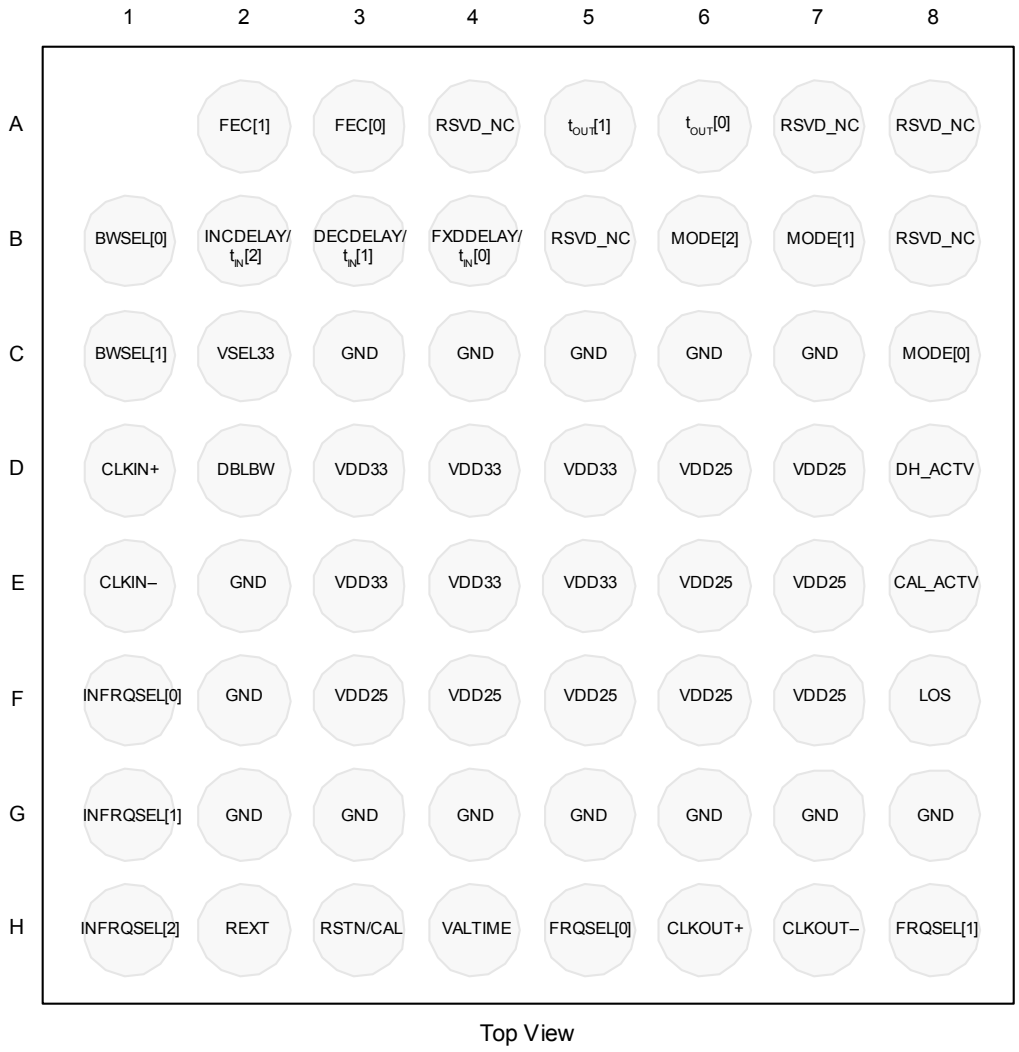
Figure 11. Power Supply Noise Tolerance Mask

4. Pin Descriptions: Si5320



Bottom View

Figure 12. Si5320 Pin Configuration (Bottom View)



Top View

Figure 13. Si5320 Pin Configuration (Transparent Top View)

Table 13. Si5320 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
D1 E1	CLKIN+ CLKIN–	I	See Table 2	**System Clock Input.** Clock input to the DSPLL circuitry. The frequency of the CLKIN signal is multiplied by the DSPLL to generate the CLKOUT clock output. The input-to-output frequency multiplication factor is set by selecting the clock input range and the clock output range. The frequency of the CLKIN clock input can be in the 19, 38, 77, 155, 311, or 622 MHz range (nominally 19.44, 38.88, 77.76, 155.52, 311.04, or 622.08 MHz) as indicated in Table 3 on page 8. The clock input frequency is selected using the INFRQSEL[2:0] pins. The clock output frequency is selected using the FRQSEL[1:0] pins. An additional scaling factor of either 255/238 or 238/255 may be selected for FEC operation using the FEC[1:0] control pins.
F1 G1 H1	INFRQSEL[0] INFRQSEL[1] INFRQSEL[2]	I*	LVTTL	**Input Frequency Range Select.** Pins(INFRQSEL[2:0]) select the frequency range for the input clock, CLKIN. (See Table 3 on page 8.) 000 = Reserved. 001 = 19 MHz range. 010 = 38 MHz range. 011 = 77 MHz range. 100 = 155 MHz range. 101 = 311 MHz range. 110 = 622 MHz range. 111 = Reserved.
F8	LOS	O	LVTTL	**Loss-of-Signal (LOS) Alarm for CLKIN.** Active high output indicates that the Si5320 has detected missing pulses on the input clock signal. The LOS alarm is cleared after either 100 ms or 13 seconds of a valid CLKIN clock input, depending on the setting of the VALTIME input.
D8	DH_ACTV	O	LVTTL	**Digital Hold Mode Active.** Active high output indicates that the DSPLL is in digital hold mode. Digital hold mode locks the current state of the DSPLL and forces the DSPLL to continue generation of the output clock with no additional phase or frequency information from the input clock.
***Note:** The LVTLL inputs on the Si5320 device have an internal pulldown mechanism that causes these inputs to default to a logic low state if the input is not driven from an external source.				

Table 13. Si5320 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
H3	RSTN/CAL	I*	LVTTL	**Reset/Calibrate.** When low, the internal circuitry enters the reset mode and all LVTTL outputs are forced into a high-impedance state. Also, the CLKOUT+ and CLKOUT– pins are forced to a nominal CML logic LOW and HIGH respectively. This feature is useful for in-circuit test applications. A low-to-high transition on RSTN/CAL initializes all digital logic to a known condition, enables the device output, and initiates self-calibration of the DSPLL. Upon completion of self-calibration, the DSPLL begins to lock to the selected clock input signal.
H6 H7	CLKOUT+ CLKOUT–	O	CML	**Differential Clock Output.** High frequency clock output. The frequency of the CLKOUT output is a multiple of the frequency of the CLKIN input. The input-to-output frequency multiplication factor is set by selecting the clock input range and the clock output range. The frequency of the CLKOUT clock output can be in the 19, 155, or 622 MHz range as indicated in Table 3 on page 8. The clock output frequency is selected using the FRQSEL[1:0] pins. The clock input frequency is selected using the INFRQSEL[2:0] pins. An additional scaling factor of either 255/238 or 238/255 may be selected for FEC operation using the FEC[1:0] control pins.
H5 H8	FRQSEL[0] FRQSEL[1]	I*	LVTTL	**Clock Output Frequency Range Select** Select frequency range of the clock output, CLKOUT. (See Table 3 on page 8.) 00 = Clock Driver Powerdown. 01 = 19 MHz Frequency Range. 10 = 155 MHz Frequency Range. 11 = 622 MHz Frequency Range.

***Note:** The LVTLL inputs on the Si5320 device have an internal pulldown mechanism that causes these inputs to default to a logic low state if the input is not driven from an external source.

Table 13. Si5320 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
A3 A2	FEC[0] FEC[1]	I*	LVTTL	**Forward Error Correction (FEC) Selection.** Enable or disable scaling of the input-to-output frequency multiplication factor for FEC clock rate compatibility. The frequency of the CLKOUT output is a multiple of the frequency of the CLKIN input. The input-to-output frequency multiplication factor is set by selecting the clock input range and the clock output range. The clock output frequency is selected using the FRQSEL[1:0] pins. The clock input frequency is selected using the INFRQSEL[2:0] pins. An additional scaling factor of either 255/238 or 238/255 may be selected for FEC operation using the FEC[1:0] control pins as indicated below. 00 = No FEC scaling. 01 = 255/238 FEC scaling for all clock outputs. 10 = 238/255 FEC scaling for all clock inputs. 11 = Reserved. **Note:** FEC[1:0] must be set to 00 when DBLBW is set high.
B1 C1	BWSEL[0] BWSEL[1]	I*	LVTTL	**Bandwidth Select.** BWSEL[1:0] pins set the bandwidth of the loop filter within the DSPLL to 6400, 3200, 1600, or 800 Hz as indicated below. 00 = 3200 Hz 01 = 1600 Hz 10 = 800 Hz 11 = 6400 Hz **Note:** The loop filter bandwidth will be twice the value indicated when DBLBW is set high.
E8	CAL_ACTV	O	LVTTL	**Calibration Mode Active.** This output is driven high during the DSPLL self-calibration and the subsequent initial lock acquisition period.
H4	VALTIME	I*	LVTTL	**Clock Validation Time for LOS.** VALTIME sets the clock validation times for recovery from an LOS alarm condition. When VALTIME is high, the validation time is approximately 13 seconds. When VALTIME is low, the validation time is approximately 100 ms.
B2, B3, B6, B7, C8	RSVD_GND		LVTTL	**Reserved—GND.** This pin must be tied to GND for normal operation.
***Note:** The LVTLL inputs on the Si5320 device have an internal pulldown mechanism that causes these inputs to default to a logic low state if the input is not driven from an external source.				

Table 13. Si5320 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
A4–8, B5, B8	RSVD_NC		LVTTL	**Reserved—No Connect.** This pin must be left unconnected for normal operation.
C2	VSEL33	I*	LVTTL	**Select 3.3 V V_{DD} Supply.** This is an enable pin for the internal regulator. To enable the regulator, connect this pin to the V_{DD33} pins.
D3–D5, E3–E5	V_{DD33}	V_{DD}	Supply	**3.3 V Supply.** 3.3 V power is applied to the V_{DD33} pins. Typical supply bypassing/decoupling for this configuration is indicated in the typical application diagram for 3.3 V supply operation.
D6, D7, E6, E7, F3–F7	V_{DD25}	V_{DD}	Supply	**2.5 V Supply.** These pins provide a means of connecting the compensation network for the on-chip regulator.
C3–C7, E2, F2, G2–G8	GND	GND	Supply	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of the device.
H2	REXT	I	Analog	**External Biasing Resistor.** Used by on-chip circuitry to establish bias currents within the device. This pin must be connected to GND through a 10 kΩ (1%) resistor.
D2	DBLBW	I*	LVTTL	**Double Bandwidth.** Active high input to boost the selected bandwidth 2x. When this pin is high, the loop filter bandwidth selected on BWSEL[1:0] is doubled. When this pin is high, FXDDELAY must also be high and FEC[1:0] must be 00.
B6 B7 C8	MODE[2] MODE[1] MODE[0]	I	LVTTL	**Mode Select.** Used to enable output phase adjust mode (output phase adjust register control).
***Note:** The LVTLL inputs on the Si5320 device have an internal pulldown mechanism that causes these inputs to default to a logic low state if the input is not driven from an external source.				

Table 13. Si5320 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
B4	FXDDELAY	I*	LVTTL	**Fixed delay mode.** Set high to disable hitless recovery from digital hold mode. This configuration is useful in applications that require a known or constant input-to-output phase relationship. When this pin is high, hitless switching from digital hold mode back to a valid clock input is disabled. When switching from digital hold mode to a valid clock input with FXDDELAY high, the clock output changes as necessary to re-establish the initial/ default input-to-output phase relationship that is established after powerup or reset. The rate of change is determined by the setting of BWSEL[1:0]. When this pin is low, hitless switching from digital hold mode back to a valid clock input is enabled. When switching from digital hold mode to a valid clock input with FXDDELAY low, the device enables "phase build out" to absorb the phase difference between the clock output and the clock input so that the phase change at the clock output is minimized. In this case, the input-to-output phase relationship following the transition out of digital hold mode is determined by the phase relationship at the time that switching occurs. **Note:** FXDDELAY should remain at a static high or static low level during normal operation. Transitions on this pin are allowed only when the RSTN/CAL pin is low. FXDDELAY must be set high when DBLBW is set high. The state of FXDELAY cannot be changed when the device is in the output phase adjust mode. Instead, the device retains the last valid state of FXDDELAY and uses this setting for the duration of time the device is in output phase adjust mode.
	$t_{IN}[0]$			**Envelope Select (Register Read Out).** This pin must be held high to read the value of the phase detector DAC (output phase adjust register control).
	$t_{IN}[0]$			**Serial Clock Input (Output Phase INC/DEC).** A rising edge on this pin drives serial data from $t_{IN}[1]$ into the phase adjust registers (output phase adjust register control).

***Note:** The LVTLL inputs on the Si5320 device have an internal pulldown mechanism that causes these inputs to default to a logic low state if the input is not driven from an external source.

Table 13. Si5320 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
B3	DECDELAY	I	LVTTL	**Decrement Output Phase Delay** The INCDELAY and DECDELAY pins can adjust the phase of the Si5320 clock output. Adjustment is accomplished by driving a pulse (a transition from low to high and then back to low) into one of the pins while the other pin is held at a logic low level. Each pulse on the DECDELAY pin removes a fixed delay from the Si5320's clock output. The fixed delay time is equal to twice the period of the 622 MHz output clock ($t_{DELAY} = 2/f_{o\_622}$). The frequency of the 622 MHz output clock (f_{o_622}) is nominally 32x the frequency of the input clock. The frequency of the 622 MHz output clock (fo_622) is scaled additionally according to the setting of the FEC[1:0] pins. When the phase of the Si5320 clock output is adjusted using the INCDELAY and/or DECDELAY pins, the output clock moves to its new phase setting at a rate of change that is determined by the setting of the BWSEL[1:0] pins (output phase adjust pin control).
	t_{IN}[1]			**Serial Data Input (Output Phase INC/DEC).** Input pin for transferring data into the phase adjust registers (output phase adjust register control).

***Note:** The LVTLL inputs on the Si5320 device have an internal pulldown mechanism that causes these inputs to default to a logic low state if the input is not driven from an external source.

Table 13. Si5320 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
B2	INCDELAY/ $t_{IN}[2]$ $t_{IN}[2]$	I	LVTTL	**Increment Output Phase Delay.** The INCDELAY and DECDELAY pins can adjust the phase of the Si5320 clock output. Adjustment is accomplished by driving a pulse (a transition from low to high and then back to low) into one of the pins while the other pin is held at a logic low level. Each pulse on the INCDELAY pin adds a fixed delay to the Si5320's clock output. The fixed delay time is equal to twice the period of the 622 MHz output clock ($t_{DELAY} = 2/f_{o\_622}$). The frequency of the 622 MHz output clock (f_{o_622}) is nominally 32x the frequency of the input clock. The frequency of the 622 MHz output clock (fo_622) is scaled additionally according to the setting of the FEC[1:0] pins. When the phase of the Si5320 clock output is adjusted using the INCDELAY and/or DECDELAY pins, the output clock moves to its new phase setting at a rate of change that is determined by the setting of the BWSEL[1:0] pins (output phase adjust pin control). INCDELAY is ignored when the Si5320 is operating in digital hold (DH) mode. **Read Register (Register Read Out).** This pin should be held high to shift the phase detector DAC values out of the device (output phase adjust register control). **Load Phase Offset (Output Phase INC/DEC).** A rising edge on this signal loads data from the phase adjust registers into the phase offset circuitry (output phase adjust register control).
A6	$t_{OUT}[0]$	O	LVTTL	**Serial Clock Output (Register Read Out).** A rising edge on this pin shifts data from the device registers to the serial data output pin ($t_{OUT}[1]$) (output phase adjust register control).
A5	$t_{OUT}[1]$	O	LVTTL	**Serial Data Output (Register Read Out).** Output pin for transferring data out of the device registers (output phase adjust register control).

***Note:** The LVTLL inputs on the Si5320 device have an internal pulldown mechanism that causes these inputs to default to a logic low state if the input is not driven from an external source.

5. Ordering Guide

Part Number	Package	Temperature Range
Si5320-G-XC3	63-Ball CBGA (Prior Revision) RoHS-5	–40 to 85 °C
Si5320-H-XL3	63-Ball PBGA (Current Revision) RoHS-5	–40 to 85 °C
Si5320-H-ZL3	63-Ball PBGA (Current Revision) RoHS-6	–40 to 85 °C

6. Package Outline

Figure 14 illustrates the package details for the Si5320-XC3. Table 14 lists the values for the dimensions shown in the illustration.

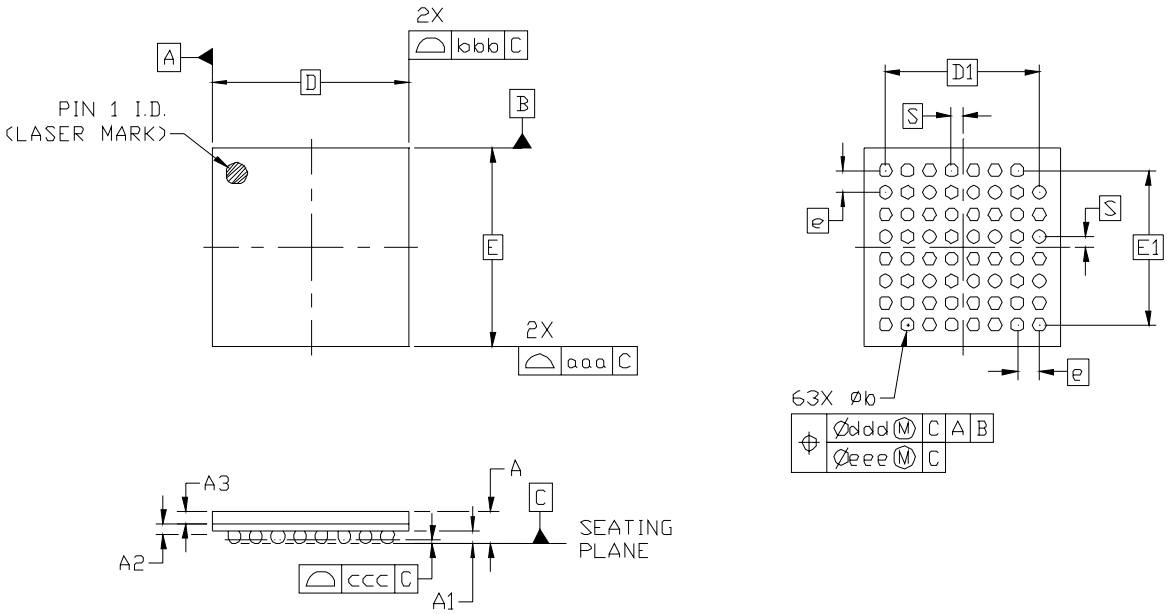


Figure 14. 63-Ball Plastic Ball Grid Array (PBGA)

Table 14. Package Diagram Dimensions (mm)

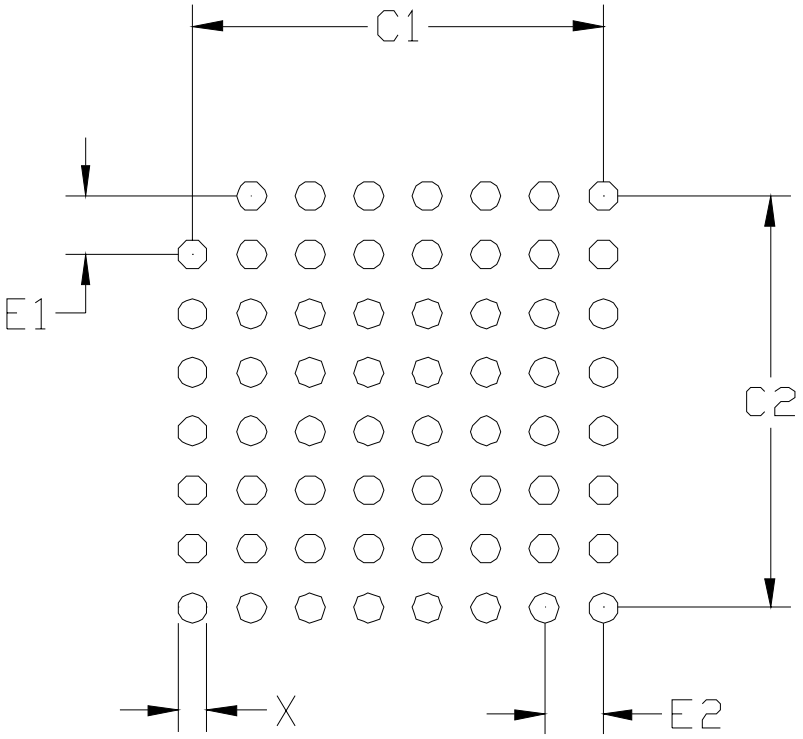
Symbol	Min	Nom	Max
A	1.24	1.41	1.58
A1	0.40	0.50	0.60
A2	0.34	0.38	0.42
A3	0.50	0.53	0.56
b	0.50	0.60	0.70
D	9.00 BSC		
E	9.00 BSC		
D1	7.00 BSC		

Symbol	Min	Nom	Max
E1	7.00 BSC		
e	1.00 BSC		
S	0.50 BSC		
aaa	0.10		
bbb	0.10		
ccc	0.12		
ddd	0.15		
eee	0.08		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-192, variation AAB-1.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7. 9x9 mm PBGA Card Layout



Symbol	Min	Nom	Max
X	0.40	0.45	0.50
C1		7.00	
C2		7.00	
E1		1.00	
E2		1.00	

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 2.3 to Revision 2.4

- Updated Figure 5, “Output Phase Adjust Timing Diagrams (Register Control),” on page 6.
- Added specification for Register Read Out READ Clock High in Table 3, “AC Characteristics,” on page 8.
- Updated output phase increment/decrement example on page 22.
- Updated "6. Package Outline" on page 37.

Revision 2.4 to Revision 2.5

- Table 11 on page 21 updated.
- Table 12 on page 22 updated.
- "3.7.2. Output Phase Increment/Decrement" on page 22 updated.

Revision 2.5 to Revision 2.6

- Corrected pin assignments in Table 11, “Output Phase Adjust Control Pins,” on page 21.

Revision 2.6 to Revision 2.7

- Updated "5. Ordering Guide" on page 36.
- Updated "6. Package Outline" on page 37.
- Updated "7. 9x9 mm PBGA Card Layout" on page 38.

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