AT&T Microelectronics

T7504 and T5504 Quad PCM Codecs with Filters

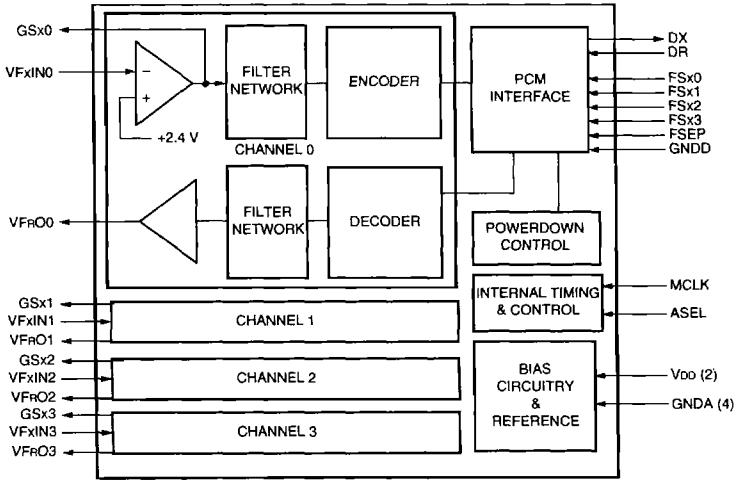
Features

- +5 V only
- Low-power, latch-up-free CMOS technology
  — 37 mW/channel typical operating power dissipation
  — 1 mW/channel typical powerdown dissipation
- Automatic master clock frequency selection
  — 2.048 MHz or 4.096 MHz
- On-chip sample and hold, autozero, and precision voltage reference
- Differential architecture for high noise immunity and power supply rejection
- Flexible time-slotted PCM interface
  — 2.048 MHz or 4.096 MHz data rate
- Meets or exceeds D3/D4 (as per AT&T PUB43801) and CCITT G.711—G.714 requirements
- Operating temperature range: –40 °C to +85 °C
- μ-law/A-law companding selectable

Description

The T7504 and T5504 devices are single-chip, four-channel μ-law/A-law PCM codecs with filters. These integrated circuits provide analog-to-digital and digital-to-analog conversion. They provide the transmit and receive filtering necessary to interface a voice telephone circuit to a time-division multiplexed system. These devices are packaged in both 28-pin DIPs and 28-pin PLCCs.

The T5504 differs from the T7504 in its timing mode. The T5504 operates in the nondelay timing mode (digital data valid when frame sync goes high), and the T7504 operates in the delayed timing mode (digital data is valid one clock cycle after frame sync goes high) (see Figures 5—8).



5-3579C

Figure 1. Block Diagram

Functional Description

Four channels of PCM data input and output are passed through only two ports, Dx and D_R, so some type of time-slot assignment is necessary. The scheme used here is to utilize timing modes of 32 or 64 time slots corresponding to master clock frequencies of either 2.048 MHz or 4.096 MHz, respectively. Each device has four transmit frame sync (FSx) inputs, one for each channel. During a single 125 µs frame, each transmit frame sync input is supplied a single pulse. The timing of the pulse indicates the beginning of the time slot during which the data for that channel is clocked out of the device. During a frame, transmit frame sync pulses must be separated from each other by one or more time slots. A channel is placed in a standby (low-power) mode if its FSx input has been low for 500 µs.

There is a single frame sync separation input (FSEP). The number of negative clock edges minus one that occur while FSEP is high is the delay (in clock periods) that is placed between the rising edge of a transmit frame sign bit and the falling edge used by the receiver to sample the sign bit. There must always be a pulse on the FSEP input since this input provides the 8 kHz signal required to maintain internal timing. If the FSEP pulse is one clock period or less, the device makes the transmit edges and receive sampling edges one half clock period apart. The entire device is placed in a powerdown mode if FSEP remains low for 500 µs.

Time slot zero is defined as starting on the first rising MCLK edge after FSEP = "1" is detected by a negative MCLK edge. In the T7504, MCLK negative-going edges that detect the start of FSEP and FSxN must be integer multiples of eight MCLK periods apart (zero multiples are allowed). Since FSEP is assumed to define time slot 0, the number of multiples separating FSxN and FSEP is the time-slot number. In the T5504, FSxN for time slot 0 nominally starts on the MCLK positive edge following the negative edge which detects FSEP.

The frequency of the master clock must be either 2.048 MHz or 4.096 MHz. Internal circuitry determines the master clock frequency during the powerup reset interval.

Powerdown is not guaranteed if MCLK is lost unless the device is already in the powerdown mode due to FSEP low for at least 500 µs.

The analog input section in Figure 2 includes an on-chip op amp that is used in conjunction with external, user-supplied resistors to vary encoder passband gain. The load impedance to ground at the GSx outputs should be greater than 10 kΩ in parallel with less than 50 pF. The input signal at VFxIN should be ac coupled. For best performance, the maximum gain of this op amp should be limited to 20 dB or less.

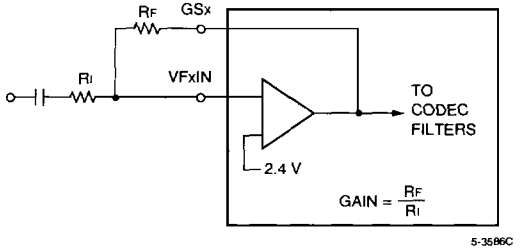
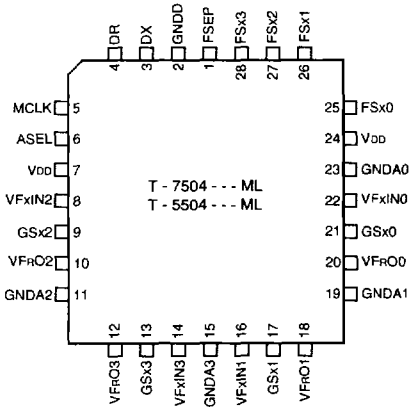
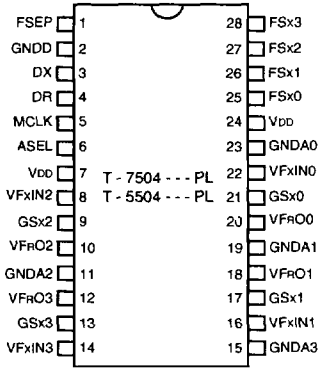


Figure 2. Typical Analog Input Section

Pin Information





5-3580B

Figure 3. Pin Diagrams

Pin Information

Table 1. Pin Descriptions

Symbol	Pin	Type*	Name/Function
VFxIN3 VFxIN2 VFxIN1 VFxIN0	14 8 16 22	I	**Voice Frequency Transmitter Input.** Analog inverting input to the uncommitted operational amplifier at the transmit filter input. Connect the signal to be digitized to this pin through a resistor R_I (see Figure 2).
GSx3 GSx2 GSx1 GSx0	13 9 17 21	O	**Gain Set for Transmitter.** Output of the transmit uncommitted operational amplifier. The pin is the input to the transmit differential filters. Connect the pin to its corresponding VFxIN through a resistor R_F (see Figure 2).
VFRO3 VFRO2 VFRO1 VFRO0	12 10 18 20	O	**Voice Frequency Receiver Output.** This pin can drive 2000 Ω (or greater) loads.
V_{DD} [1:0]	7, 24	—	**+5 V Analog Power Supplies.** Both pins must be connected on the circuit board. Each pin should be bypassed to ground with at least 0.1 µF of capacitance as close to the device as possible.
GNDA3 GNDA2 GNDA1 GNDA0	15 11 19 23	—	**Analog Grounds.** All ground pins must be connected on the circuit board.
D_R	4	I	**Receive PCM Data Input.** The data on this pin is shifted into the device on the falling edges of MCLK. Data is only entered for valid time slots as defined by the relationship of the pulses on the FSx inputs and the pulse on the FSEP input.
Dx	3	O	**Transmit PCM Data Output.** This pin remains in the high-impedance state except during active transmit time slots. An active transmit time slot is defined as one in which a pulse is present on one of the FSx inputs. Data is shifted out on the rising edge of MCLK.
MCLK	5	I	**Master Clock Input.** The frequency must be 2.048 MHz or 4.096 MHz. This clock serves as the bit clock for all PCM data transfer. A 40% to 60% duty cycle is required.
GNDD	2	—	**Digital Ground.** Ground connection for the digital circuitry. All ground pins must be connected on the circuit board.
FSx3 FSx2 FSx1 FSx0	28 27 26 25	I^d	**Transmit Frame Sync.** This signal is an edge trigger and must be high for a minimum of one MCLK cycle. This signal must be derived from MCLK. The division ratio is 1:256 or 1:512 (FSx:MCLK). Each FSx input must have a pulse present at the start of the desired active output time slot. Pulses on the various FSx inputs must be separated by one or more integer multiples of time slots. An internal pull-down device is included on each FSx.
ASEL	6	I^d	**A-Law/µ-Law Select.** A logic low selects µ-law coding. A logic high selects A-law coding. A pull-down device is included.
FSEP	1	I	**Frame Sync Separation.** The pulse width of this 8 kHz signal defines the timing offset between the transmit and receive frames. Internally generated receive frame sync pulses are delayed from the corresponding transmit frame sync pulse rising edge by one less than the FSEP pulse width in negative MCLK edges. If the pulse width is one MCLK period or less, the transmit and receive frame sync are made coincident. Loss of FSEP causes the device to powerdown. If the master clock frequency is 2.048 MHz or 4.096 MHz, delays of 255 or 511 clock pulses are not allowed, respectively. Timing relationships between FSEP, FSxN, and time slot 0 are given in Figures 5—8.

* I^d A pull-down device is included on this lead.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Units
Storage Temperature Range	T_{stg}	–55	150	°C
Power Supply Voltage	V_{DD}	—	6.5	V
Voltage on Any Pin with Respect to Ground	—	–0.5	0.5 + V_{DD}	V
Maximum Power Dissipation (package limit)	P_{DISS}	—	600	mW

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

HBM ESD Threshold Voltage	
Device	**Rating**
T7504	>2000 V
T5504	>2000 V

Electrical Characteristics

Specifications apply for T_A = –40 °C to + 85 °C, V_{DD} = 5 V ± 5%, MCLK = either 2.048 MHz or 4.096 MHz, and GND = 0 V, unless otherwise noted.

dc Characteristics

Table 2. Digital Interface

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	All digital inputs	—	—	0.8	V
Input High Voltage	V_{IH}	All digital inputs	2.0	—	—	V
Output Low Voltage	V_{OL}	Dx, I_L = 3.2 mA	—	—	0.4	V
Output High Voltage	V_{OH}	Dx, I_L = –3.2 mA	2.4	—	—	V
		Dx, I_L = –320 µA	3.5	—	—	V
Input Current, Pins without Pull-down	I_I	Any digital input GND < V_{IN} < V_{DD}	–10	—	10	µA
Input Current, Pins with Pull-down	I_I	Any digital input GND < V_{IN} < V_{DD}	—	—	150	µA
Output Current in High-impedance State	I_{OZ}	Dx	–30	—	30	µA
Input Capacitance	C_I	—	—	—	5	pF

Electrical Characteristics (continued)

dc Characteristics

Table 3. Power Dissipation

Power measurements are made at MCLK = 4.096 MHz, outputs unloaded.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Powerdown Current	I_{DDO}	MCLK present, FSx[3:0] = 0.4 V, FSEP = 0.4 V	—	0.2	1	mA
Powerup Current	I_{DD1}	MCLK, FSx[3:0], FSEP present	—	30	50	mA
Standby Current	I_{DDS}	MCLK, FSEP present; FSx[3:0] = 0.4 V	—	6	10	mA

Transmission Characteristics

Table 4. Analog Interface

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Resistance, VFxIN	R_{VFXI}	0.25 V < VFxI < 4.75 V	1.0	—	—	MΩ
Input Leakage Current, VFxIN	I_{BVFXI}	0.25 V < VFxI < 4.75 V	—	—	2.4	µA
dc Open-loop Voltage Gain, GSx	A_{VOL}	—	5000	—	—	—
Open-loop Unity Gain Bandwidth, GSx	f_O	—	1	3	—	MHz
Load Capacitance, GSx	C_{LX1}	—	—	—	50	pF
Load Resistance, GSx	R_{LX1}	—	10	—	—	kΩ
Input Voltage, VFxIN	V_{IX}	Relative to ground	2.3	2.4	2.5	V
Load Resistance, VFRO	R_{LVFRO}	—	2000	—	—	Ω
Load Capacitance, VFRO	C_{LVFRO}	—	—	—	100	pF
Output Resistance, VFRO	RO_{VFRO}	0 dBm0, 1020 Hz PCM code applied to D_R	—	—	20	Ω
		Partial powerdown FSx = "0" for channel under test	3000	—	10000	Ω
Output Voltage, VFRO	V_{OR}	Alternating ± zero µ-law PCM code applied to D_R	2.3	2.4	2.5	V
Output Voltage, VFRO, Standby	VO_{RPD}	FSx[3:0] = 0.4 V, FSEP = active, no load	2.15	2.4	2.65	V
Output Leakage Current, VFRO, Powerdown	IO_{VFRO}	FSEP = 0.4 V	-30	—	30	µA
Output Voltage Swing, VFRO	V_{SWR}	RL = 2000 Ω	3.2	—	—	VPP

Transmission Characteristics (continued)

ac Transmission Characteristics

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave; the input amplifier is set for unity gain. The digital input is a PCM bit stream equivalent to that obtained by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. The output level is sin(x)/x-corrected.

Table 5. Absolute Gain

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Encoder Milliwatt Response (transmit gain tolerance)	EmW	Signal input of 0.775 Vrms, μ-law or A-law	–0.25	—	0.25	dBm0
Decoder Milliwatt Response (receive gain tolerance)	DmW	Measured relative to 0.775 Vrms μ-law or A-law, PCM input of 0 dBm0 1020 Hz RL = 10 kΩ	–0.25	—	0.25	dBm0

Table 6. Gain Tracking

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Transmit Gain Tracking Error	GTx	+3 dBm0 to –37 dBm0	–0.25	—	0.25	dB
Sinusoidal Input μ-Law/A-Law		–37 dBm0 to –50 dBm0	–0.50	—	0.50	dB
Receive Gain Tracking Error	GTR	+3 dBm0 to –37 dBm0	–0.25	—	0.25	dB
Sinusoidal Input μ-Law/A-Law		–37 dBm0 to –50 dBm0	–0.50	—	0.50	dB

Table 7. Distortion

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Transmit Signal to Distortion	SDx	μ-law 3 dBm0 ≤ VFxI ≤ –30 dBm0	36	—	—	dB
		A-law 3 dBm0 ≤ VFxI ≤ –30 dBm0	35	—	—	dB
		μ-law –30 dBm0 ≤ VFxI ≤ –40 dBm0	30	—	—	dB
		A-law –30 dBm0 ≤ VFxI ≤ –40 dBm0	29	—	—	dB
		μ-law –40 dBm0 ≤ VFxI ≤ –45 dBm0	25	—	—	dB
		A-law –40 dBm0 ≤ VFxI ≤ –45 dBm0	25	—	—	dB
Receive Signal to Distortion	SDR	μ-law 3 dBm0 ≤ VFRO ≤ –30 dBm0	36	—	—	dB
		A-law 3 dBm0 ≤ VFRO ≤ –30 dBm0	35	—	—	dB
		μ-law –30 dBm0 ≤ VFRO ≤ –40 dBm0	30	—	—	dB
		A-law –30 dBm0 ≤ VFRO ≤ –40 dBm0	29	—	—	dB
		μ-law –40 dBm0 ≤ VFRO ≤ –45 dBm0	25	—	—	dB
		A-law –40 dBm0 ≤ VFRO ≤ –45 dBm0	25	—	—	dB
Single Frequency Distortion, Transmit	SFDx	200 Hz—3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz	—	—	–38	dBm0
Single Frequency Distortion, Receive	SFDR	200 Hz—3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz	—	—	–40	dBm0
Intermodulation Distortion	IMD	Transmit or receive, two frequencies in the range (300 Hz—3400 Hz) at –6 dBm0	—	—	–42	dBm0

Transmission Characteristics (continued)

ac Transmission Characteristics (continued)

Table 8. Envelope Delay Distortion

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Tx Delay, Absolute*	D_{XA}	f = 1600 Hz	—	—	175 to 425	µs
Tx Delay, Relative to 1600 Hz	D_{XR}	f = 500 Hz—600 Hz	—	—	220	µs
		f = 600 Hz—800 Hz	—	—	145	µs
		f = 800 Hz—1000 Hz	—	—	75	µs
		f = 1000 Hz—1600 Hz	—	—	40	µs
		f = 1600 Hz—2600 Hz	—	—	75	µs
		f = 2600 Hz—2800 Hz	—	—	105	µs
		f = 2800 Hz—3000 Hz	—	—	155	µs
Rx Delay, Absolute*	D_{RA}	f = 1600 Hz	—	—	150 to 405	µs
Rx Delay, Relative to 1600 Hz	D_{RR}	f = 500 Hz—1000 Hz	-40	—	—	µs
		f = 1000 Hz—1600 Hz	-30	—	—	µs
		f = 1600 Hz—2600 Hz	—	—	90	µs
		f = 2600 Hz—2800 Hz	—	—	125	µs
		f = 2800 Hz—3000 Hz	—	—	175	µs
Round Trip Delay, Absolute*	D_{RTA}	Any time slot/channel to any time slot/channel f = 1600 Hz	—	—	325 to 650	µs

* Varies as a function of time slots chosen.

Overload Compression

Figure 4 shows the region of operation for encoder signal levels above the reference input power (0 dBm0).

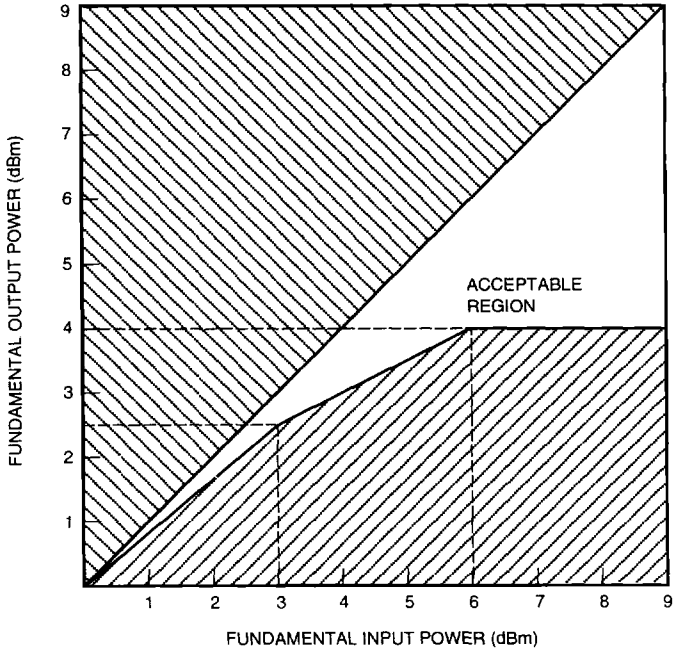


Figure 4. Overload Compression

Transmission Characteristics (continued)

ac Transmission Characteristics (continued)

Table 9. Noise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Transmit Noise μ-Law	N_{XC}	—	—	—	18	dBrnC0
		Input amplifier gain = 20 dB	—	—	19	dBrnC0
Transmit Noise A-Law	N_{XP}	—	—	—	–68	dBm0p
Receive Noise μ-Law	N_{RC}	PCM code is alternating positive and negative zero	—	—	13	dBrnC0
Receive Noise A-Law	N_{RP}	PCM code is A-law positive one	—	—	–75	dBm0p
Noise, Single Frequency f = 0 kHz—100 kHz	N_{RS}	VFxIN = 0 Vrms, measurement at VF_{RO}, D_R = Dx	—	—	–53	dBm0
Power Supply Rejection Transmit	PSRx	V_{DD} = 5.0 V_{dc} + 100 mVrms:				
		f = 0 kHz—4 kHz	36	—	—	dB
		f = 4 kHz—50 kHz	30	—	—	dB
Power Supply Rejection Receive	PSRx	PCM code is positive one LSB. V_{DD} = 5.0 V_{dc} + 100 mVrms:				
		f = 0 kHz—4 kHz	36	—	—	dB
		f = 4 kHz—25 kHz	40	—	—	dB
		f = 25 kHz—50 kHz	30	—	—	dB
Spurious Out-of-Band Signals at VF_{RO} Relative to Input	SOS	0 dBm0, 300 Hz—3400 Hz input PCM code applied:				
		4600 Hz—7600 Hz	—	—	–30	dB
		7600 Hz—8400 Hz	—	—	–40	dB
		8400 Hz—50 kHz	—	—	–30	dB

Table 10. Receive Gain Relative to Gain at 1.02 kHz

Frequency (Hz)	Min	Typ	Max	Unit
Below 3000	–0.150	±0.04	0.150	dB
3140	–0.570	±0.04	0.150	dB
3380	–0.885	–0.58	0.010	dB
3860	—	–10.7	–9.4	dB
4600 and above	—	—	–28	dB

Table 11. Transmit Gain Relative to Gain at 1.02 kHz

Frequency (Hz)	Min	Typ	Max	Unit
16.67	—	–50	–30	dB
40	—	–34	–26	dB
50	—	–36	–30	dB
60	—	–50	–30	dB
200	–1.8	–0.5	0	dB
300 to 3000	–0.150	±0.04	0.150	dB
3140	–0.570	±0.04	0.150	dB
3380	–0.885	–0.58	0.010	dB
3860	—	–10.7	–9.4	dB
4600 and above	—	—	–32	dB

Transmission Characteristics (continued)

ac Transmission Characteristics (continued)

Table 12. Interchannel Crosstalk (Between Channels) R_F = ≤ 200 kΩ (See Note.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Transmit to Receive Crosstalk 0 dBm0 Transmit Levels	CT_{XX-RY}	f = 300 Hz—3400 Hz idle PCM code for channel under test; 0 dBm0 into any other single channel VFxIN	—	—	–75	dB
Receive to Transmit Crosstalk 0 dBm0 Receive Levels	CT_{RX-XY}	f = 300 Hz—3400 Hz VFxIN = 0 Vrms for channel under test; 0 dBm0 code level on any other single channel D_R	—	—	–75	dB
Transmit to Transmit Crosstalk 0 dBm0 Transmit Levels	CT_{XX-XY}	f = 300 Hz—3400 Hz 0 dBm0 applied to any single channel VFxIN except channel under test, which has VFxIN = 0 Vrms	—	—	–75	dB
Receive to Receive Crosstalk 0 dBm0 Receive Levels	CT_{RX-RY}	f = 300 Hz—3400 Hz 0 dBm0 code level on any single channel D_R except channel under test which has idle code applied	—	—	–75	dB

Table 13. Intrachannel Crosstalk (Within Channels) R_F = ≤ 200 kΩ (See Note.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Transmit to Receive Crosstalk 0 dBm0 Transmit Levels	CT_{XX-RX}	f = 300 Hz—3400 Hz idle PCM code for channel under test; 0 dBm0 into VFxIN	—	—	–65	dB
Receive to Transmit Crosstalk 0 dBm0 Receive Levels	CT_{RX-XX}	f = 300 Hz—3400 Hz VFxIN = 0 Vrms for channel under test; 0 dBm0 code level on D_R	—	—	–65	dB

Note: For Tables 12 and 13, crosstalk into the transmit channels (VFxIN) can be significantly affected by parasitic capacitive feeds from GSx and VF_RO outputs. PWB layouts should be arranged to keep these parasitics low. The resistor value of R_F (from GSx to VFxIN) should also be kept as low as possible (while maintaining the load on GSx above 10 kΩ per Table 4) to minimize crosstalk.

Timing Characteristics

Table 14. Clock Section (See Figures 5, 6, 7, and 8.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
tMCHMCL1	Clock Pulse Width	—	97	—	—	ns
tCDC	Duty Cycle, MC	—	40	—	60	%
tMCH1MCH2 tMCL2MCL1	Clock Rise and Fall Time	—	0	—	15	ns

Table 15. T7504 Transmit Section (See Figure 5.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
tMCHDV	Data Enabled on TS Entry	0 < CLOAD < 100 pF	0	—	60	ns
tMCHDV1	Data Delay from MC	0 < CLOAD < 100 pF	0	—	60	ns
tMCLDZ*	Data Float on TS Exit	CLOAD = 0	10	—	100	ns
tFSHMCL	Frame-sync Hold Time	—	50	—	—	ns
tMCLFSH	Frame-sync High Setup	—	50	—	—	ns
tFSLMCL	Frame-sync Low Setup	—	50	—	—	ns
tFSHFSL	Frame-sync Pulse Width	—	0.1	—	125 – tMCHMCH	µs

* Timing parameter tMCLDZ is referenced to a high-impedance state.

Table 16. T5504 Transmit Section (See Figure 7.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
tFSHDV	Data Enabled on TS Entry	0 < CLOAD < 100 pF	0	—	80	ns
tMCHDV1	Data Delay from FSx	0 < CLOAD < 100 pF	0	—	60	ns
tMCHDZ*	Data Float on TS Exit	CLOAD = 0	0	—	30	ns
tFSHMCL	Frame-sync Hold Time	—	50	—	—	ns
tMCLFSH	Frame-sync High Setup	—	50	—	—	ns
tFSLMCL	Frame-sync Low Setup	—	50	—	—	ns
tFSHFSL	Frame-sync Pulse Width	—	0.1	—	125 – tMCHMCH	µs

* Timing parameter tMCHDZ is referenced to a high-impedance state.

Timing Characteristics (continued)

Table 17. T7504 and T5504 Receive Section (See Figures 5, 6, 7, and 8.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
tDVMCL	Receive Data Setup	—	30	—	—	ns
tMCLDV	Receive Data Hold	—	15	—	—	ns
tFSHMCL	Frame Separation Hold Time	—	50	—	—	ns
tMCLSPH	Frame Separation High Setup	—	50	—	—	ns
tFSLMCL	Frame Separation Low Setup	—	50	—	—	ns

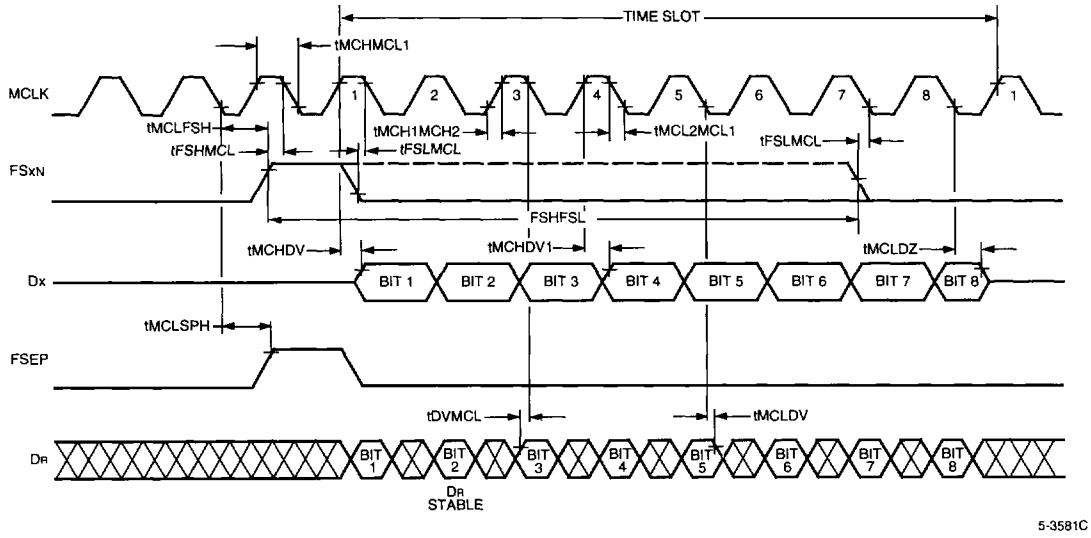


Figure 5. T7504 Transmit & Receive Timing, FSEP = 1 MCLK

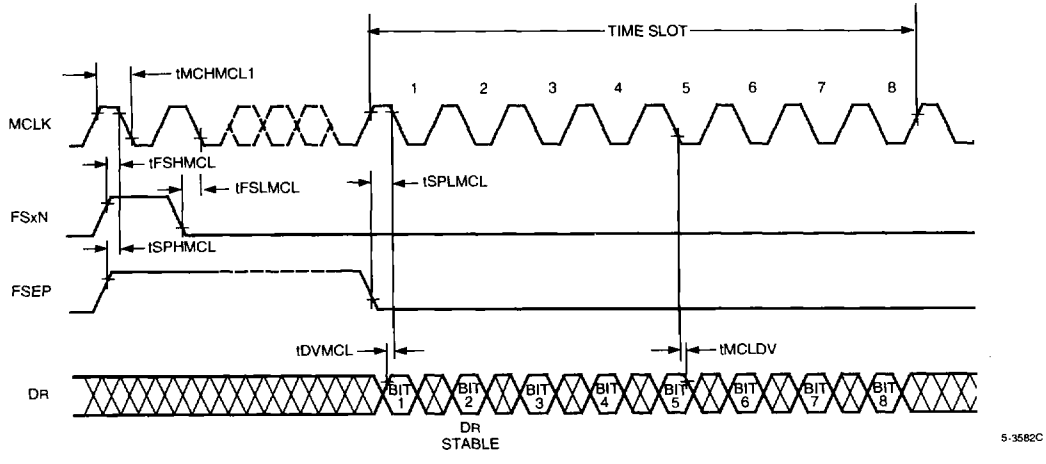


Figure 6. T7504 Receive Timing, FSEP > 1 MCLK

Timing Characteristics (continued)

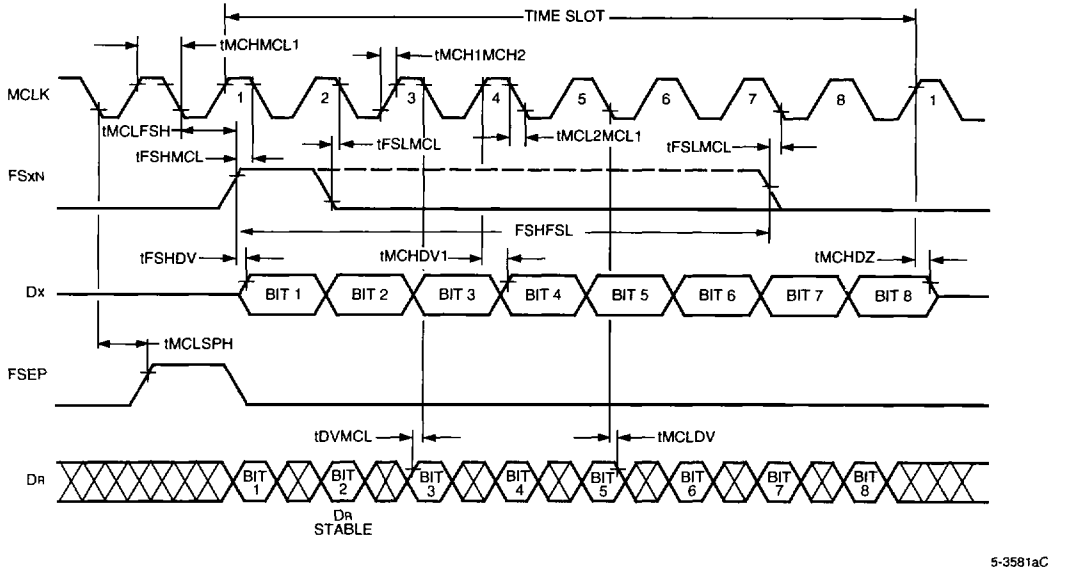


Figure 7. T5504 Transmit & Receive Timing, FSEP = 1 MCLK

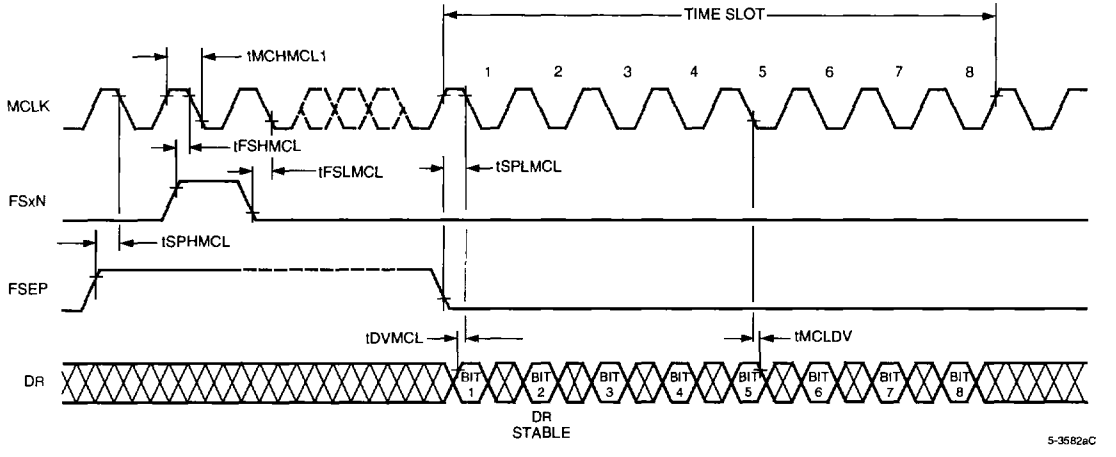


Figure 8. T5504 Receive Timing, FSEP > 1 MCLK

Timing Characteristics (continued)

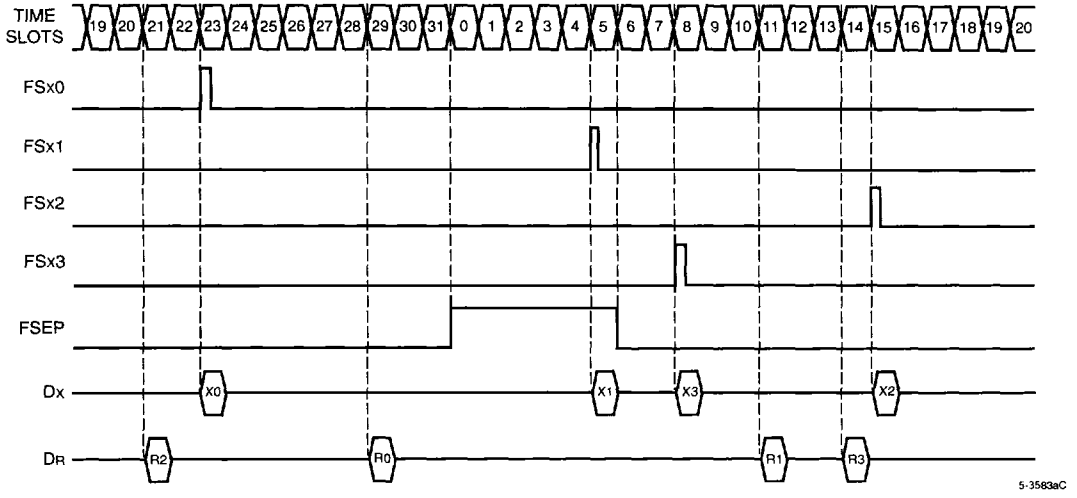


Figure 9. Typical Frame Sync Timing (2 MHz operation)

Applications

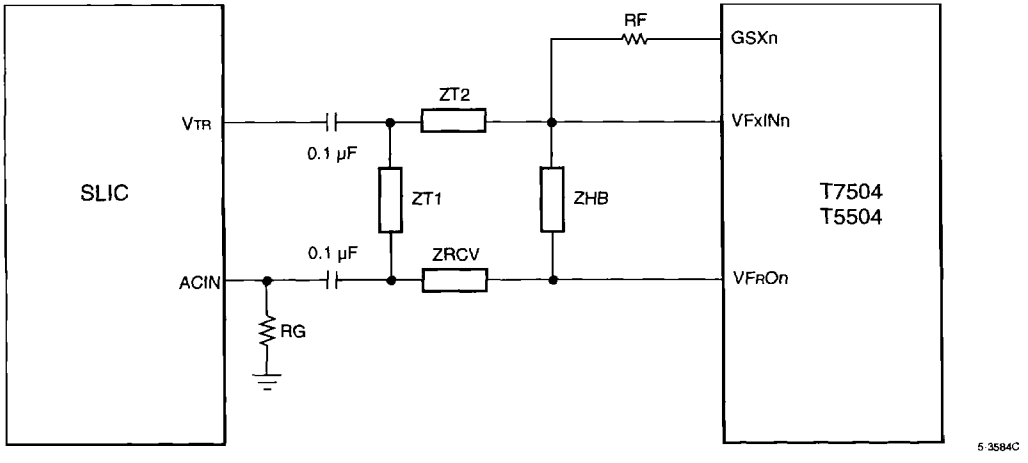
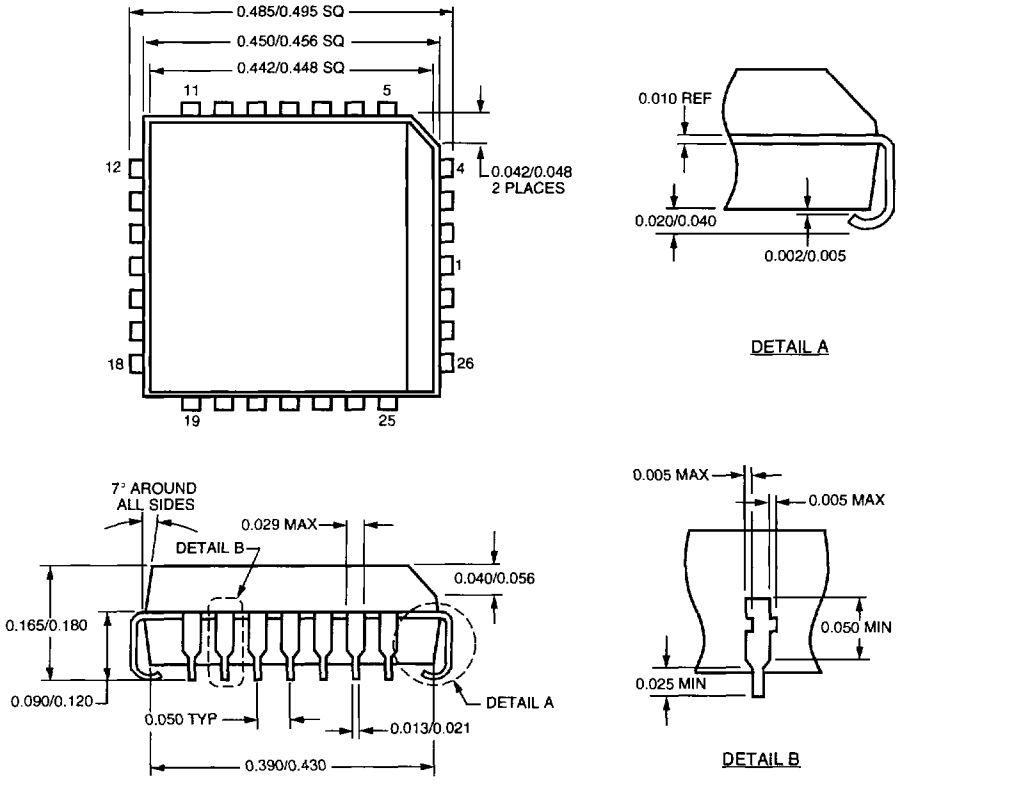


Figure 10. Typical T7504 and T5504/SLIC Interconnection

Outline Diagrams

28-Pin PLCC

Controlling dimensions are in inches.



5-2608C

Outline Diagrams (continued)

28-Pin DIP

Controlling dimensions are in inches.