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| Memory Products | |

# 48F010

## 1024K-bit FLASH memory (128K × 8)

### DESCRIPTION

The 48F010 is a 1024K bit CMOS FLASH Memory organized as 128K × 8 bits. Philips Components' 48F010 brings together the high density and cost effectiveness of U.V. EPROMs with the electrical erase, in-circuit reprogrammability and package options of EEPROMs.

The FLASH Memory cell design reduces both the time and cost required to alter code in program and data storage applications.

The 48F010's fast electrical erase and 0.5ms/byte programming is 20 times faster than reprogramming of U.V. EPROMs. Electrical erase and reprogramming make the 48F010 ideal for applications with high density requirements, but where ultraviolet erasure is either impractical or impossible.

Philips Components' FLASH memories provide users with the flexibility to alter code in all or small sections of the memory array. The memory array is divided into 128 sectors, with each sector containing 1024 bytes. Each sector can be individually erased, or the chip can be bulk erased before reprogramming.

On-chip latches and timers permit simplified microprocessor interface, freeing the microprocessor to perform other tasks once write/erase/read cycles have been initiated.

Endurance, the number of times each byte can be written, is specified at 100 cycles with an optional screen for 1000 cycles available. Electrical write/erase capability allows the 48F010 to accommodate a wide range of plastic, ceramic and surface mount packages.

### FEATURES

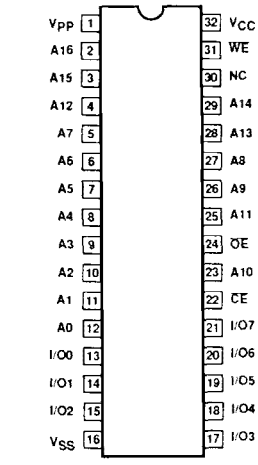
- 128K-byte FLASH erasable non-volatile memory
- Sector erase and chip erase
- Fast read access time
- Low power CMOS process
  - 40mA maximum active current
  - 100μA maximum standby current
- Input latches for writing and erasing
- 5V ± 10% $V_{CC}$, 12V ± 5% $V_{PP}$
- Ideal for low-cost program and data storage
  - Minimum 100 cycle endurance
  - Optional 1000 cycle endurance
  - Minimum 10 year data retention
- JEDEC standard byte wide pinout
  - 32-Pin Dual-in-Line Package
  - 32-Pin Plastic Leaded Chip Carrier

### PIN DESCRIPTIONS

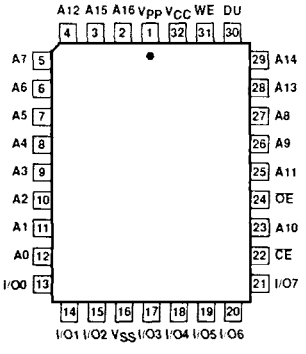
| | |
|---|---|
| A0 - A9 | Column address input |
| A10 - A16 | Row address input |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| I/O0 - I/O7 | Data Input (write)/ Output (read) |
| N.C. | No internal connection |
| $V_{PP}$ | Write/erase input voltage |
| D.U. | Don't Use |

### PIN CONFIGURATIONS

F and N Packages

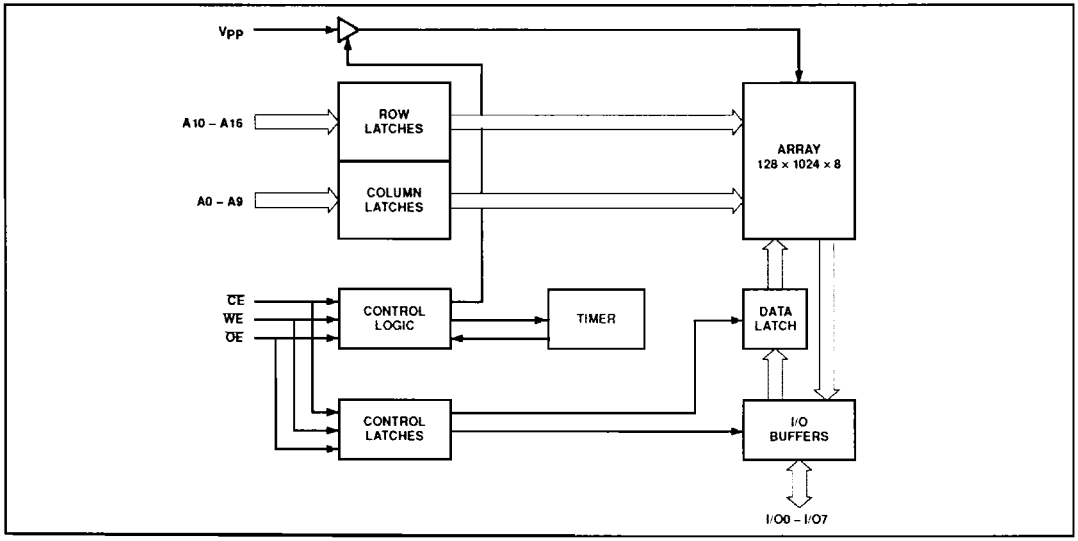



A Package



# 1024K-bit FLASH memory (128K × 8) 48F010

## BLOCK DIAGRAM




## READ

Reading is accomplished by presenting a valid address on A0 - A16 with Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) at $V_{IL}$ and Write Enable ($\overline{WE}$) at $V_{IH}$. The $V_{PP}$ pin can be at any TTL level or $V_P$ during read operations. See page 185 for additional information on AC parameters and read timing waveforms.

## ERASE AND WRITE

Erasing and writing of the 48F010 can only be accomplished when $V_{PP} = V_P$. Latches on address, data and control inputs permit erasing and writing using normal microprocessor bus timing. Address inputs are latched on the falling edge of Write Enable or Chip Enable, whichever is later, while data inputs are latched on the rising edge of Write Enable or Chip Enable, whichever is earlier. All control pins are noise protected; a pulse of less than 20ns will not initiate a write or erase. In addition, Chip Enable, Output Enable and Write Enable must be in the proper state to initiate a write or erase. Timing diagrams depict Write Enable controlled writes; the timing also applies to Chip Enable controlled writes.

## SECTOR ERASE

Sector erase changes all bits in a sector of the array to a logical "1". It requires that the $V_{PP}$ pin be brought to a high voltage and a write cycle performed. The sector to be erased is defined by address inputs A10 through A16. The data inputs must be all "1"s to begin the erase. Following a write of 'FF', the part will wait for time $t_{ABORT}$ to allow aborting the erase by writing again. This permits recovering from an unintentional sector erase if, for example, in loading a block of data a byte of 'FF' was written. After the $t_{ABORT}$ delay, the sector erase will begin. The erase is accomplished by following the erase algorithm in Figure 2. $V_{PP}$ can be brought to any TTL level or left at high voltage after the erase.

## CHIP ERASE

Chip erase will change all bits in the memory to a logical "1". The 48F010 uses a two-step, software controlled looping algorithm to perform the chip erase operation. Each loop requires that a chip erase select be performed prior to the start of each chip erase cycle.

## BYTE WRITE

A byte write is used to change any 1 in a byte to a 0. Individual bytes, multiple bytes or the entire memory can be written at one time. If a bit in a byte needs to be changed from a 0 to a 1, the byte must first be erased via sector or chip erase and then reprogrammed with the desired data. Any byte write operation requires that the $V_{PP}$ pin be at high voltage ($V_P$).

Data is organized in the 48F010 in a group of bytes called a sector. The memory array is divided into 128 sectors of 1024 bytes each. Individual bytes are written as part of a sector write operation. Sectors need not be written separately; the entire device or any combination of sectors can be written using the write algorithm.

The 48F010 uses a software controlled looping algorithm (Figure 1.) to perform writes and verify successful byte programming. During a byte write operation, all non "FF" bytes are incrementally written using a 75µs minimum $t_{WC}$ (**NOTE: Only non "FF" bytes can be written.**). Each byte write is automatically latched and timed on-chip, so that the microprocessor can perform other tasks once the write cycle has been initiated. Write cycle time duration can be controlled by the microprocessor, or the on-chip timer will automatically terminate $t_{WC}$ after 150µs. One write loop has been completed when all non "FF" data for all desired bytes have been written. After 7 programming loops, a read-verification cycle is performed. For any bytes which do not verify, a fill-in programming loop is performed.

Because bytes can only be written as part of a sector write, if data is to be added to a partially written sector or one or more bytes in a sector must be changed, the contents of the sectors must first be read into system RAM; the bytes can then be added to the block of data in RAM and the sector written using the sector write algorithm.

# 1024K-bit FLASH memory (128K × 8) 48F010

## HIGH VOLTAGE INPUT PROTECTION

The $V_{PP}$ pin is at a high voltage for writing and erasing. There is an absolute maximum specification which must not be exceeded, even briefly, or permanent damage may result. To minimize switching transients on this pin it is recommended to use a minimum 0.1µf decoupling capacitor with good high frequency response connected from $V_{PP}$ to ground at each device. In addition, sufficient bulk capacitance should be provided to minimize $V_{PP}$ voltage sag when a device goes from standby to a write or erase cycle.

## INTELLIGENT IDENTIFIER

The intelligent identifier provides the reading out of a binary code from a fixed ROM that will identify its manufacturer and type. This mode is functional in the 25° ± 5°C ambient temperature range. To activate this mode, the equipment must force 11.5V to 12.5V on address A9. Two bytes may then be read from the device outputs by toggling address line $A_0$ from $V_{IL}$ to $V_{IH}$. The $\overline{CE}$, $\overline{OE}$ and all other address lines must be at $V_{IL}$ during interrogation.

The identifier information for Philips Components' 48F010 FLASH Memory is as follows:

When A0 = $V_{IL}$
data is "Manufacturer" $94_{(HEX)}$

When A0 = $V_{IH}$
data is "Product" $1C_{(HEX)}$

## ORDERING INFORMATION

| DESCRIPTION | ORDER CODE | |
|---|---|---|
| | 100 CYCLE ENDURANCE | 1000 CYCLE ENDURANCE |
| 32-Pin Ceramic Dual In-Line | 48F010-20F<br>48F010-25F<br>48F010-30F | 48F010K-20F<br>48F010K-25F<br>48F010K-30F |
| 32-Pin Plastic Dual In-Line | 48F010-20N<br>48F010-25N<br>48F010-30N | 48F010K-20N<br>48F010K-25N<br>48F010K-30N |
| 32-Pin Plastic Leaded Chip Carrier | 48F010-20A<br>48F010-25A<br>48F010-30A | 48F010K-20A<br>48F010K-25A<br>48F010K-30A |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_{amb}$ | Operating temperature range | -10 to +85 | °C |
| $T_{stg}$ | Storage temperature range | -65 to +125 | °C |
| $V_I$, $V_O$ | All inputs except $V_{PP}$ and outputs with respect to $V_{SS}$ | -0.5 to +7.0 | V |
| $V_{PP}$ | $V_{PP}$ pin with respect to $V_{SS}$ | +14 | V |

**NOTES:**

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_{amb}$ | Temperature range (ambient) | 0 to +70 | °C |
| $V_{CC}$ | Supply voltage | 5.0 ± 10% | V |

## DEVICE OPERATION

| MODE | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $V_{PP}$ | A10 - A16 | A0 - A9 | D0 - D7 |
|---|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | Address | Address | $D_{OUT}$ |
| Standby | $V_{IH}$ | X | X | X | X | X | Hi-Z |
| Byte Write | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_P$ | Address | Address | $D_{IN}$ |
| Chip Erase Select | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | TTL | X | X | X |
| Chip Erase | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_P$ | X | X | 'FF' |
| Block Erase | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_P$ | Address | X | 'FF' |

## DC ELECTRICAL CHARACTERISTICS

Over the $V_{CC}$ and temperature range

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $I_{LI}$ | Input Leakage | $V_{IN}$ = 0.1V to $V_{CC}$ | | | 1.0 | µA |
| $I_{LO}$ | Output Leakage | $V_{IN}$ = 0.1V to $V_{CC}$ | | | 10 | µA |
| $V_P$ | Program/Erase Voltage | | 11.4 | | 13 | V |
| $V_{PR}$ | $V_{PP}$ Voltage during Read | | 0 | | $V_P$ | V |
| $I_{PP}$ | $V_P$ Current | | | | | |
| | Standby Mode | $\overline{CE}$ = $V_{IH}$, $V_{PP}$ = $V_{PR}$ | | | 200 | µA |
| | Read Mode | $\overline{CE}$ = $V_{IL}$, $V_{PP}$ = $V_{PR}$ | | | 200 | µA |
| | Byte Write | $V_{PP}$ = $V_P$ | | | 30 | mA |
| | Chip Erase | $V_{PP}$ = $V_P$ | | | 60 | mA |
| | Sector Erase | $V_{PP}$ = $V_P$ | | | 10 | mA |
| $I_{CC1}$ | Standby $V_{CC}$ Current | $\overline{CE}$ = $V_{CC}$ - 0.3V | | | 100 | µA |
| $I_{CC2}$ | Standby $V_{CC}$ Current | $\overline{CE}$ = $V_{IH}$ Min | | | 5 | mA |
| $I_{CC3}$ | Active $V_{CC}$ Current | $\overline{CE}$ = $V_{IL}$ | | | 40 | mA |
| $V_{IL}$ | Input Low Voltage | | -0.3 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | | 7.0 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | | 0.45 | V |
| $V_{OH1}$ | Output Level (TTL) | $I_{OH}$ = -400µA | 2.4 | | | V |
| $V_{OH2}$ | Output Level (CMOS) | $I_{OH}$ = -100µA | $V_{CC}$ - 1.0 | | | V |

## CAPACITANCE

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $C_{IN}$ | Input Capacitance[1] | $T_{amb}$ = 25°C, f = 1MHz; $V_{IN}$ = 0V | | 6 | | pF |
| $C_{OUT}$ | Output Capacitance[1] | $T_{amb}$ = 25°C, f = 1MHz; $V_{I/O}$ = 0V | | 12 | | pF |

**NOTE:**

1. This parameter is only sampled and not 100% tested.

## READ AC ELECTRICAL CHARACTERISTICS[1]

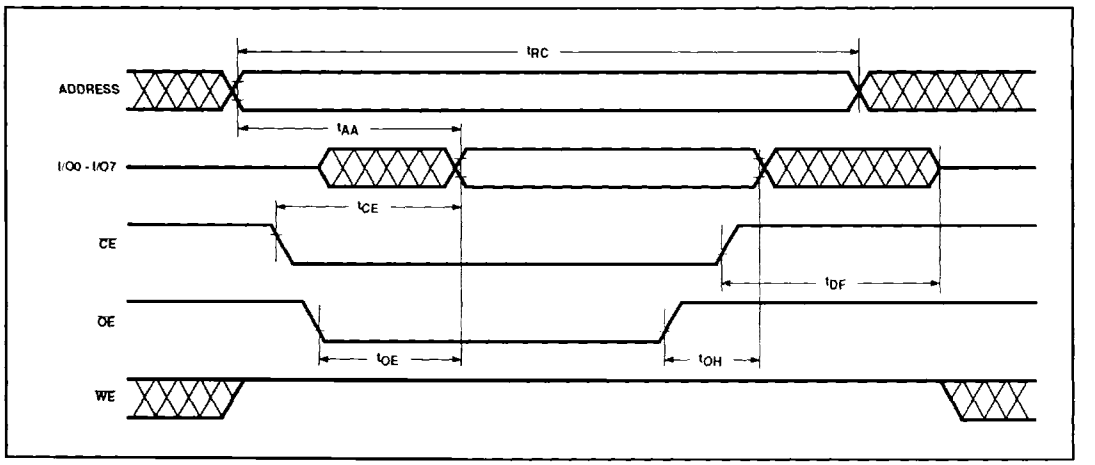
Over the $V_{CC}$ and temperature range

| SYMBOL | PARAMETER | 48F010-20 | | 48F010-25 | | 48F010-30 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{RC}$ | Read Cycle time | 200 | | 250 | | 300 | | ns |
| $t_{AA}$ | Address to data | | 200 | | 250 | | 300 | ns |
| $t_{CE}$ | $\overline{CE}$ to data | | 200 | | 250 | | 300 | ns |
| $t_{OE}$ | $\overline{OE}$ to data | | 75 | | 100 | | 150 | ns |
| $t_{DF}$ | $\overline{OE}$/$\overline{CE}$ to Data Float | | 50 | | 60 | | 100 | ns |
| $t_{OH}$ | Output Hold time | 0 | | 0 | | 0 | | ns |

**NOTE:**

1. Output load: 1 TTL gate and C (load) = 100pF
   Input Rise and Fall Times: < 20ns
   Input Pulse Levels: 0.45V to 2.4V
   Timing Measurement Reference Level: Inputs 1V and 2V
   Outputs 0.8V and 2V

## READ TIMING DIAGRAM



## BYTE WRITE AC ELECTRICAL CHARACTERISTICS[1]

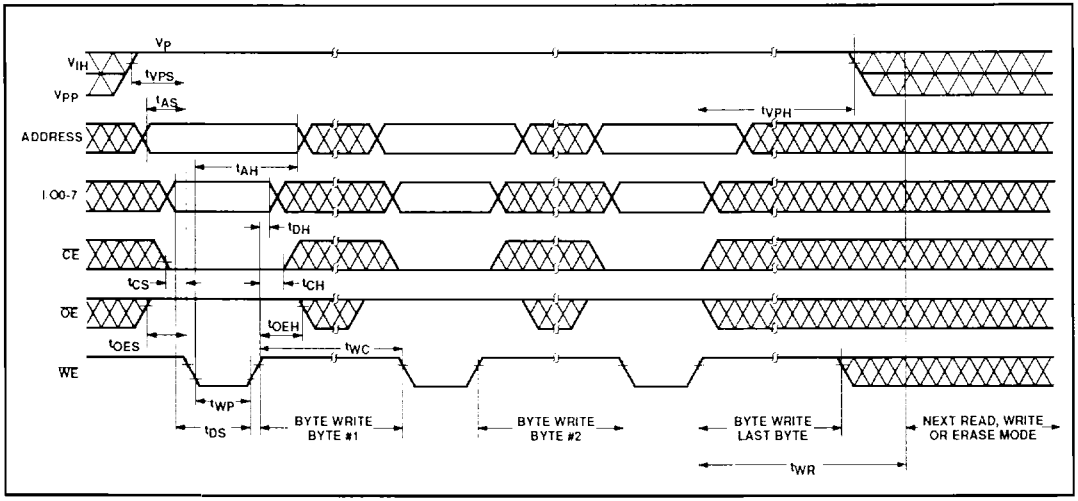
Over the $V_{CC}$ and temperature range

| SYMBOL | PARAMETER | 48F010 | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{VPS}$ | $V_{PP}$ Setup time | 2 | | µs |
| $t_{VPH}$ | $V_{PP}$ Hold time | 150 | | µs |
| $t_{CS}$ | $\overline{CE}$ Setup time | 0 | | ns |
| $t_{CH}$ | $\overline{CE}$ Hold time | 0 | | ns |
| $t_{OES}$ | $\overline{OE}$ Setup time | 10 | | ns |
| $t_{OEH}$ | $\overline{OE}$ Hold time | 10 | | ns |
| $t_{AS}$ | Address Setup time | 20 | | ns |
| $t_{AH}$ | Address Hold time | 100 | | ns |
| $t_{DS}$ | Data Setup time | 50 | | ns |
| $t_{DH}$ | Data Hold time | 0 | | ns |
| $t_{WP}$ | $\overline{WE}$ Pulse Width | 100 | | ns |
| $t_{WC}$ | Write Cycle time | 75 | | µs |
| $t_{WR}$ | Write Recovery time | | 1.5 | ms |

NOTE:

1. In AC characteristics, all inputs to the device, e.g., setup time, hold time, and cycle time, are tabulated as a minimum time; the user must provide a valid state on that input or wait for the state minimum time to assure proper operation. All outputs from the device, e.g., access time, erase time, recovery time, are tabulated as a maximum time, the device will perform the operation within the stated time

## BYTE WRITE TIMING DIAGRAM



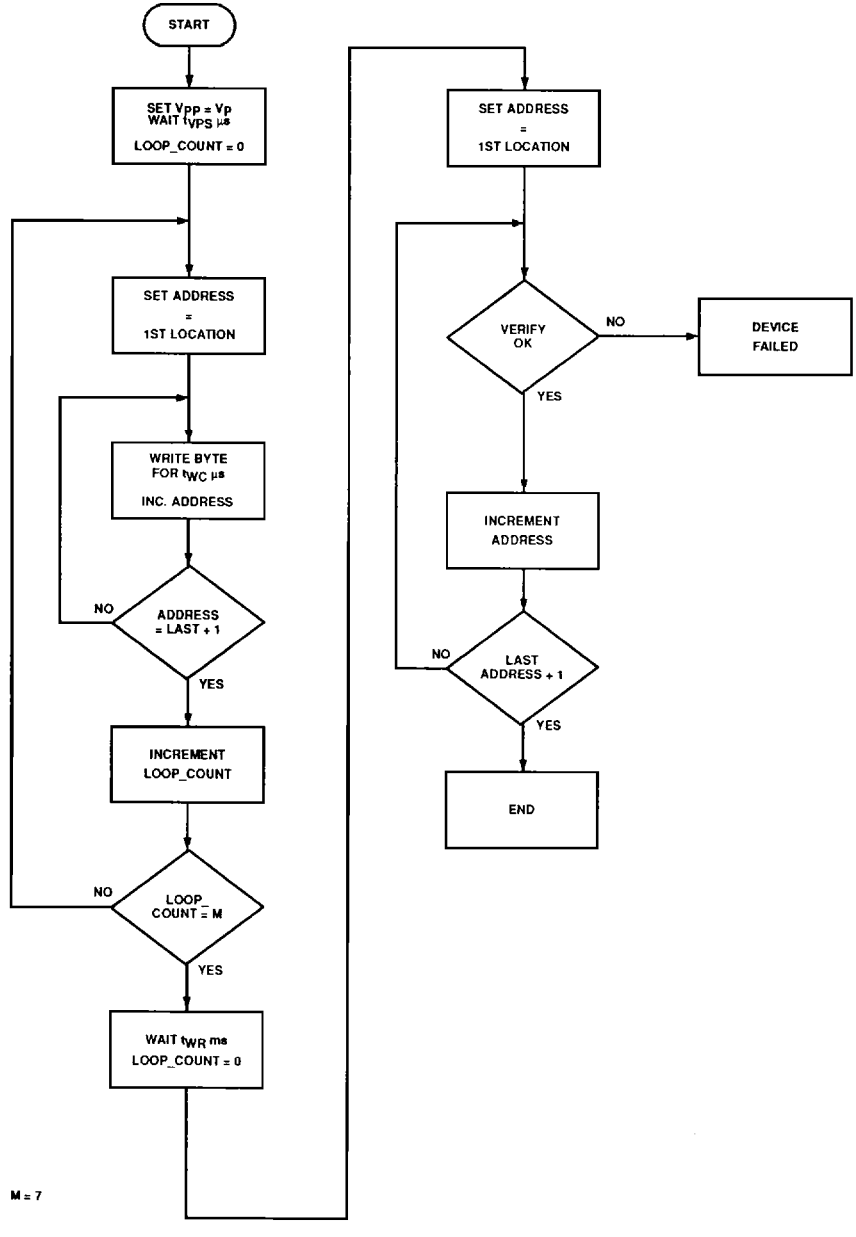


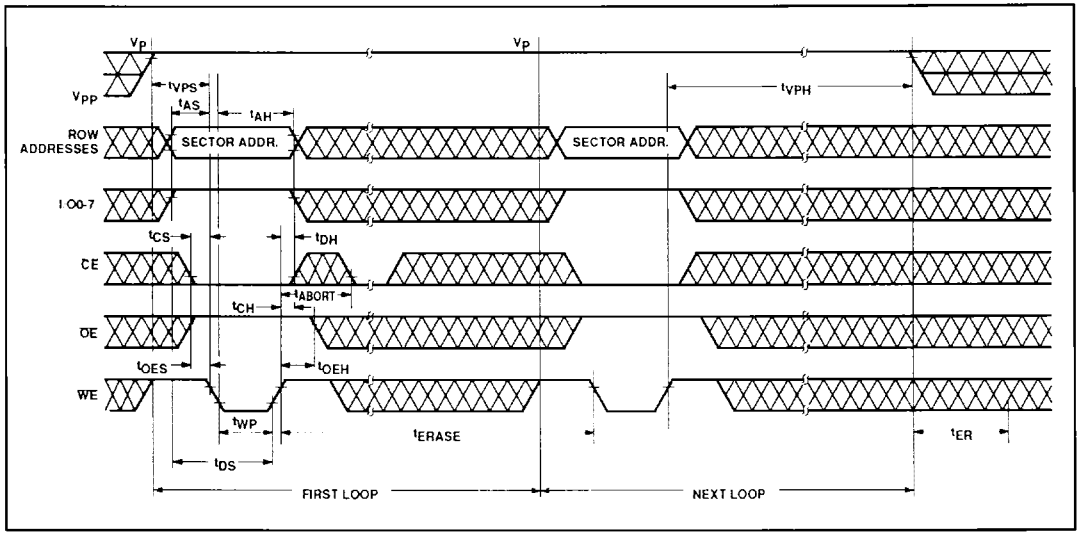

Figure 1. 48F010 Write Algorithm

## SECTOR ERASE AC ELECTRICAL CHARACTERISTICS

Over the $V_{CC}$ and temperature range

| SYMBOL | PARAMETER | 48F010 | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{VPS}$ | $V_{PP}$ Setup time | 2 | | µs |
| $t_{VPH}$ | $V_{PP}$ Hold time | 500 | | ms |
| $t_{CS}$ | $\overline{CE}$ Setup time | 0 | | ns |
| $t_{OES}$ | $\overline{OE}$ Setup time | 0 | | ns |
| $t_{AS}$ | Address Setup time | 20 | | ns |
| $t_{AH}$ | Address Hold time | 100 | | ns |
| $t_{DS}$ | Data Setup time | 50 | | ns |
| $t_{DH}$ | Data Hold time | 0 | | ns |
| $t_{WP}$ | $\overline{WE}$ Pulse Width | 100 | | ns |
| $t_{CH}$ | $\overline{CE}$ Hold time | 0 | | ns |
| $t_{OEH}$ | $\overline{OE}$ Hold time | 0 | | ns |
| $t_{ERASE}$ | Sector Erase time | 500 | | ms |
| $t_{ABORT}$ | Sector Erase delay | | 250 | µs |
| $t_{ER}$ | Erase Recovery time | | 250 | ms |

## SECTOR ERASE TIMING DIAGRAM



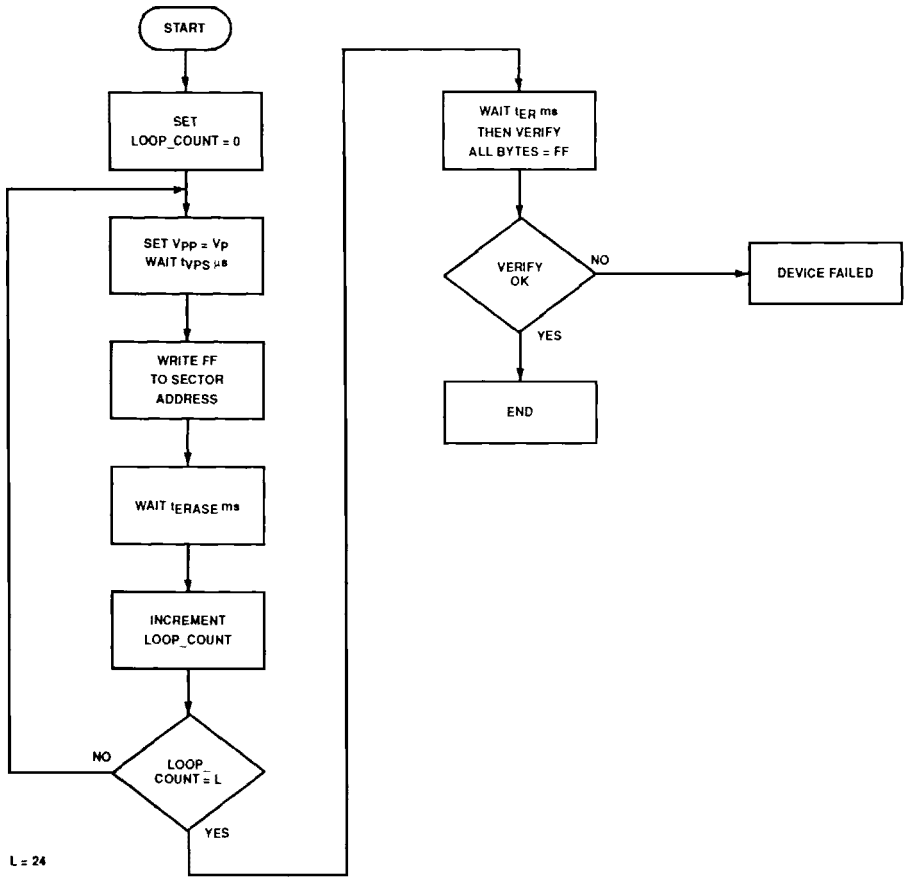


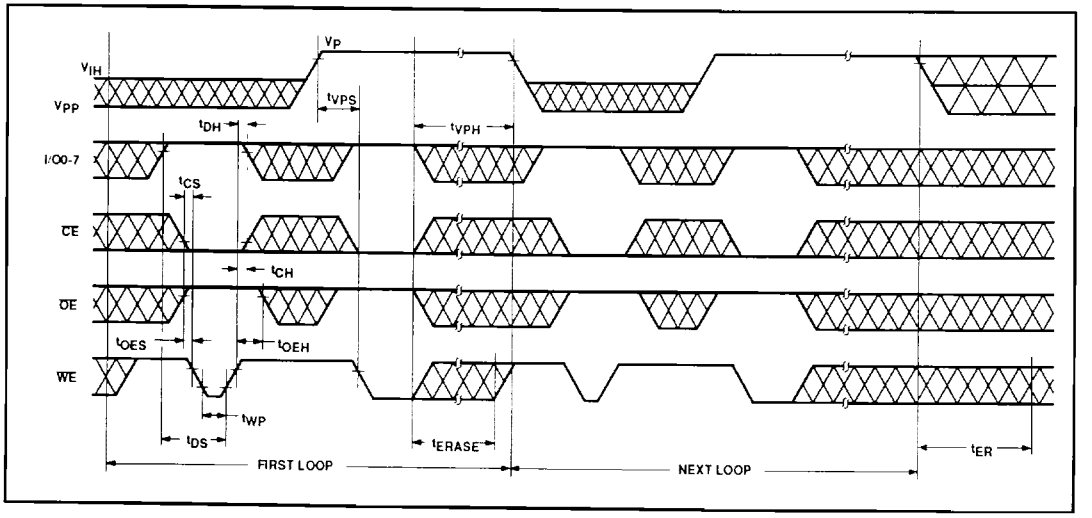

Figure 2. 48F010 Sector Erase Algorithm

## CHIP ERASE AC ELECTRICAL CHARACTERISTICS

Over the $V_{CC}$ and temperature range

| SYMBOL | PARAMETER | 48F010 | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{VPS}$ | $V_{PP}$ Setup time | 2 | | µs |
| $t_{VPH}$ | $V_{PP}$ Hold time | 500 | | ms |
| $t_{CS}$ | $\overline{CE}$ Setup time | 0 | | ns |
| $t_{OES}$ | $\overline{OE}$ Setup time | 0 | | ns |
| $t_{DS}$ | Data Setup time | 50 | | ns |
| $t_{DH}$ | Data Hold time | 0 | | ns |
| $t_{WP}$ | $\overline{WE}$ Pulse Width | 100 | | ns |
| $t_{CH}$ | $\overline{CE}$ Hold time | 0 | | ns |
| $t_{OEH}$ | $\overline{OE}$ Hold time | 0 | | ns |
| $t_{ERASE}$ | Chip Erase time | 500 | | ms |
| $t_{ER}$ | Erase Recovery time | | 250 | ms |

## CHIP ERASE TIMING DIAGRAM



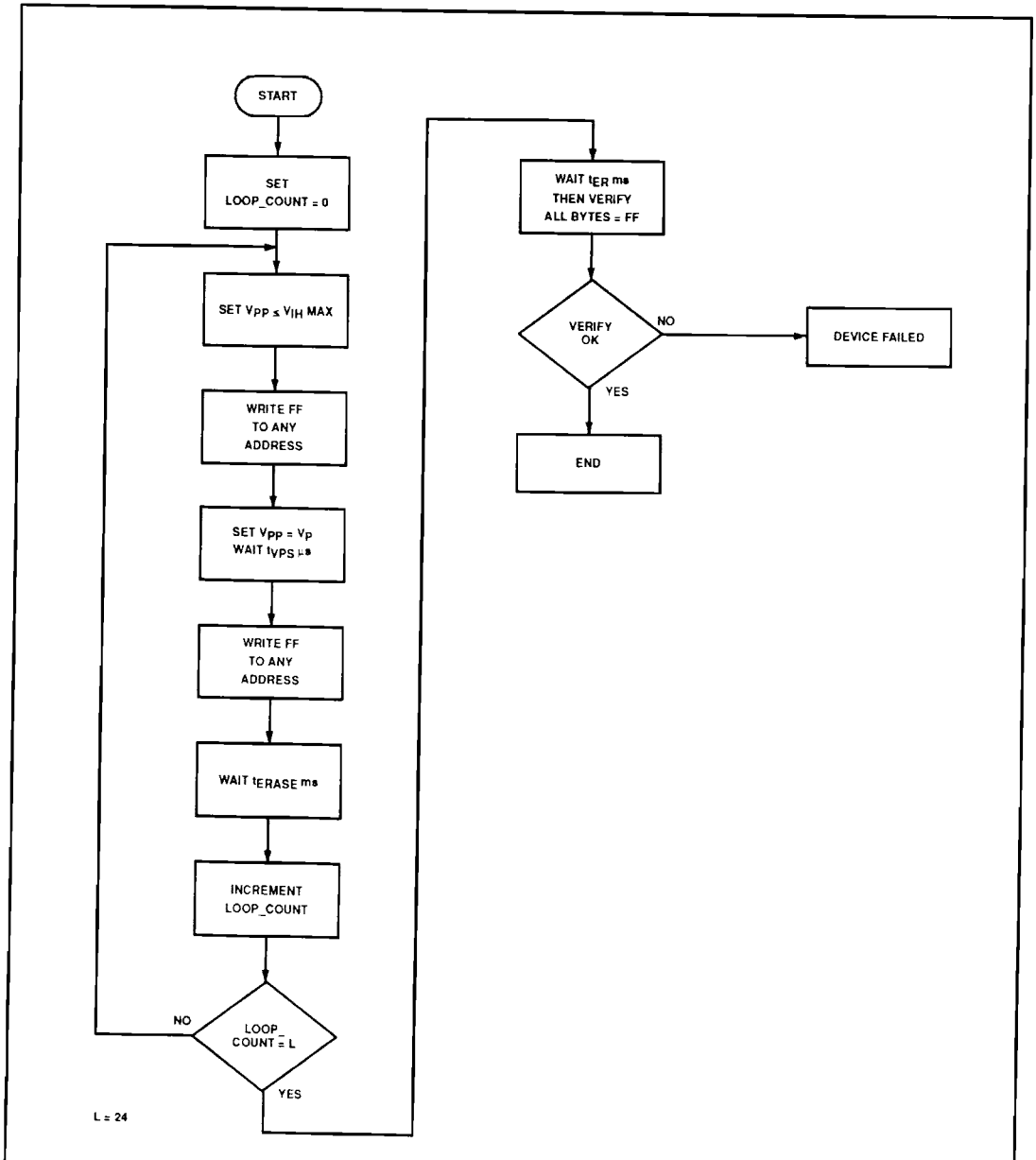



Figure 3. 48F010 Chip Erase Algorithm