Monolithic N-Channel JFET Duals

PRODUCT SUMMARY				
Part Number	**$V_{GS(off)}$ (V)**	**$V_{(BR)GSS}$ Min (V)**	**g_{fs} Min (mS)**	**$\|V_{GS1} - V_{GS2}\|$ Max (mV)**
SST421NL	−0.4 to−2	−40	0.3	10
SST423NL	−0.4 to −2	−40	0.3	25

FEATURES

- Anti Latchup Capability
- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 0.6 pA
- Low Noise
- High CMRR: 102 dB

BENEFITS

- External Substrate Bias—Avoids Latchup
- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signals

APPLICATIONS

- Ultralow Input Current Differential Amps
- High-Speed Comparators
- Impedance Converters

DESCRIPTION

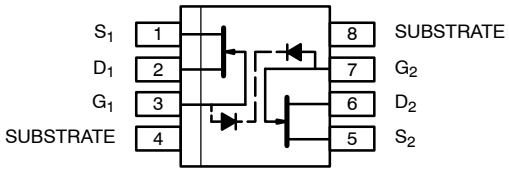
The SST421NL/423NL are monolithic dual n-channel JFETs designed to provide very high input impedance for differential amplification and impedance matching. Among its many unique features, this series offers low operating gate current.

The SO-8 package provides ease of manufacturing, and the symmetrical pinout prevents improper orientation. The SO-8 package is available with tape-and-reel options for compatibility with automatic assembly methods.

Pins 4 and 8 on SST421NL/423NL part numbers enable the substrate to be connected to a positive polarity, external bias (V_{DD}) to avoid latchup.

Similar versions of these part numbers are available in the hermetically sealed TO-78 package. Full military processing is available. See data sheets for part numbers U421/423.

Narrow Body SOIC



Top View

Marking Codes:

SST421NL – (421NL)
SST423NL – (423NL)

ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage . . . . . −40 V
Gate-Gate Voltage . . . . . ±40 V
Gate Current . . . . . 10 mA
Lead Temperature ($^1/_{16}$" from case for 10 sec.) . . . . . 300 °C
Storage Temperature . . . . . −65 to 200°C
Operating Junction Temperature . . . . . −55 to 150°C

Power Dissipation :
Per Side[a] . . . . . 300 mW
Total[b] . . . . . 500 mW

Notes
a. Derate 2.4 mW/°C above 25°C
b. Derate 4 mW/°C above 25°C

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Specific Test Conditions	Typ[a]	Limits SST421NL Min	Limits SST421NL Max	Limits SST423NL Min	Limits SST423NL Max	Unit
Static								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = –1 μA, V_{DS} = 0 V	–60	–40		–40		V
Gate-Gate Breakdown Voltage	$V_{(BR)G1-G2}$	I_G = ±1 μA, I_D = 0, I_S = 0	±55	±40		±40		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 nA	–1.2	–0.4	–2	–0.4	–2	V
Saturation Drain Current	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	400	60	1000	60	1000	μA
Gate Reverse Current	I_{GSS}	V_{GS} = –20 V, V_{DS} = 0 V	–0.6		–50		–50	pA
		T_A = 125°C	–0.3		–50		–50	nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 30 μA	–1.0					pA
Drain-Source On-Resistance	$r_{DS(on)}$	V_{GS} = 0 V, I_D = 10 μA	2000					Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 10 V, I_D = 30 μA	–0.8		–1.8		–1.8	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA , V_{DS} = 0 V	0.7					V
Dynamic								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	0.6	0.3	1.5	0.3	1.5	mS
Common-Source Output Conductance	g_{os}		4		10		10	μS
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 30 μA , f = 1 kHz	0.2	0.12	0.35	0.12	0.35	mS
Common-Source Output Conductance	g_{os}		0.4		3		3	μS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	1.4		3		3	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		1.5		1.5	pF
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DS} = 10 V, I_D = 30 μA , f = 10 Hz	30					$\frac{nV}{\sqrt{Hz}}$
Matching								
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	V_{DG} = 10 V, I_D = 30 μA			10		25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 30 μA T_A = –55 to 125°C			10		40	μV/°C
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 30 μA	102	90		80		dB

Notes
a. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.

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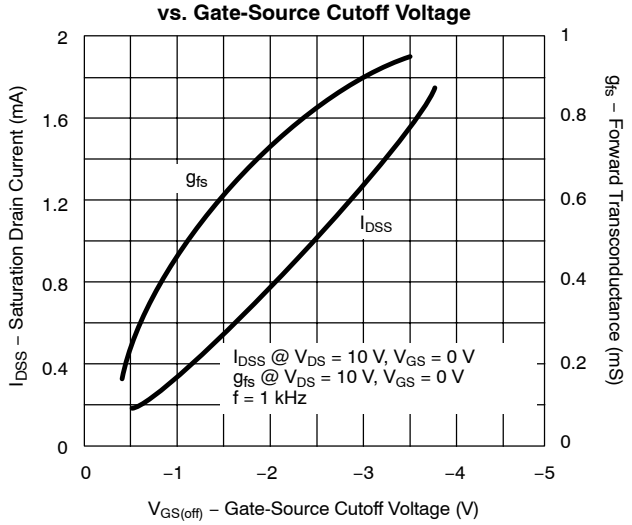
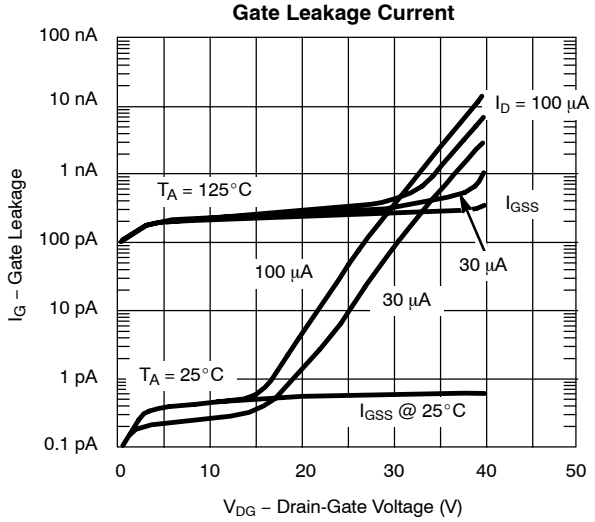
TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

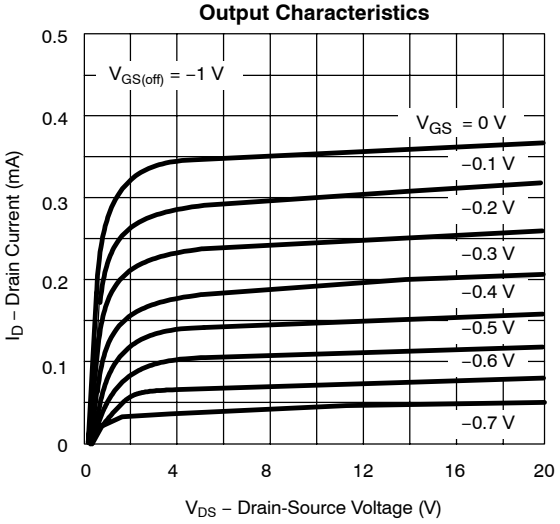
Drain Current and Transconductance vs. Gate-Source Cutoff Voltage



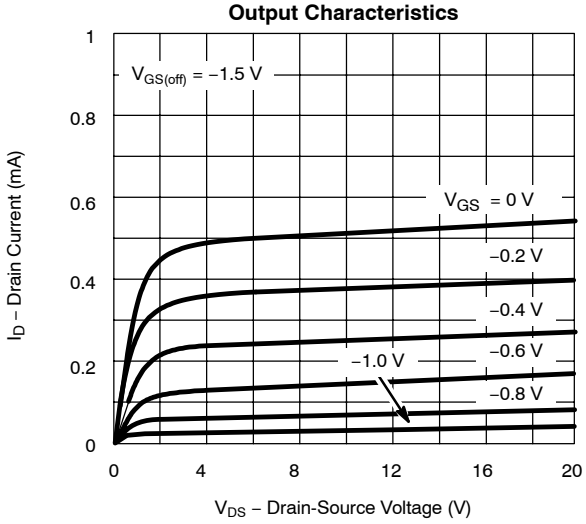
Gate Leakage Current



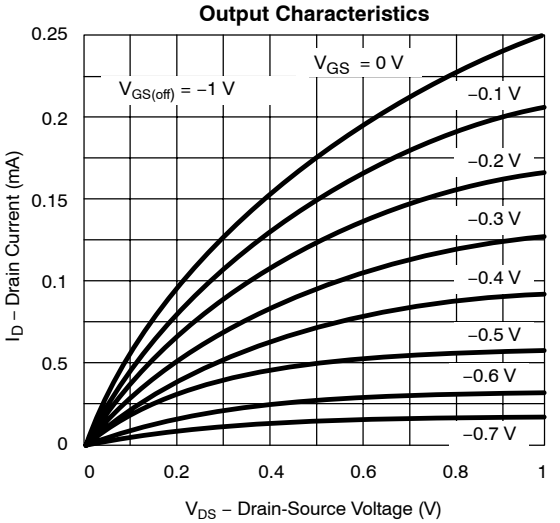
Output Characteristics



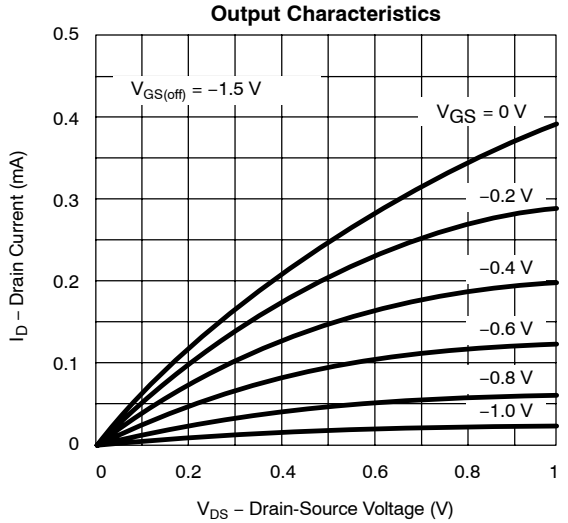
Output Characteristics



Output Characteristics

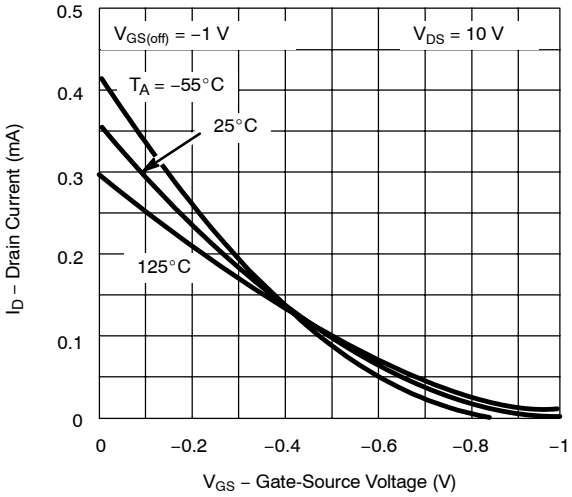


Output Characteristics

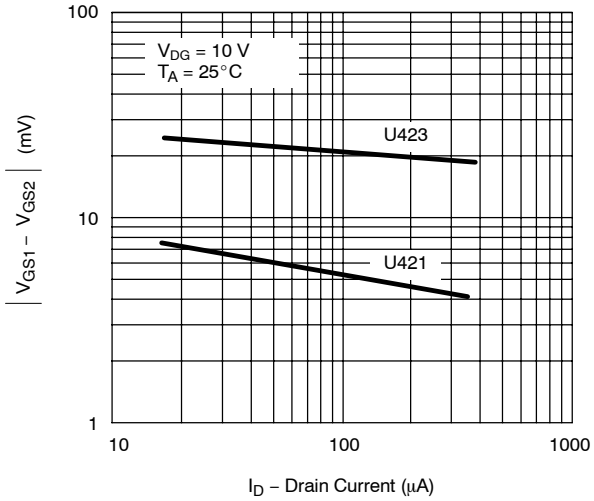


TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

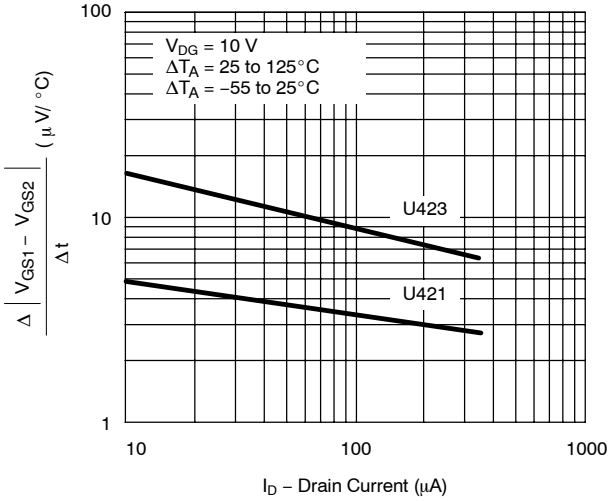
Transfer Characteristics



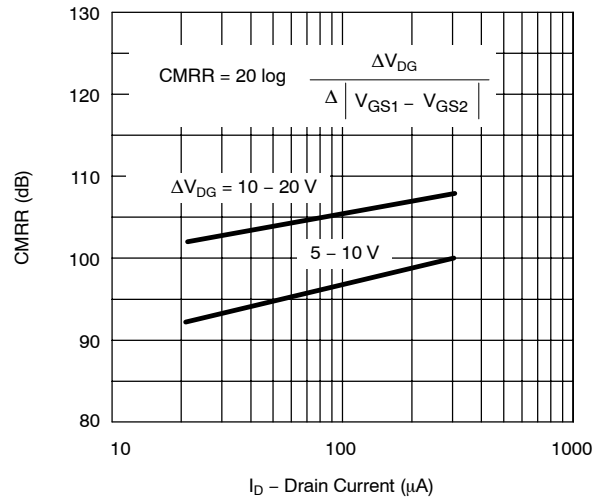
Gate-Source Differential Voltage vs. Drain Current



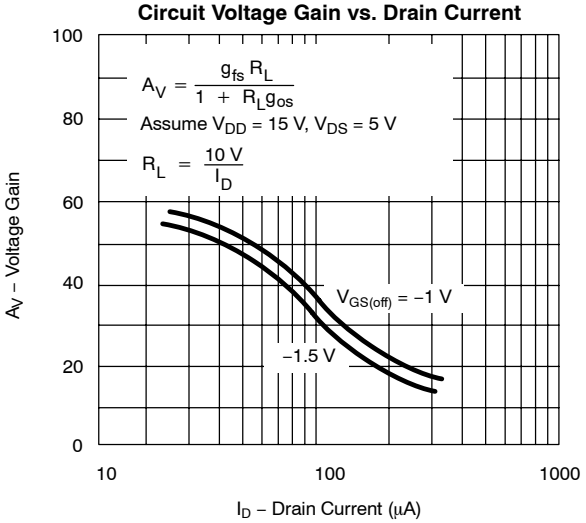
Voltage Differential with Temperature vs. Drain Current



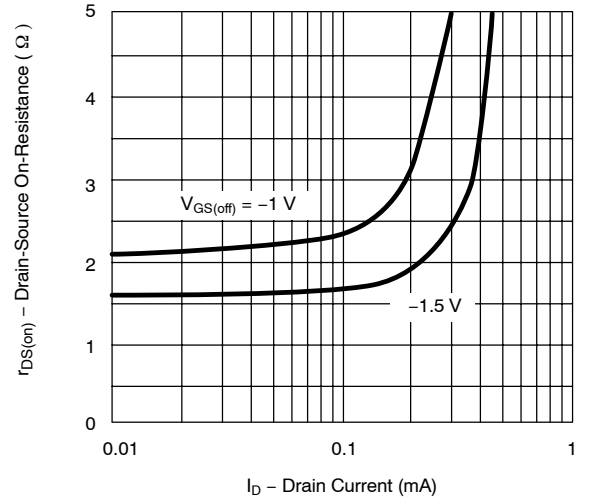
Common Mode Rejection Ratio vs. Drain Current



Circuit Voltage Gain vs. Drain Current



On-Resistance vs. Drain Current



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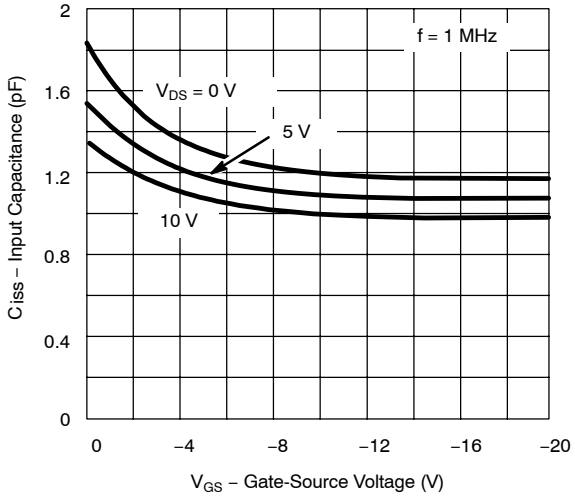
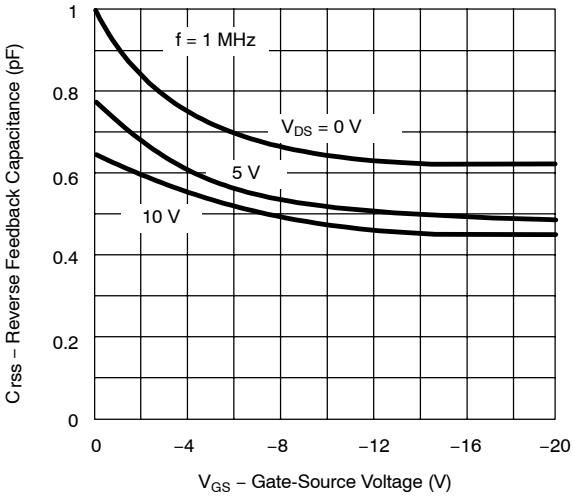
TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

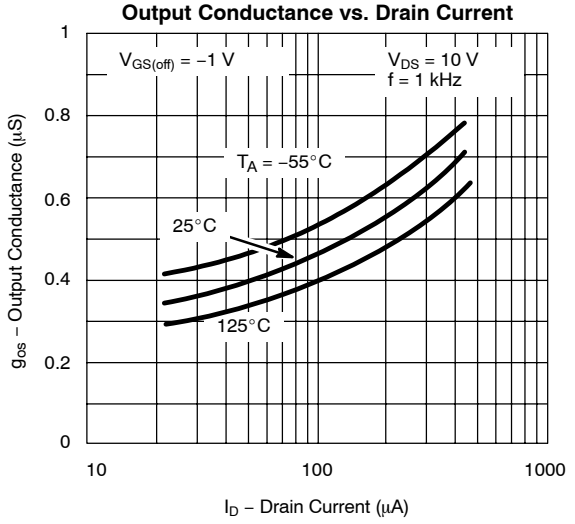
Common-Source Input Capacitance vs. Gate-Source Voltage



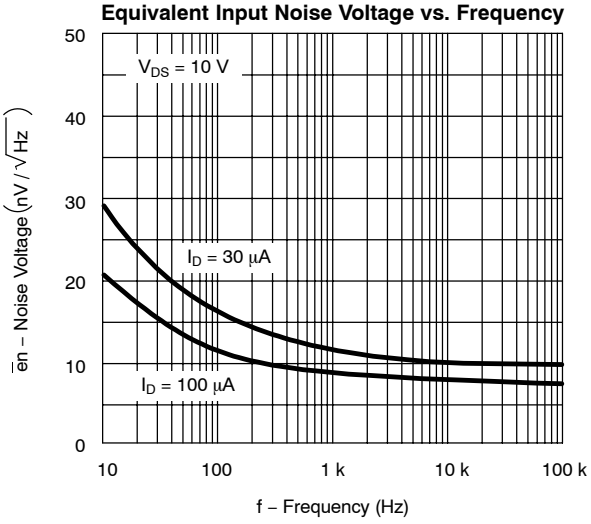
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



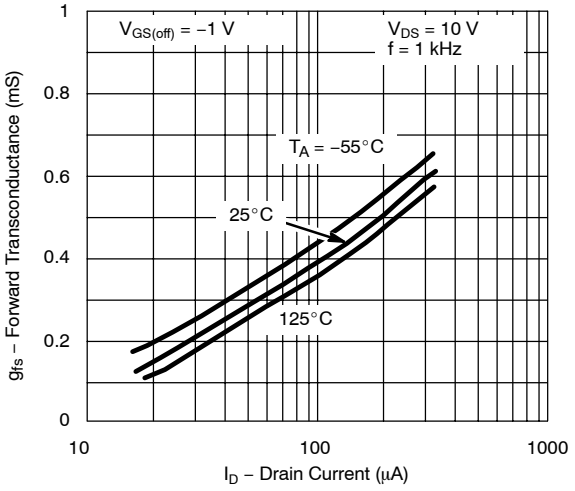
Output Conductance vs. Drain Current



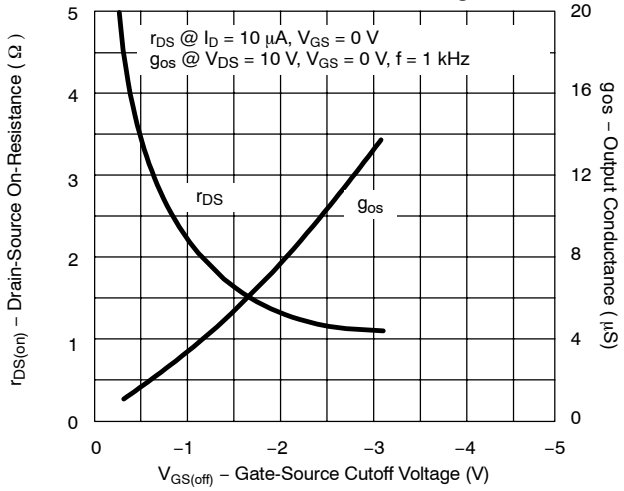
Equivalent Input Noise Voltage vs. Frequency



Common-Source Forward Transconductance vs. Drain Current



On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage



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