STK14CB16

256K x 16 *AutoStore*™ nvSRAM
QuantumTrap™ CMOS
Nonvolatile Static RAM

Advanced Information

FEATURES

- **25ns Access Time**
- **"Hands-off" Automatic *STORE* on Power Down with only a small capacitor**
- ***STORE* to *QuantumTrap*™ Nonvolatile Elements is Initiated by Software , device pin or *AutoStore*™ on Power Down**
- ***RECALL* to SRAM Initiated by Software or Power Up**
- **Unlimited *READ, WRITE* and *RECALL* Cycles**
- **10mA Typical I_{CC} at 200ns Cycle Time**
- **500,000 *STORE* Cycles to *QuantumTrap*™**
- **100-Year Data Retention to *QuantumTrap*™**
- **Single 3V +20%, -10% Operation**
- **Commercial and Industrial Temperatures**
- **SSOP and TSOP II packages**
- **RoHS Compliance**

DESCRIPTION

The Simtek STK14CB16 is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate Simtek's *QuantumTrap*™ technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent, nonvolatile data resides in the highly reliable *QuantumTrap*™ cell. Data transfers from the SRAM to the nonvolatile elements (the *STORE* operation) takes place automatically at power down. On power up, data is restored to the SRAM (the *RECALL* operation) from the nonvolatile memory. Both the *STORE* and *RECALL* operations are also available under software control.

BLOCK DIAGRAM

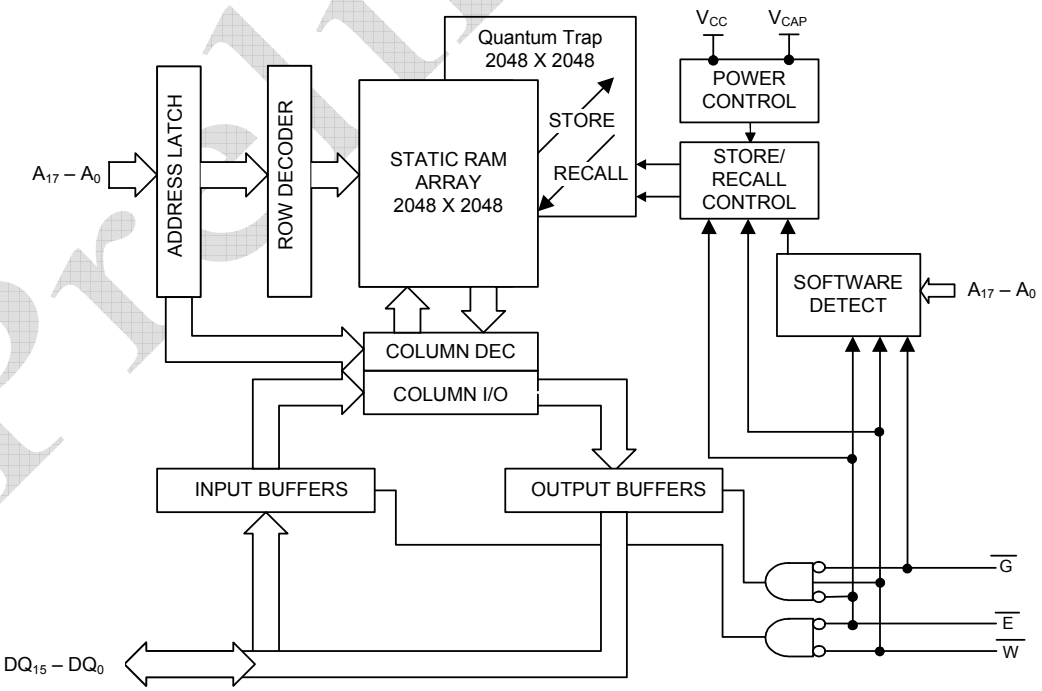
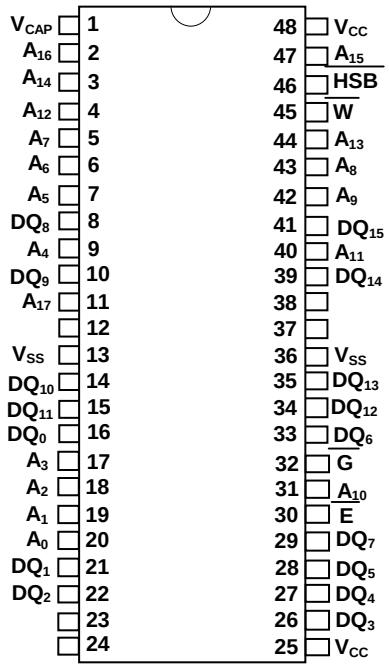
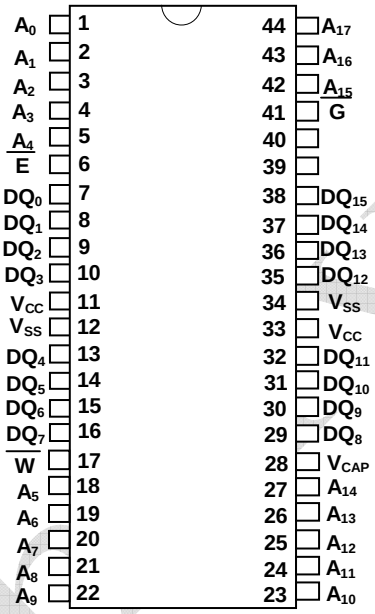


Figure 1. Block Diagram

PACKAGES



48 Pin SSOP



44 Pin TSOP II

Relative PCB area usage.
See website for detailed package size specifications.

PIN DESCRIPTIONS

Pin Name	I/O	Description
$A_{17} - A_0$	Input	Address: The 18 address inputs select one of 262,144 words in the nvSRAM array.
$DQ_{15} - DQ_0$	I/O	Data: Bi-directional 16-bit data bus for accessing the nvSRAM.
$\overline{E}$	Input	Chip Enable: The active low $\overline{E}$ input selects the device.
$\overline{W}$	Input	Write Enable: The active low $\overline{W}$ enables data on the DQ pins to be written to the address location latched by the falling edge of $\overline{E}$.
$\overline{G}$	Input	Output Enable: The active low $\overline{G}$ input enables the data output buffers during read cycles. De-asserting $\overline{G}$ high causes the DQ pins to tri-state.
V_{CC}	Power Supply	Power 3.0V +20%, -10%
$\overline{HSB}$	I/O	Hardware Store Busy: When low this output indicates a Hardware Store is in progress. When pulled low external to the chip it will initiate a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin high if not connected. (Connection Optional)
V_{CAP}	Power Supply	*Autostore* Capacitor: Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.
V_{SS}	Power Supply	Ground
(Blank)	No Connect	Unlabeled pins have no internal connection.

ABSOLUTE MAXIMUM RATINGS[a]

Power Supply Voltage	-0.5V to +4.1V
Voltage on Input Relative to V_{SS}	-0.5V to (V_{CC} + 0.5V)
Voltage on Outputs	-0.5V to (V_{CC} + 0.5V)
Temperature under Bias	–55°C to 125°C
Junction Temperature	–55°C to 140°C
Storage Temperature	–65°C to 150°C
Power Dissipation	1W
DC Output Current (1 output at a time, 1s duration)	15mA

Notes

a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Package Thermal Characteristics see website: http://www.simtek.com/

DC CHARACTERISTICS

Symbol	Parameter	Commercial		Industrial		Units	Notes
		MIN	MAX	MIN	MAX		
I_{CC1}	Average V_{CC} Current		55 45 30		60 50 45	mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns Dependent on output loading and cycle rate. Values obtained without output loads.
I_{CC2}	Average V_{CC} Current during STORE		2		2	mA	All Inputs Don't Care, V_{CC} = max Average current for duration of *STORE* cycle (t_{STORE}).
I_{CC3}	Average V_{CC} Current at t_{AVAV} = 200ns 3V, 25°C, Typical		10		10	mA	$\overline{W}$ ≥ (V_{CC} – 0.2V) All Others Inputs Cycling, at CMOS Levels. Dependent on output loading and cycle rate. Values obtained without output loads.
I_{CC4}	Average V_{CAP} Current during *AutoStore*™ Cycle		2		2	mA	All Inputs Don't Care Average current for duration of *STORE* cycle (t_{STORE}).
I_{SB}	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		3		3	mA	$\overline{E}$ ≥ (V_{CC} – 0.2V) All Others V_{IN} ≤ 0.2V or ≥ (V_{CC} – 0.2V) Standby current level after nonvolatile cycle is complete.
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max V_{IN} = V_{SS} to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±1		±1	µA	V_{CC} = max V_{IN} = V_{SS} to V_{CC}, $\overline{E}$ or $\overline{G}$ ≥ V_{IH}
V_{IH}	Input Logic "1" Voltage	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – 0.5	0.8	V_{SS} – 0.5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –2mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 4mA
T_A	Operating Temperature	0	70	–40	85	°C	
V_{CC}	Operating Voltage	2.7	3.6	2.7	3.6	V	3.0V +20%, -10%
V_{CAP}	Storage Capacitor	44	100	44	100	µF	Between Vcap pin and Vss, 5V rated.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	≤ 5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 2 and Figure 3

CAPACITANCE[b] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	7	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Notes
b: These parameters are guaranteed but not tested

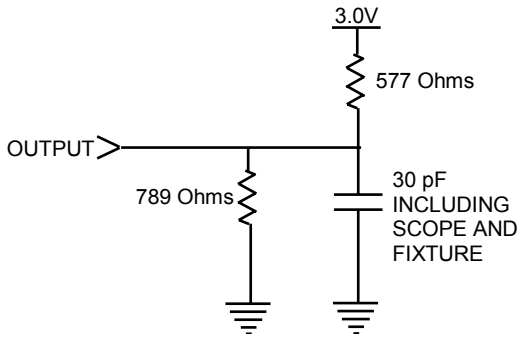


Figure 2. AC Output Loading

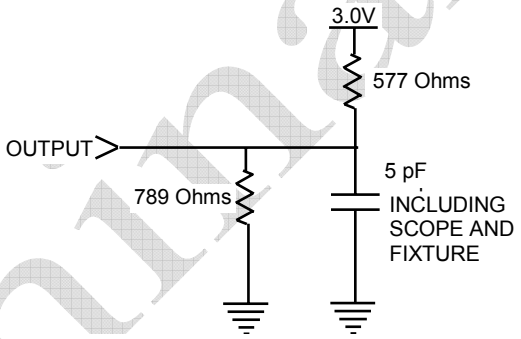


Figure 3. AC Output Loading, for tristate specs (t_{HZ}, t_{LZ}, t_{WLQZ}, t_{WHQZ}, t_{GLQX}, t_{GHQZ})

SRAM READ CYCLES #1 & #2

NO.	SYMBOLS			PARAMETER					STK14CB16-25		UNITS
	#1	#2	Alt.						MIN	MAX	
1		t_{ELQV}	t_{ACS}	Chip Enable Access Time						25	ns
2	t_{AVAV}[c]	t_{AVAV}[c]	t_{RC}	Read Cycle Time					25		ns
3	t_{AVQV}[d]		t_{AA}	Address Access Time						25	ns
4		t_{GLQV}	t_{OE}	Output Enable to Data Valid						12	ns
5	t_{AXQX}[d]		t_{OH}	Output Hold after Address Change					3		ns
6		t_{ELQX}	t_{LZ}	Chip Enable to Output Active					3		ns
7		t_{EHQZ}[e]	t_{HZ}	Chip Disable to Output Inactive						10	ns
8		t_{GLQX}	t_{OLZ}	Output Enable to Output Active					0		ns
9		t_{GHQZ}[e]	t_{OHZ}	Output Disable to Output Inactive						10	ns
10		t_{ELICC}[b]	t_{PA}	Chip Enable to Power Active					0		ns
11		t_{EHICC}[b]	t_{PS}	Chip Disable to Power Standby						25	ns

Notes

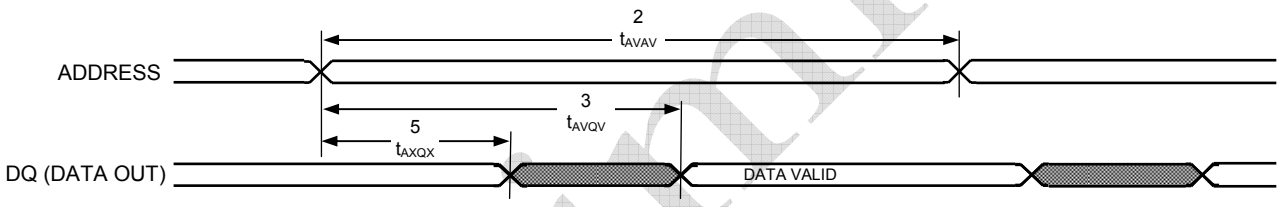
c: $\overline{W}$ must be high during SRAM READ cycles

d: Device is continuously selected with $\overline{E}$ and $\overline{G}$ both low

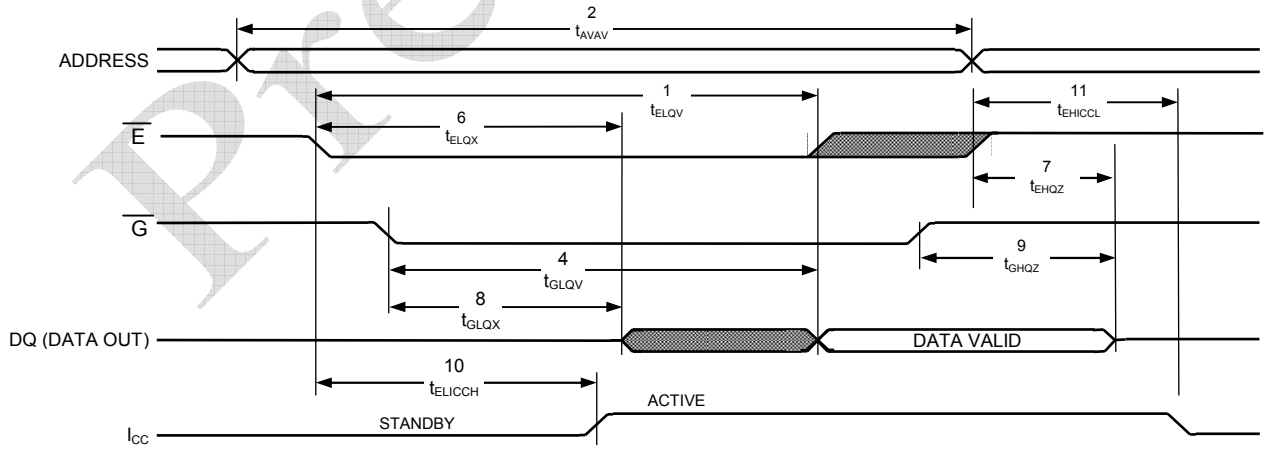
e: Measured ± 200mV from steady state output voltage

f: $\overline{HSB}$ must remain high during READ and WRITE cycles.

SRAM READ CYCLE #1: Address Controlled[c,d,f]



SRAM READ CYCLE #2: $\overline{E}$ Controlled[c,f]



SRAM WRITE CYCLES #1 & #2

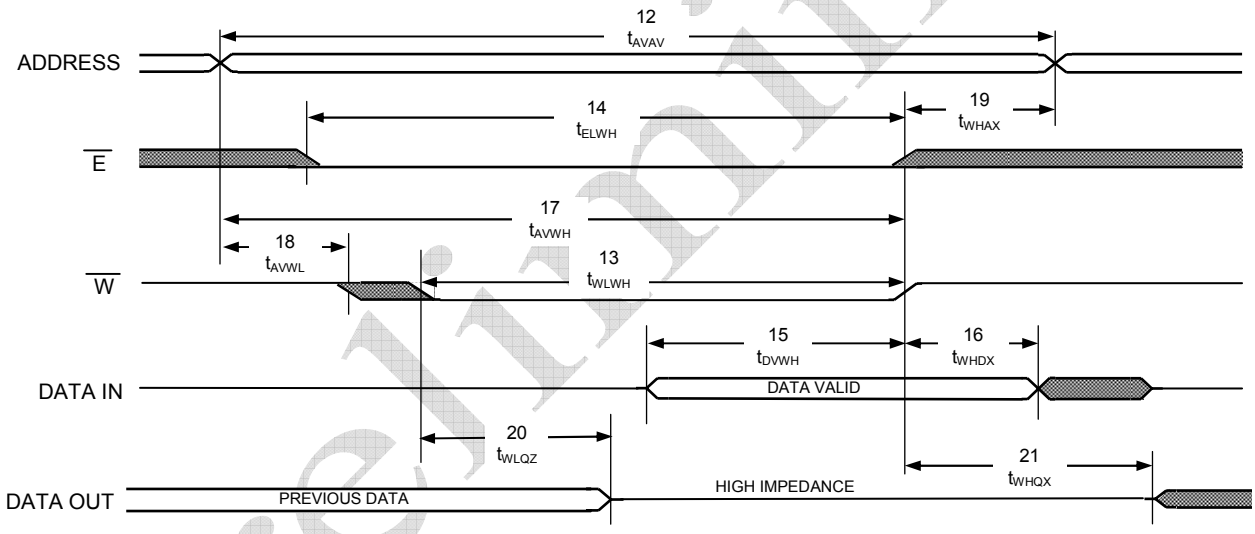
NO.	SYMBOLS			PARAMETER					STK14CB16-25		UNITS
	#1	#2	Alt.						MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time					25		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width					20		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write					20		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write					10		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write					0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write					20		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write					0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write					0		ns
20	t_{WLQZ}[e,g]		t_{WZ}	Write Enable to Output Disable						10	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write					3		ns

Notes

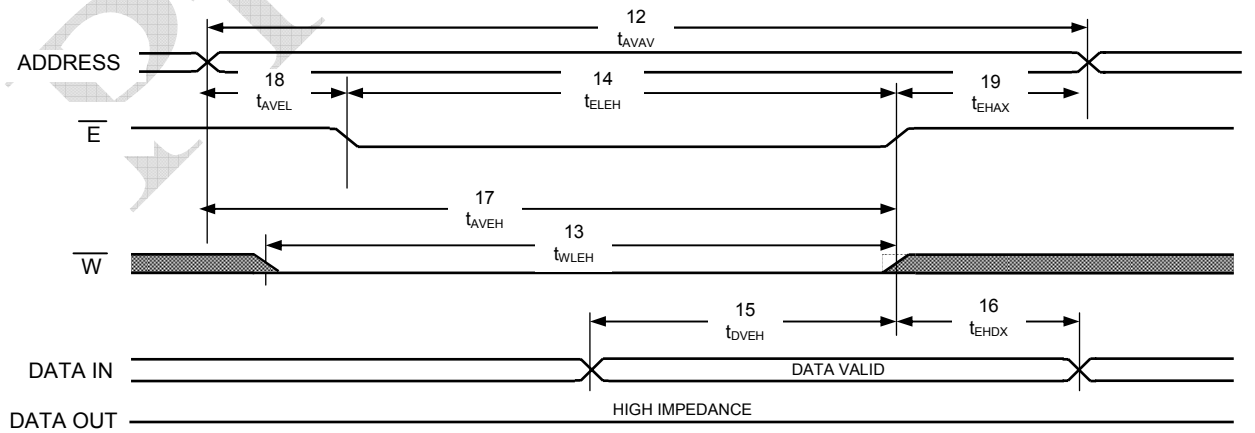
g: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.

h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.

SRAM WRITE CYCLE #1: $\overline{W}$ Controlled[h,f]



SRAM WRITE CYCLE #2: $\overline{E}$ Controlled[h,f]

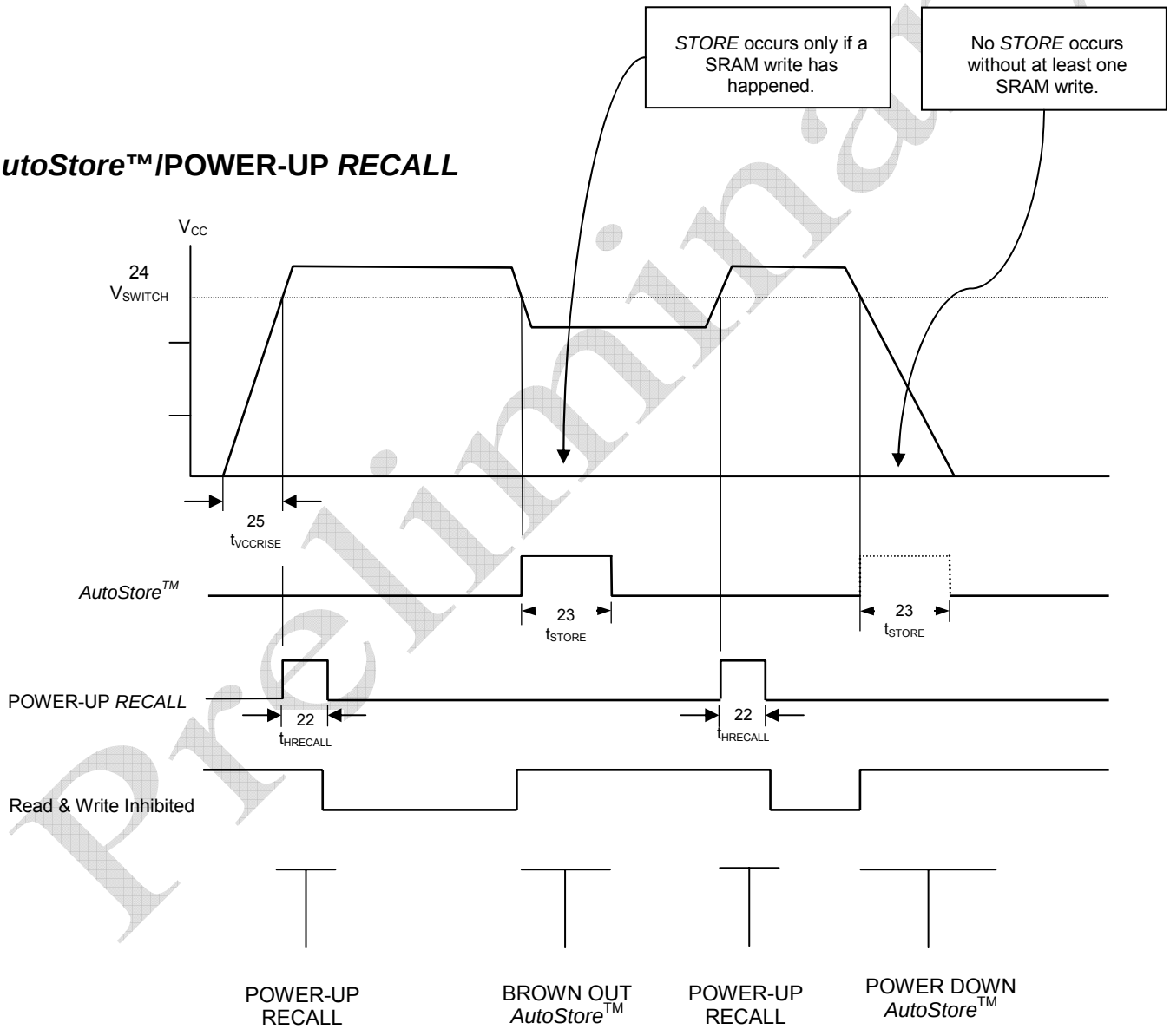


*AutoStore™ /*POWER-UP *RECALL*

NO.	SYMBOLS		PARAMETER	STK14CB16		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	$t_{HRECALL}$		Power-up RECALL Duration		10	ms	**i**
23	t_{STORE}	t_{HLHZ}	STORE Cycle Duration		15	ms	**j**
24	V_{SWITCH}		Low Voltage Trigger Level	2.55	2.65	V	
25	$t_{VCCRISE}$		V_{CC} Rise Time	150		µs	

Notes
i: $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}
j: If an SRAM WRITE has not taken place since the last nonvolatile cycle, no *STORE* will take place

*AutoStore™/*POWER-UP *RECALL*



Note: Read and Write cycles will be ignored during *STORE, RECALL* and while V_{CC} is below V_{SWITCH}

SOFTWARE-CONTROLLED *STORE/RECALL* CYCLE[k,l]

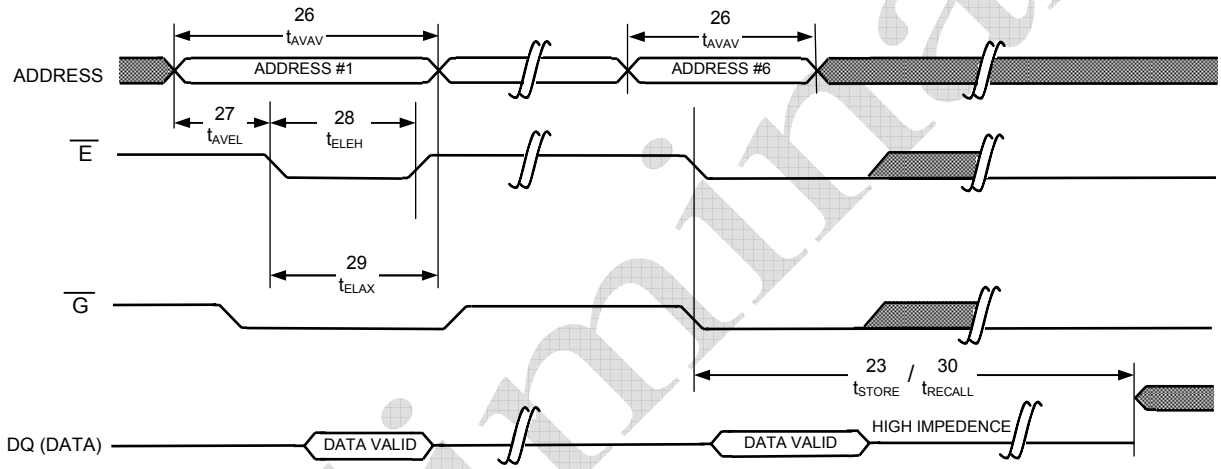
NO.	SYMBOLS			PARAMETER					STK14CB16-25		UNITS	NOTES
	$\overline{E}$ cont	$\overline{G}$ cont	Alt.						MIN	MAX		
26	t_{AVAV}	t_{AVAV}	t_{RC}	*STORE/RECALL* Initiation Cycle Time					25		ns	I
27	t_{AVEL}	t_{AVGL}	t_{AS}	Address Set-up Time					0		ns	
28	t_{ELEH}	t_{GLGH}	t_{CW}	Clock Pulse Width					20		ns	
29	t_{ELAX}	t_{GLAX}		Address Hold Time					20		ns	
30	t_{RECALL}	t_{RECALL}		*RECALL* Duration						50	µs	

Notes

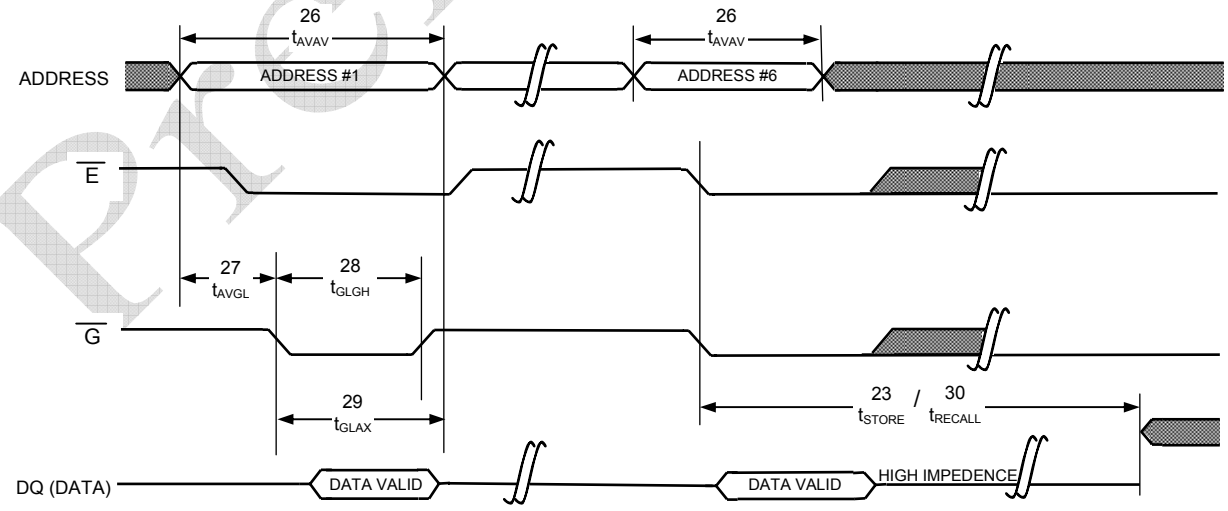
k: The software sequence is clocked with $\overline{E}$ controlled READs or $\overline{G}$ controlled READs.

l: The six consecutive addresses must be read in the order listed in the Mode Selection Table. $\overline{W}$ must be high during all six consecutive cycles.

SOFTWARE *STORE/RECALL* CYCLE: $\overline{E}$ Controlled[l]



SOFTWARE *STORE/RECALL* CYCLE: $\overline{G}$ Controlled[l]



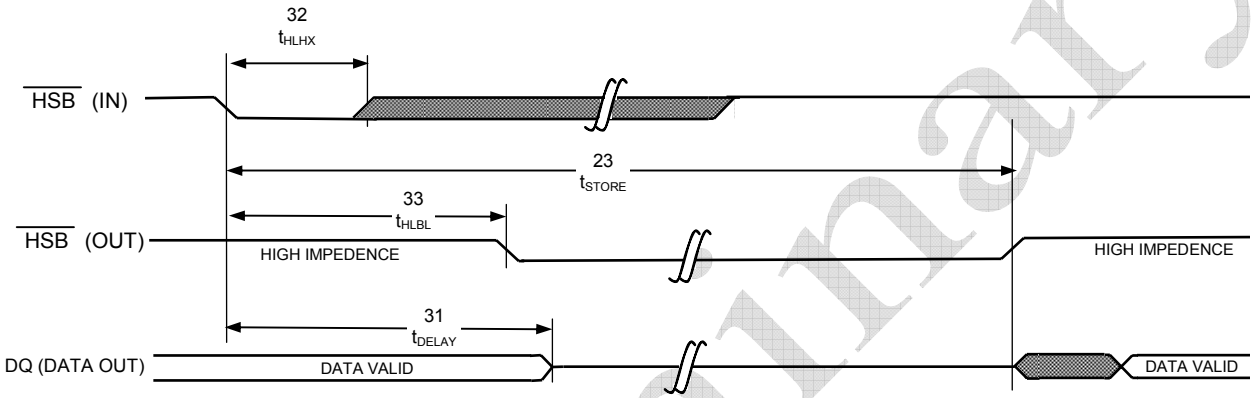
HARDWARE *STORE* CYCLE

NO.	SYMBOLS		PARAMETER	STK14CB16		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
31	t_{DELAY}	t_{HLQZ}	Time Allowed to Complete SRAM Cycle	1		µs	p
32	t_{HLHX}		Hardware *STORE* Pulse Width	15		ns	
33	t_{HLBL}		Hardware *STORE* Low to *STORE* Busy		300	ns	

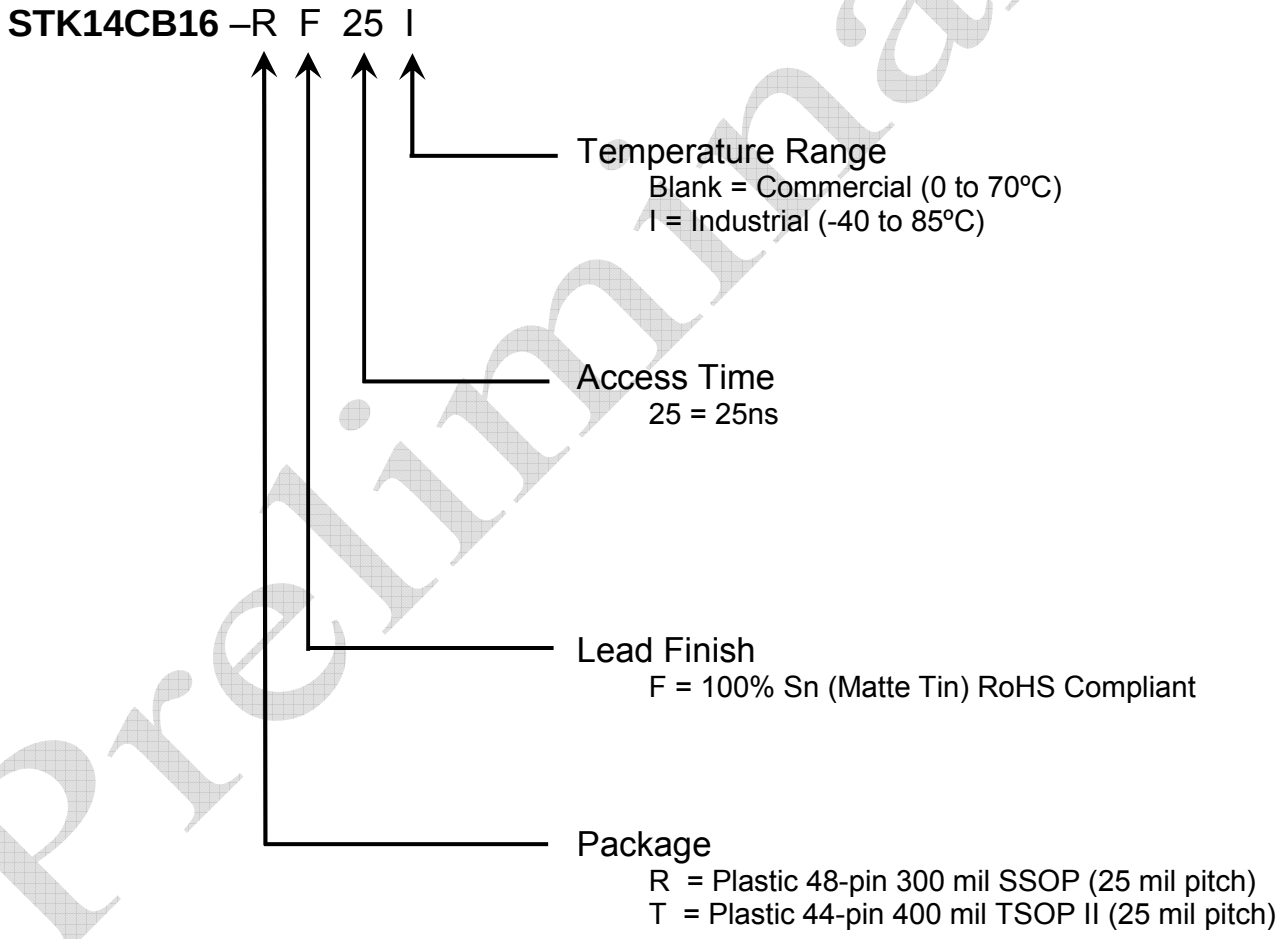
Notes

m: Read and Write cycles in progress before $\overline{HSB}$ is asserted are given this amount of time to complete.

HARDWARE *STORE* CYCLE



ORDERING INFORMATION



Document Revision History

Revision	Date	Summary
0.0	October 2005	Advanced Information