FAIRCHILD
SEMICONDUCTOR®

AN9101
EVALUATION BOARD
APPLICATION NOTE

FEATURES

- Up to 125 MSPS Sample Rate
- On-Board Differential Clock Driver
- Controlled Impedance PCB for Critical Signals
- High-frequency, Low-distortion SMA Connectors for I/O

APPLICATIONS

- Evaluation and Characterization of the SPT9101
- Guide for Designing with the SPT9101
- Engineering System Prototype Aid

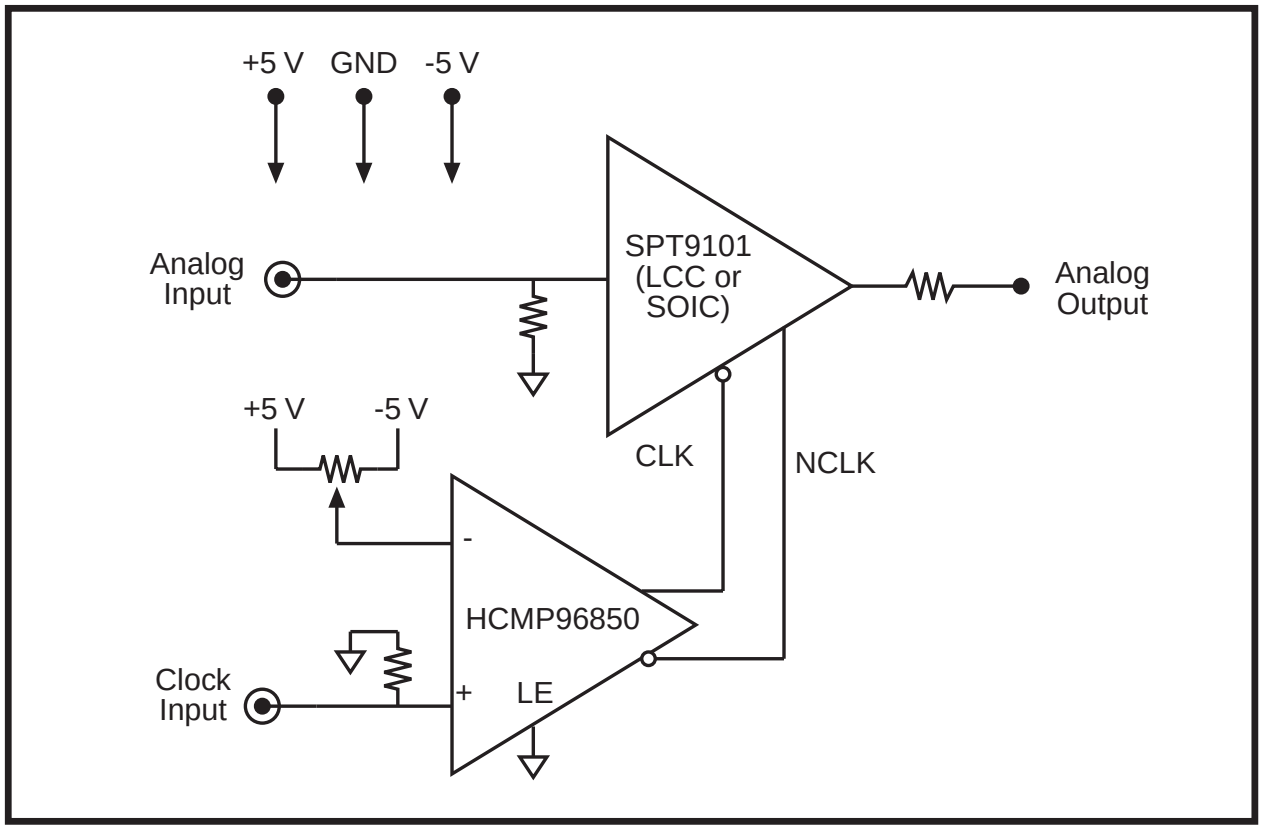
GENERAL DESCRIPTION

The EB9101 evaluation board is intended as a tool for device evaluation and characterization and to demonstrate the performance of the SPT9101 (Track-and-Hold Amplifier). The SPT9101 is a high-speed track-and-hold amplifier capable of sampling up to 125 MSPS with 8-bit resolution, and up to 50 MSPS with 12-bit resolution. It is a second source for the Analog Devices' AD9101. The devices are pin compatible, except the SPT9101 does not require an external bootstrap capacitor.

This application note is a supplement to the data sheet and includes more detailed information on the interfacing circuits required to operate the SPT9101. The evaluation board is designed to accommodate a wide variety of applications. It can be easily modified to suit a specific application by using the prototype area provided. Contact the Fairchild Applications Engineering Department if assistance is needed.

This application note describes in more detail the following functional blocks of the evaluation board: power supplies and grounding, analog input/output, sample clock circuitry and layout.

BLOCK DIAGRAM



POWER SUPPLIES AND GROUNDING

The EB9101 requires +5 V and -5.2 V supplies for all components on the evaluation board, including the comparator and the SPT9101. The supplies are adequately decoupled, but clean power supply sources are highly recommended. Note that all power is returned to a single common analog ground. This is the recommended arrangement when designing with this part. For example, if the SPT9101 is located on the front-end of an ADC, or if used as a deglicher for a high-speed DAC, it will be located in the analog section.

Before connecting any power supply to the evaluation board, set each supply to its correct value and then turn off the supplies. Ensure all supplies are connected and preset before power is applied. Fairchild recommends that both supplies be powered-up simultaneously. After power-up, verify the supply voltages are within specifications before proceeding. If adjustments are necessary, reference your measurement to the analog ground.

ANALOG INPUT/OUTPUT

The analog input signal can be fed directly through the SMA connector into V_{IN1}. There are two line termination resistors, R8 associated with the LCC package and R14 associated with the SOIC package. This design was used to ensure proper line termination with the shortest stub. That is, the resistor is as physically close to the SPT9101 as possible. Note that the termination is a chip style resistor that exhibits a low parasitic inductance and capacitance.

The SPT9101 has a fixed overall gain of four. The recommended maximum output is ±2.7 V or V_{IN} max = ±0.675 V. Figure 1 shows the transfer function of the SPT9101. The overdrive saturation characteristic can by observed in the transfer function, with a nonlinear recovery. Fairchild does not recommend operating in this region. If your design will exceed the recommended input level, Fairchild highly recommended using high-speed Schottky diodes for clamping the signal. Figure 2 shows an example circuit using Schottky diodes for the input limiting. The EB9101 is tested and verified to a ±0.5 V input range. In addition, dynamic performance at 125 MSPS is verified on the evaluation board.

The output of the SPT9101 is connected to its associated SMA output connector through a 27 Ω series resistor. Since this resistor is there to accommodate any improperly matched stub connection, its value can be changed to fit the user's purpose. The EB9101 uses either the LCC or SOIC package versions of the SPT9101. Use VOUT_1 if the SOIC package is installed and VOUT_2 if the LCC is installed.

It is not recommended to operate both devices on this board simultaneously. Degradation of performance of the SPT9101 can be expected if operated in this manner.

SAMPLE CLOCK CIRCUITRY

The evaluation board uses an HCMP96850 high-speed comparator in a 16-pin DIP package. The comparator's propagation delay is typically 2.4 ns with a very low offset of 3 mV and a minimum tracking bandwidth of 300 MHz. The comparator has been set up in a feedthrough mode by grounding the latch enable pin (ECL high), thus disabling the latch mode.

The comparator's input common mode range is ±2.5 V. Fairchild recommends that the clock input be generated from a signal generator with a sinewave amplitude of 1.0 V_{P-P} symmetrical around ground, and that R2 be open, R3 be shorted and R4 be equal to 50 Ω for proper line termination. With this input mode, a modest duty cycle adjustment is possible by adjusting potentiometer R1 to various DC levels on the comparator's non-inverting input. If a sinewave signal is not available then an ECL or TTL level signal may be used, with the proper voltage divider on the input to the comparator.

With an ECL input it is recommended that the resistor arrangement on the input of the comparator be the same as for a sinewave input. In addition, adjust R1 to approximately -1.3 V to be a mid-level for a nominal ECL signal for the comparator to operate against.

With a TTL input several aspects will need to be considered: the drive capability of the clock input; and the optimum termination for the clock signal. Using two appropriately selected resistors the amplitude of the signal will need to be divided to below the common mode range (less than 2.5 V). Fairchild recommends the addition of resistor R2 for proper termination of the clock signal, if these two resistors do not provide proper termination. For proper comparator operation, adjust potentiometer R1 to the mid-scale of the comparator input signal.

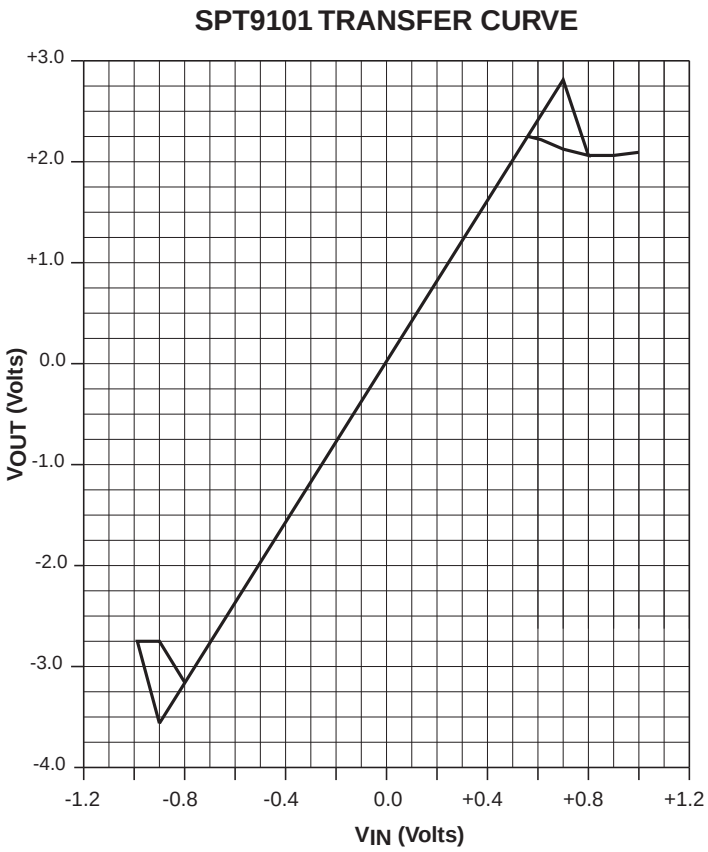
The output of the comparator is differential ECL. The CLK_IN of the comparator and CLK of the SPT9101 are in phase (note the double inversion). The outputs of the comparator use parallel termination of 270 Ω over 150 Ω (referenced to ground and -5.2 V). This parallel termination is located as close to the receiver end as physically possible to minimize reflection of the clock signals. In addition, there are clock test points (with an associated ground pad for shorter reference ground length) for a truer representation of the probed clock signal for timing purposes.

LAYOUT

This evaluation board is laid out with four layers: two signal layers with controlled 50 Ω impedance; an analog ground layer; and a power distribution layer. Decoupling surface mount capacitors are mounted as close as possible to the IC's and filter capacitors at the power input pins. Ferrite beads (FB1 and FB2) are used to further filter the SPT9101 power supply from the other associated circuitry onboard that uses the same power supplies.

The evaluation board has many capabilities and features. Easy connect, clip-on test points for power supplies (+5 V and -5 V), SMA connectors for sample clock input, analog input and track and hold output and a comparator with ECL output to drive the sample clock. The assembly is a self-contained building block that may be used for many system applications. There is a DIP footprint for a user configurable prototyping area on the left side of the board for sample clock circuitry.

Figure 1 - Transfer Function



SETUP AND CALIBRATION

The following setup should be performed to verify functional operation of the evaluation board.

1. Set and connect the power supplies as outlined in the Power Supplies and Grounding section.

2. Setup a 20 MHz sinewave, 1 V_{P-P} signal and connect it to the CLK_IN SMA. Adjust R1 for a 50% duty cycle while monitoring the CLK1 test pad.

3. Setup a 1 MHz sinewave 1.0 V_{P-P} signal and connect it to the VIN1 SMA. In addition, ensure that the two signal generators are synchronized together.

4. Using an adequate bandwidth scope, observe a signal that is similar to a sinewave with 20 steps. Note: there will be some normal over or undershoot at the time of going in and out of hold mode.

Figure 2 - Input Limiter Circuit

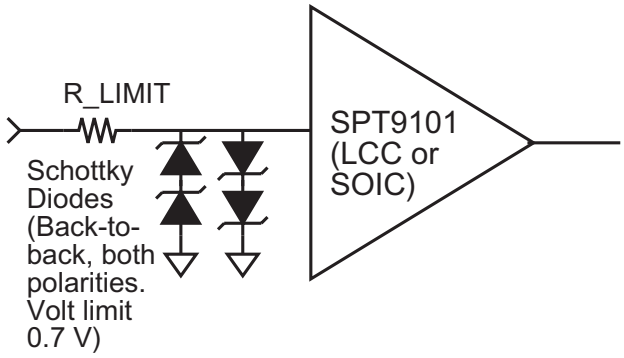


Table I - Parts List

#	Reference	Description	Part Number	Qty	Vendor
1	C1, 2	ECS-T1AY475R	Capacitor 4.7 µF, 10 V	2	Panasonic/Any
2	C3, 4	ECS-T1AY225R	Capacitor 2.2 µF, 10 V	2	Panasonic/Any
3	C5-C16	ECU-V1H103KBM	Chip Cap SMD 1206 .01 µF	12	Panasonic/Any
4	CLK_IN, $V_{IN}1$	901-144-8	PC Mount SMA Connector	3	Amphenol RF/ Any
5	FB1-2	EXC-ELSA-35	Ferrite Bead	2	Panasonic/Any
6	GND1-2, AGND, +5 V, -5.2 V, +5 PROTO -5 PROTO	40F6045	Test Point .075"	7	Newark/Any
7	R1	3266W-202-ND	Potentiometer, 2 Ω, 12T	1	Bourns/Any
8	R2	Omitted			
9	R3	0.0EBK-ND	Socketed Resistor, 1/8 W	1	Digi-Key
10	R4	51EBK-ND	Socketed Resistor, 1/8 W 5%	1	Digi-Key
11	R5,R13	ERJ-8ENF270	Resistor, 27 Ω SMD 1206	2	Panasonic/Any
12	R6-7	ERJ-8ENF102	Resistor, 1 kΩ SMD 1206	2	Panasonic/Any
13	R8, R14	ERJ-8ENF49R9	Resistor, 49.9 Ω SMD 1206	2	Panasonic/Any
14	R9-10	ERJ-8ENF151	Resistor, 150 Ω SMD 1206	2	Panasonic/Any
15	R11-12	ERJ-8ENF271	Resistor, 270 Ω SMD 1206	2	Panasonic/Any
16	U1	HCMP96850SID	H/S Comparator	1	Fairchild
17	U2	SPT9101SCP	Sample and Hold	0	Fairchild
18	U3	SPT9101SCP	Sample and Hold	0	Fairchild
19	N/A	EB9101 REV C	Printed Circuit Board	1	SAS
20	N/A	ED5045-ND	Sockets for Resistors	6	Digi-Key/Any
21	N/A	1902-ND	4-40 Nylon Hex Standoffs	4	Digi-Key/Any
22	N/A	H143-ND	Pan Head 4-40 Screws	4	Digi-Key/Any

Figure 3 - Detail Schematic

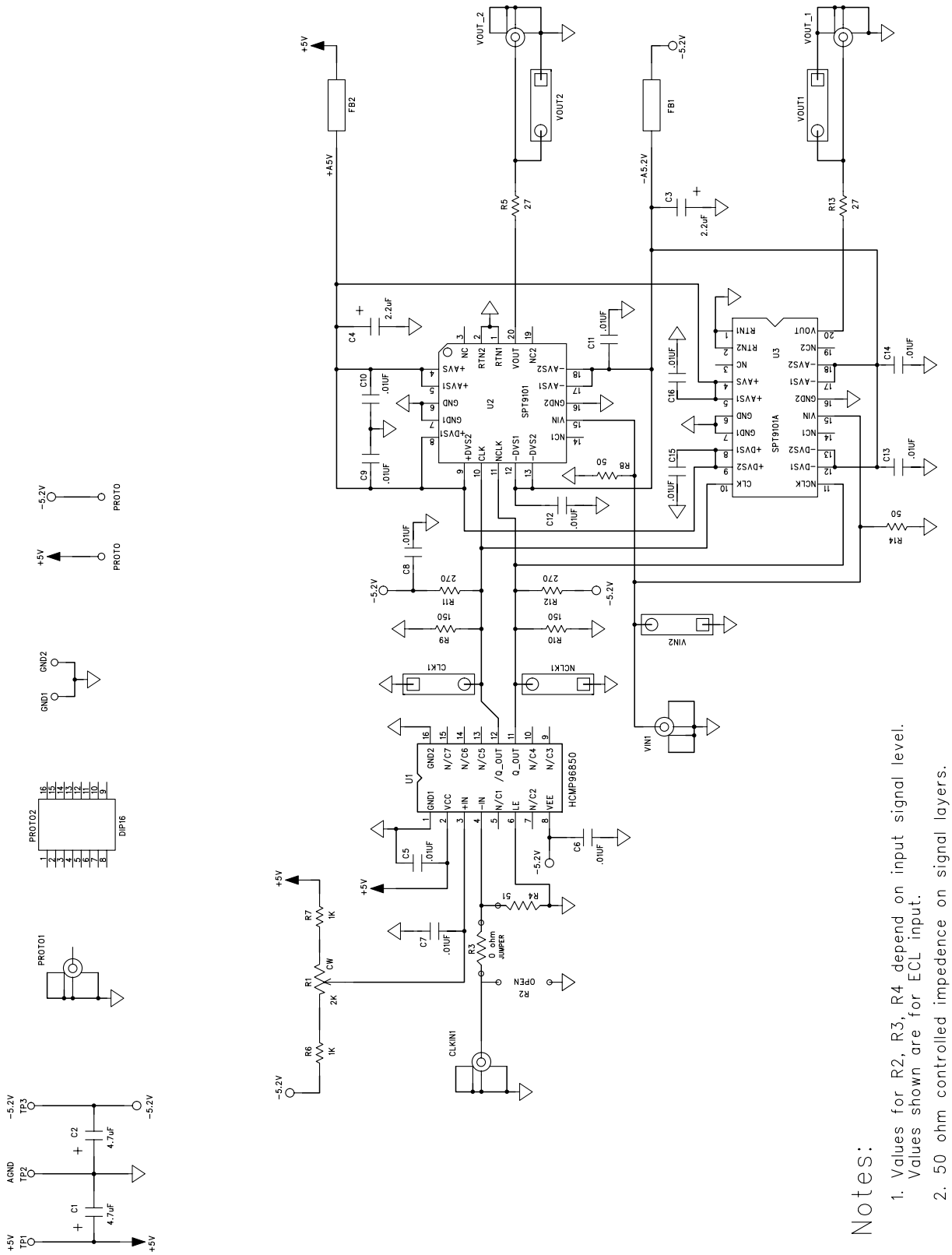


Figure 4 - Component Side Silk

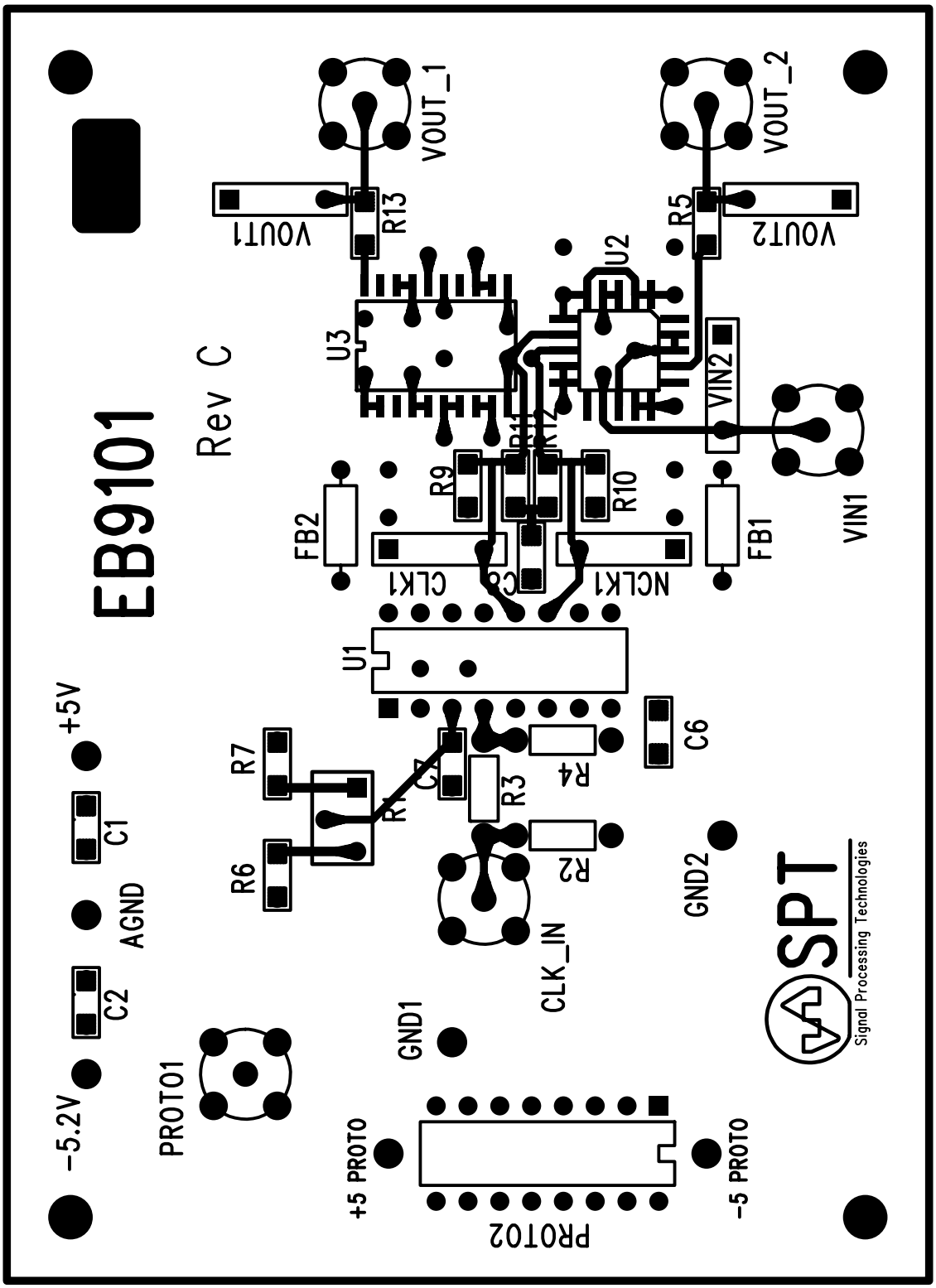
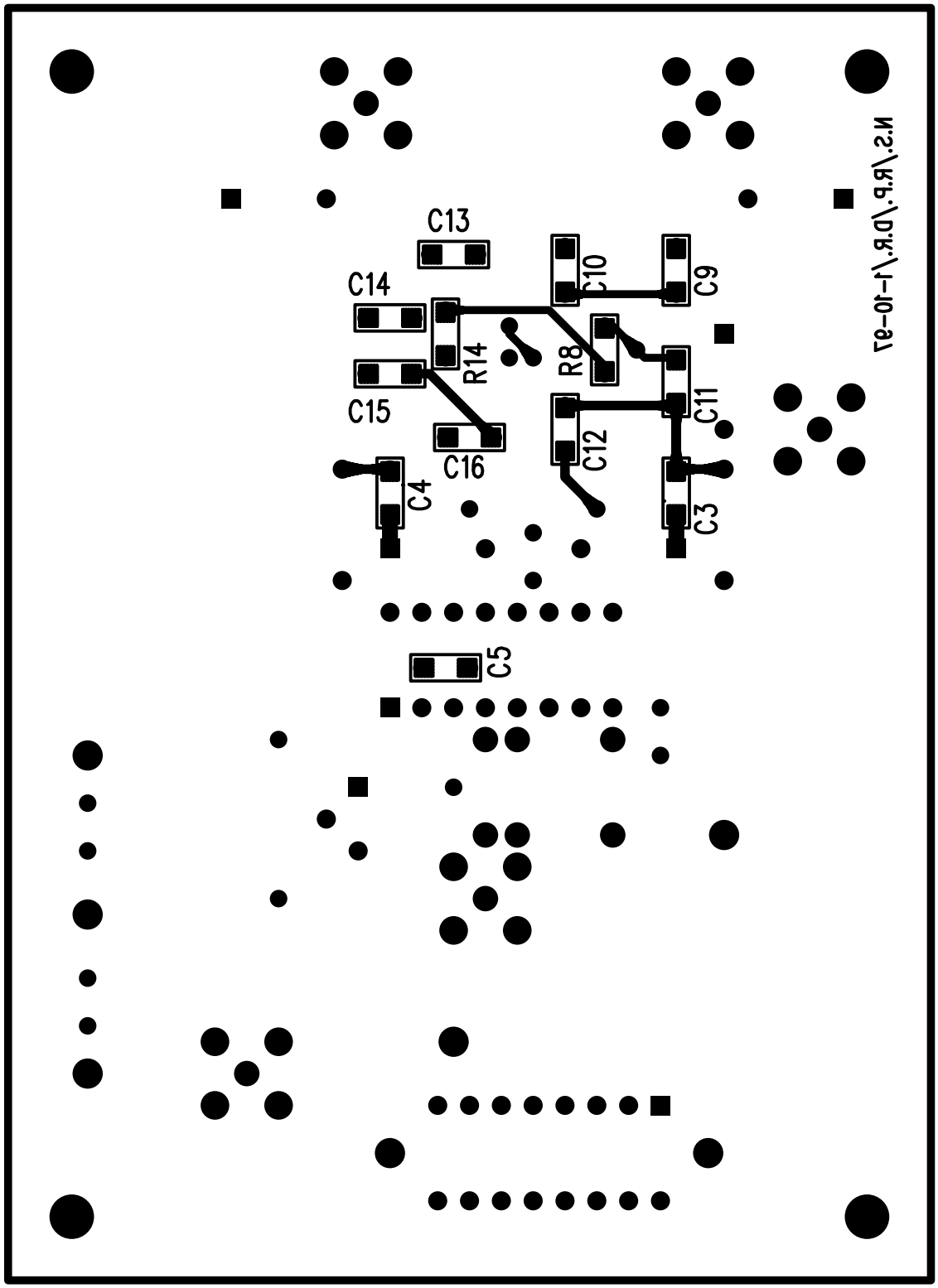


Figure 5 - Solder Side Silk



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