

## MAX31855PMB1 Peripheral Module

### General Description

The MAX31855PMB1 peripheral module provides the necessary hardware to interface the MAX31855 cold-junction compensated thermocouple-to-digital converter to any system that utilizes Pmod™-compatible expansion ports. The IC performs cold-junction compensation and digitizes the signal from a thermocouple. Versions of the IC are available that operate with a K-, J-, N-, T-, R-, or E-type thermocouple. This module is set up to operate with a K-type thermocouple. The data is output in a signed 14-bit, SPI-compatible, read-only format. This converter resolves temperatures to 0.25°C, allows readings as high as +1800°C and as low as -270°C, and exhibits thermocouple accuracy of  $\pm 2^\circ\text{C}$  for temperatures ranging from -200°C to +700°C for K-type thermocouples.

For full range accuracies, other thermocouple types, and detailed information regarding operation of the IC, refer to the MAX31855 IC data sheet.

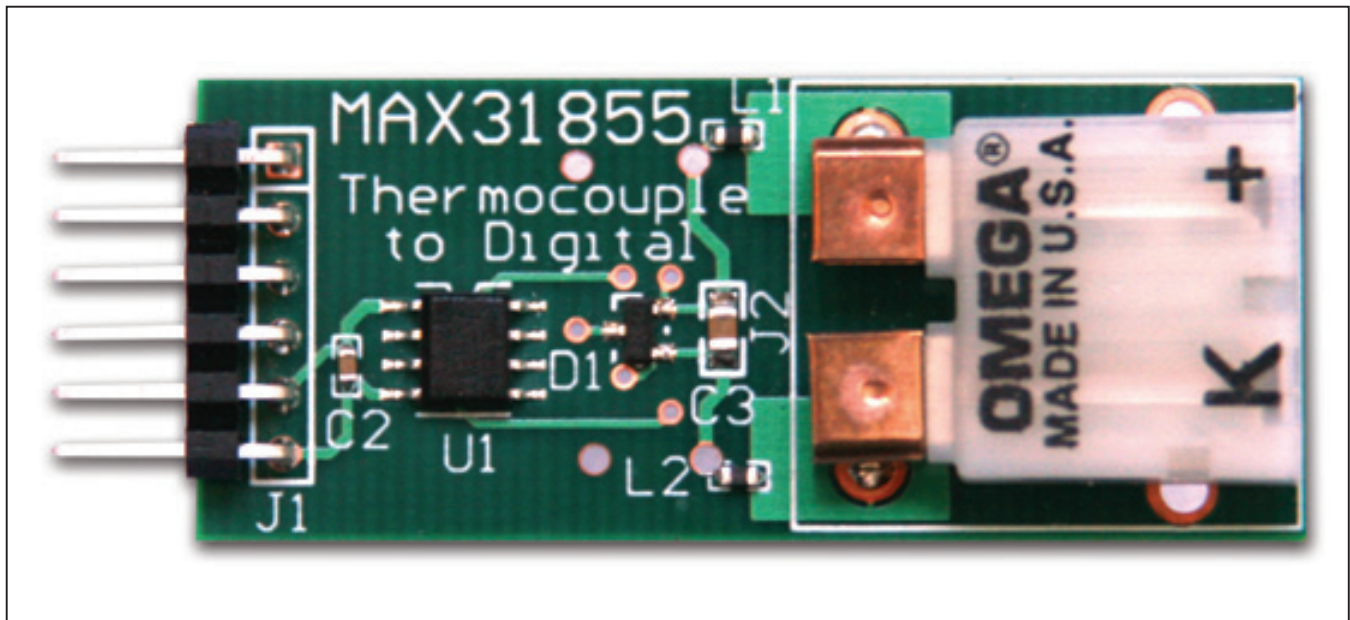
**Note:** K-type thermocouple is not included with Maxim Peripheral Module collections.

### Features

- ◆ Converts Output of a K-Type Thermocouple Directly to a Signed 14-Bit Digital Word
- ◆ Cold-Junction Compensation
- ◆ 14-Bit, 0.25°C Resolution
- ◆ Detects Thermocouple Shorts to GND or VCC
- ◆ Detects Open Thermocouple
- ◆ 6-Pin Pmod-Compatible Connector (SPI)
- ◆ Example Software Written in C for Portability
- ◆ RoHS Compliant
- ◆ Proven PCB Layout
- ◆ Fully Assembled and Tested

[Ordering Information](#) appears at end of data sheet.

### MAX31855PMB1 Photo



*Pmod is a trademark of Digilent Inc.*

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## Component List

| DESIGNATION | QTY | DESCRIPTION   |
|-------------|-----|---|
| C1, C4      | 0   | Not installed, ceramic capacitors (0805)  |
| C2          | 1   | 0.1 $\mu$ F $\pm$ 10%, 16V X7R ceramic capacitor (0603)<br>Murata GRM188R71C104KA01D  |
| C3          | 1   | 0.01 $\mu$ F $\pm$ 10%, 16V X7R ceramic capacitor (0603)<br>Murata GRM188R71C103KA01D |
| D1          | 1   | TVS diode (3 SOT3)<br>ON Semi NUP2105TL1G   |
| J1          | 1   | 6-pin right-angle male header   |

| DESIGNATION | QTY | DESCRIPTION  |
|-------------|-----|--|
| J2          | 1   | K-type thermocouple socket<br>Omega PCC-SMP-K-5-ROHS       |
| L1, L2      | 2   | 470 $\Omega$ ferrite beads (0603)<br>Murata BLM18PG471SN1D |
| R1, R2, R3  | 3   | 150 $\Omega$ $\pm$ 5% resistors (0603)                     |
| U1          | 1   | Thermocouple to digital IC (8 SO)<br>Maxim MAX31855KASA+   |
| —           | 1   | K-type thermocouple, mini plug*                            |
| —           | 1   | PCB: EPCB31855PM1  |

\* Thermocouple not included with Maxim peripheral module collections.

## Component Suppliers

| SUPPLIER                               | PHONE        | WEBSITE                     |
|--|--------------|-----------------------------|
| Murata Electronics North America, Inc. | 770-436-1300 | www.murata-northamerica.com |
| Omega Engineering                      | 888-826-6342 | www.omega.com               |
| ON Semiconductor                       | 602-244-6600 | www.onsemi.com              |

**Note:** Indicate that you are using the MAX31855PMB1 when contacting these component suppliers.

## Detailed Description

### SPI Interface

The MAX31855PMB1 peripheral module can plug directly into a Pmod-compatible port (configured for SPI) through connector J1. For information on the SPI protocol, refer to the MAX31855 IC data sheet.

Connector J1 provides connection of the module to the Pmod host. The pin functions and pin assignments adhere to the Pmod standard recommended by Digilent. See Table 1.

### Software and FPGA Code

Example software and drivers are available that execute directly without modification on several FPGA development boards that support an integrated or synthesized microprocessor. These boards include the Digilent Nexys 3, Avnet LX9, and Avnet ZEDBoard, although other platforms can be added over time. Maxim provides complete Xilinx ISE projects containing HDL, Platform Studio, and SDK projects. In addition, a synthesized bitstream, ready for FPGA download, is provided for the demonstration application.

**Table 1. Connector J1 (SPI Communication)**

| PIN | SIGNAL | DESCRIPTION  |
|-----|--------|--|
| 1   | SS     | Chip enable. Must be asserted low to enable the SPI interface. |
| 2   | N.C.   | Not connected  |
| 3   | MISO   | Serial-data output   |
| 4   | SCK    | Serial-clock input   |
| 5   | GND    | Ground   |
| 6   | VCC    | Power supply   |

The software project (for the SDK) contains several source files intended to accelerate customer evaluation and design. These include a base application (maximModules.c) that demonstrates module functionality and uses an API interface (maximDeviceSpecificUtilities.c) to set and access Maxim device functions within a specific module.

The source code is written in standard ANSI C format, and all API documentation including theory/operation, register description, and function prototypes are documented in the API interface file (maximDeviceSpecificUtilities.h & .c).

The complete software kit is available for download at [www.maxim-ic.com](http://www.maxim-ic.com). Quick start instructions are also available as a separate document.

# MAX31855PMB1 Peripheral Module

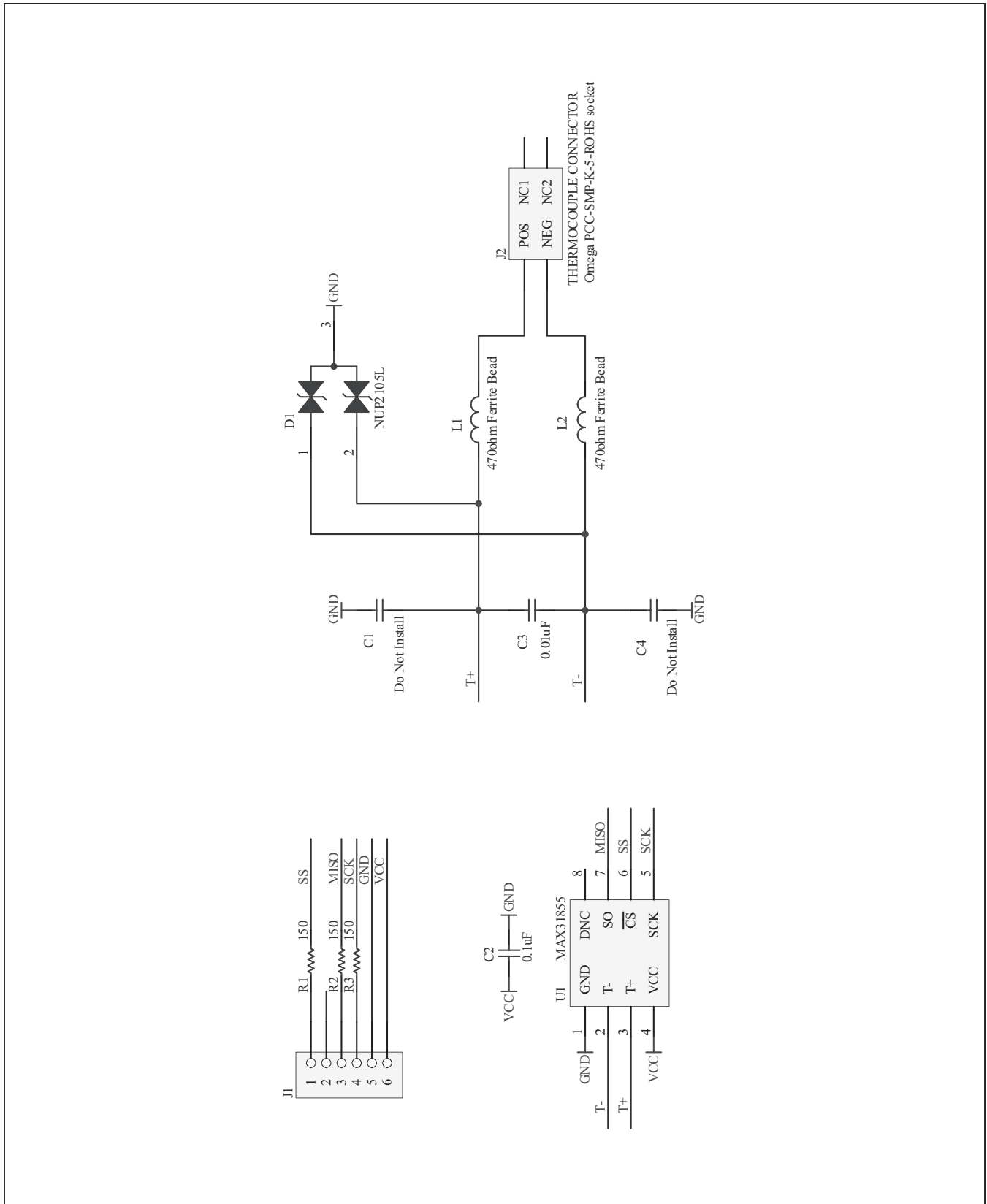


Figure 1. MAX31855PMB1 Peripheral Module Schematic

# MAX31855PMB1 Peripheral Module

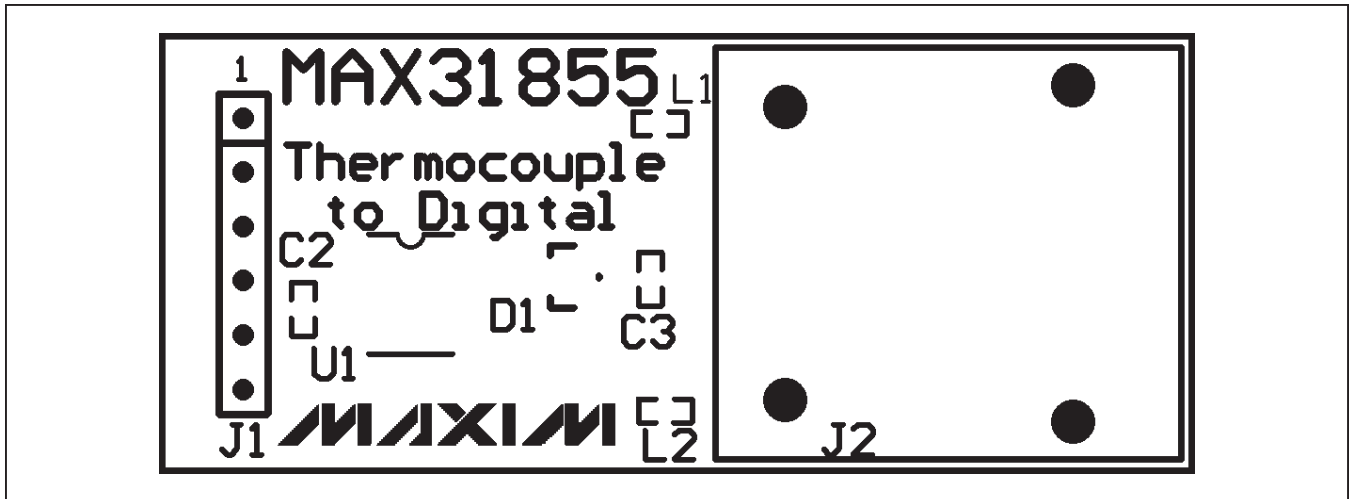


Figure 2. MAX31855PMB1 Peripheral Module Component Placement Guide—Component Side

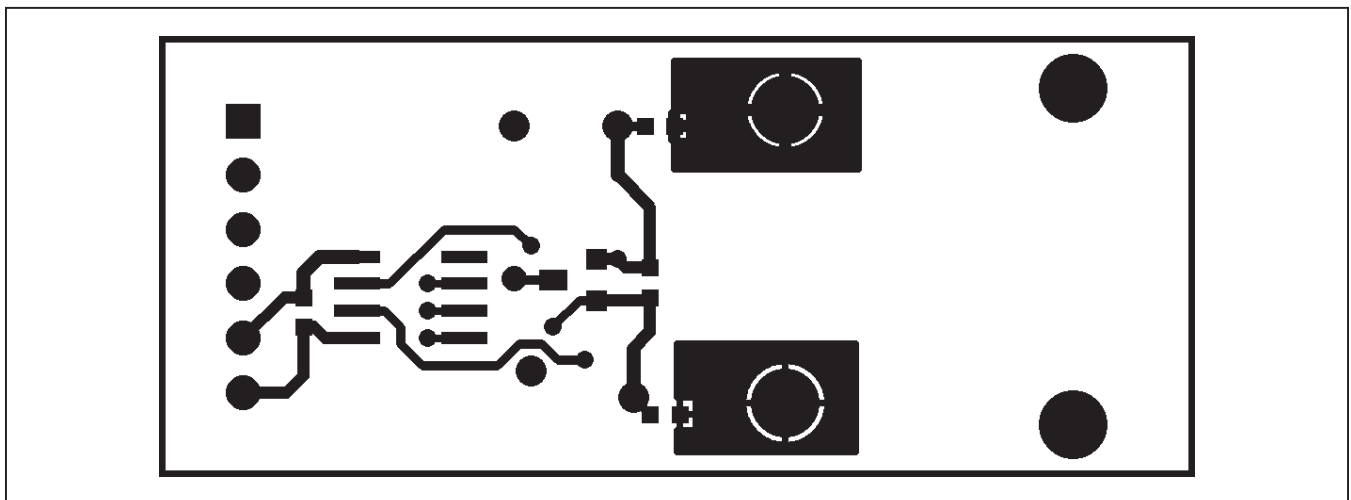


Figure 3. MAX31855PMB1 Peripheral Module PCB Layout—Component Side

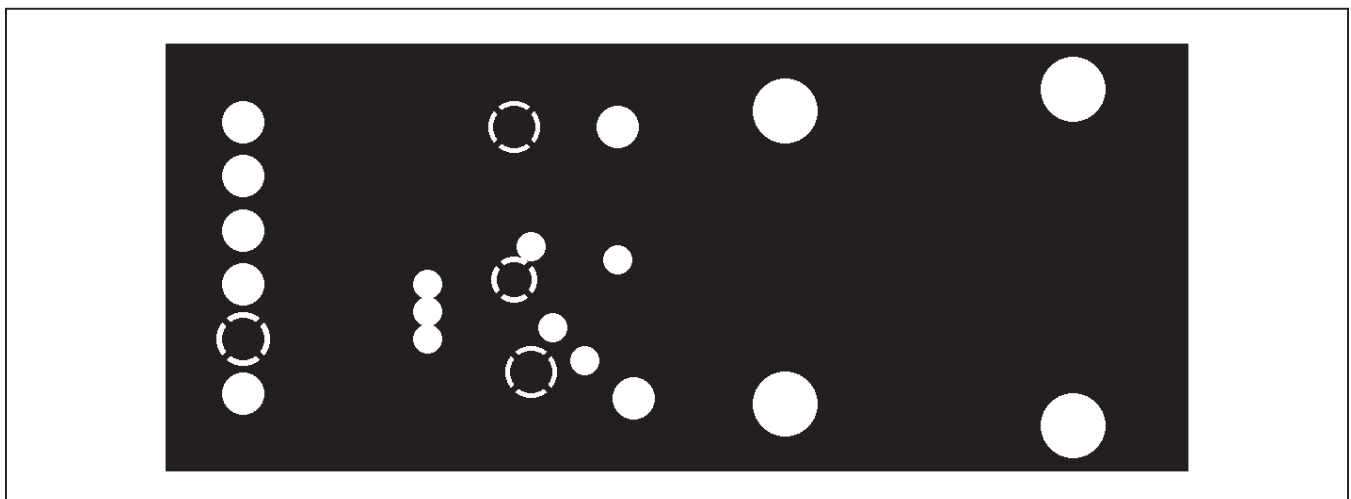


Figure 4. MAX31855PMB1 Peripheral Module PCB Layout—Inner Layer 1 (Ground)

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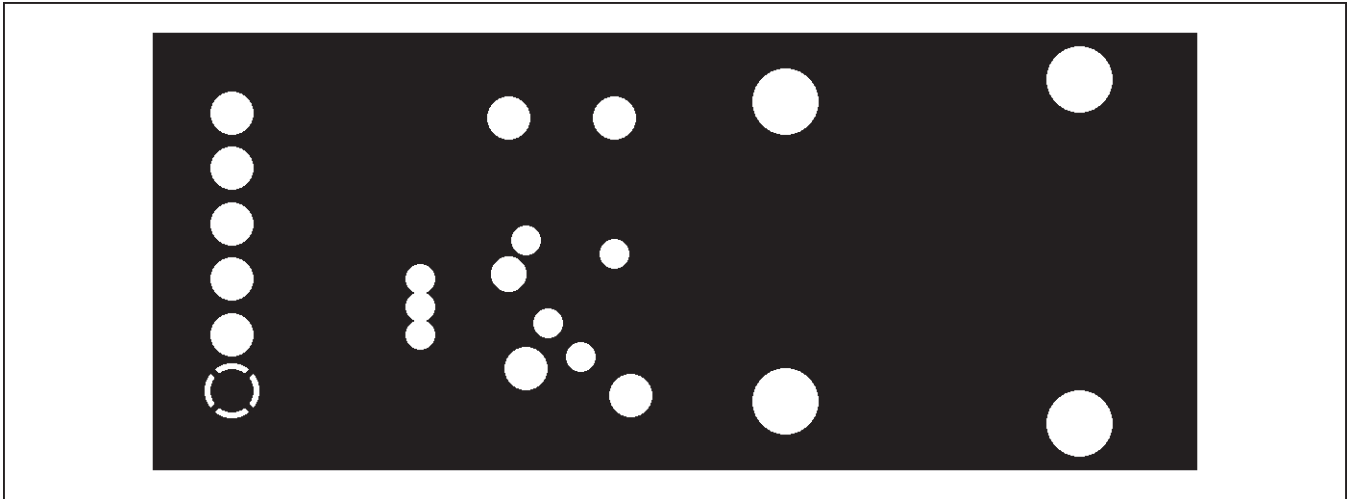


Figure 5. MAX31855PMB1 Peripheral Module PCB Layout—Inner Layer 2 (Power)

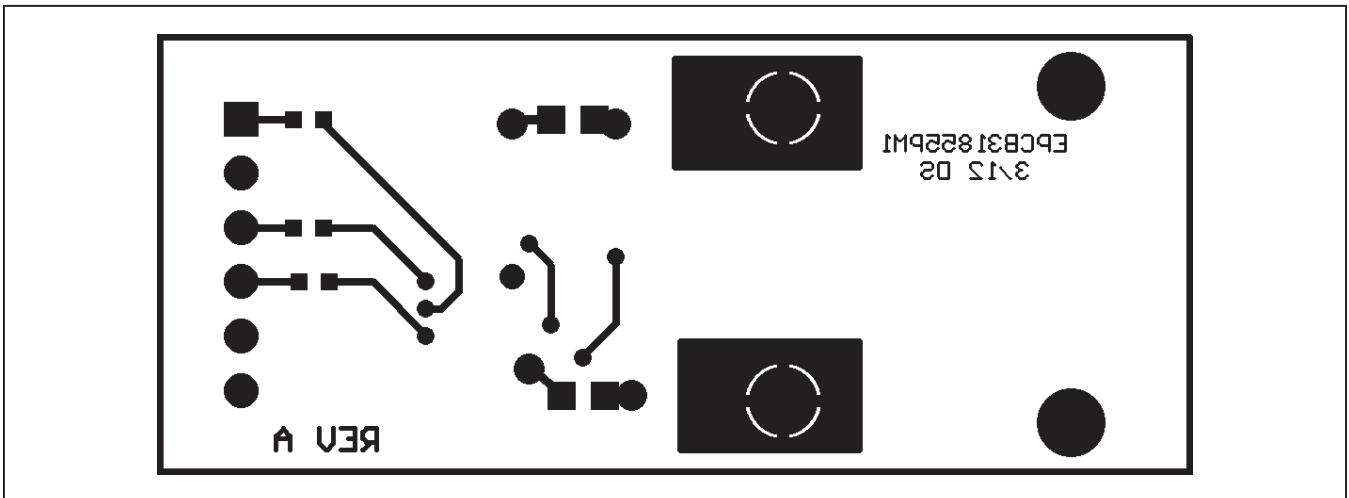


Figure 6. MAX31855PMB1 Peripheral Module PCB Layout—Solder Side

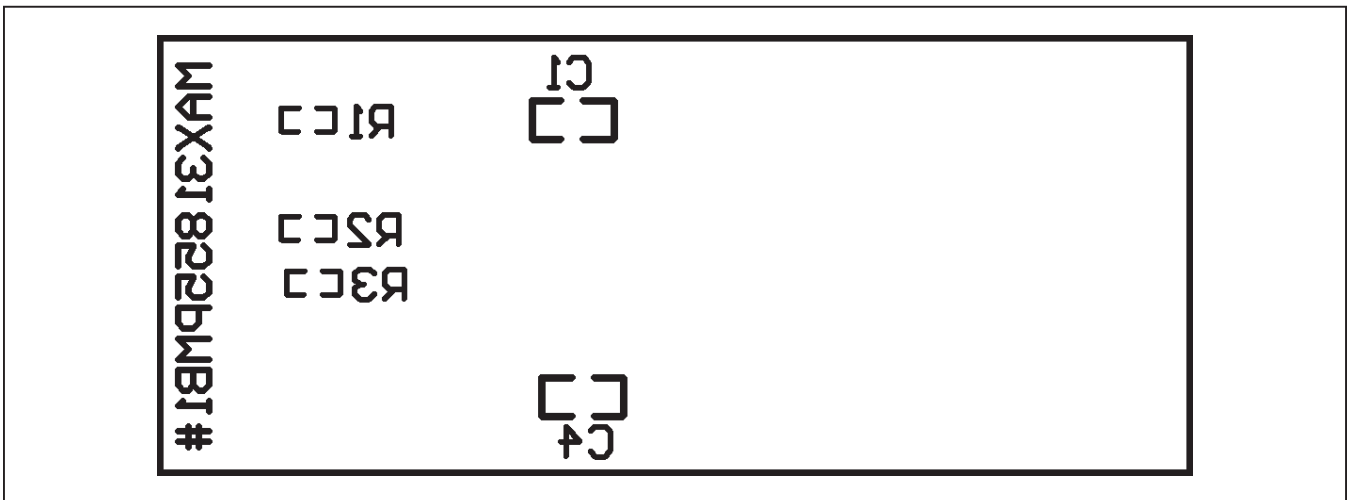


Figure 7. MAX31855PMB1 Peripheral Module Component Placement Guide—Solder Side

# MAX31855PMB1 Peripheral Module

## ***Ordering Information***

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| <b>PART</b>   | <b>TYPE</b>       |
|---------------|-------------------|
| MAX31855PMB1# | Peripheral Module |

#Denotes RoHS compliant.

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## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION     | PAGES CHANGED |
|-----------------|---------------|-----------------|---------------|
| 0               | 5/12          | Initial release | —             |

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