This datasheet is under modification and could not be completed in time for this CD-ROM. Before designing in, please be so kind as to contact your nearest OKI office or representative. The revised datasheet will be included in the next CD-ROM issue. Please also watch our web sites for further announcements. We sincerely apologise for any inconveniences.

Oki Electric Industry Co., Ltd., Tokyo, Japan
Device Business Group
Marketing Communications
tel: +81-3-5445-6027
fax: +81-3-5445-6058
email: brenner595@dm1.oii.oki.co.jp
http://www.oki.co.jp/semi/

Preliminary

OKI Semiconductor

This version: Jan. 1998
Previous version: Mar. 1996

MSM63182

Operatable at 0.9V and Built-in 512-dot LCD Driver 4-Bit Microcontroller

GENERAL DESCRIPTION

The MSM63182 is a CMOS 4-bit microcontroller to support dot matrix LCDs.
The MSM63182 has an OKI-original nX-4/250 CPU core.
The minimum instruction execution time is 1 μs (@ 2 MHz system clock).
The MSM63182 contains 4K-word program ememory, data memory (256 nibbles × 3.5 banks), two 4-bit input ports, four 4-bit output ports, three 4-bit input-output ports, LCD drivers for a maximum of 512 segments, and a buzzer output port.
The CMOS structure has realized a low power consumption.

APPLICATIONS

Games, pagers, data banks, etc.

FEATURES

- Rich instruction set
  Instructions : 439
  Transfer, rotate, increment/decrement, arithmetic operations, comparison, logic operations, mask operations, bit operations, ROM table reference, external memory transfer, stack operations, flag operations, branch, conditional branch, call/return, control.

- Rich selection of addressing modes
  Indirect addressing of four data memory types, with current bank register, extra bank register, HL register and XY register.
  Data memory bank internal direct addressing mode.

- Operating frequency
  Two clocks per machine cycle, with most instructions executed in one machine cycle.
  Minimum instruction execution time : 61 μs (@ 32.768 kHz system clock)
  : 1 μs (@ 2 MHz system clock)
  Low-speed clock : 32.768 kHz crystal oscillator
  High-speed clock : 2 MHz (Max.) RC or ceramic oscillator selectable

- Program memory space : 4K words
  Basic instruction length : 16 bits/1 word

- Data memory space : 256 nibbles x 3.5 banks
  (1bank for SFR,1bank for display register, 1.5 banks for data RAM)

- External data memory space : 64 Kbytes (expandable)

- Stack area
  - Call stack : 14 bits x 8 levels
  - Register stack : 16 bits x 16 levels

- I/O ports : Total 36
  - Input port : 2 ports x 4 bits
  - Selectable as input with pull-up resistor/input with pull-down resistor/high-impedance input
  - Output port : 4 ports x 4 bits
  - Selectable as P-channel open drain output/N-channel open drain output/CMOS output
  - Input-output port : 3 ports x 4 bits
  - Selectable as input with pull-up resistor/input with pull-down resistor/high-impedance input
  - Selectable as P-channel open drain output/N-channel open drain output/CMOS output
  - Can be interfaced with power supplies of external peripherals

- Buzzer output : One

- LCD driver : Total 48
  - Common driver : 16
  - Segment driver : 32
  - 1/1 to 1/16 duty : 512 segments (32 x 16) Max.
  - 1/4 or 1/5 bias
  - Selectable as all-on mode/all-off mode/power down mode/normal display mode, adjustable contrast

- Reset function
  - Reset through RESET pin
  - Power-on reset
  - Reset to low-speed oscillation halt

- Battery check
  - Low-voltage supply check

- Backup
  - Voltage doubler circuit operation (V_{DDH} level generator)

- Counter
  - Time-base counter : (15-bit) x 1
  - 1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz, 128 Hz output

- Interrupt
  External interrupt : 2
  Internal interrupt : 6
  (watchdog timer x 1, time base x 4, 100 Hz timer x 1)

- Chip size : 4.92 x 4.44 (mm^2)

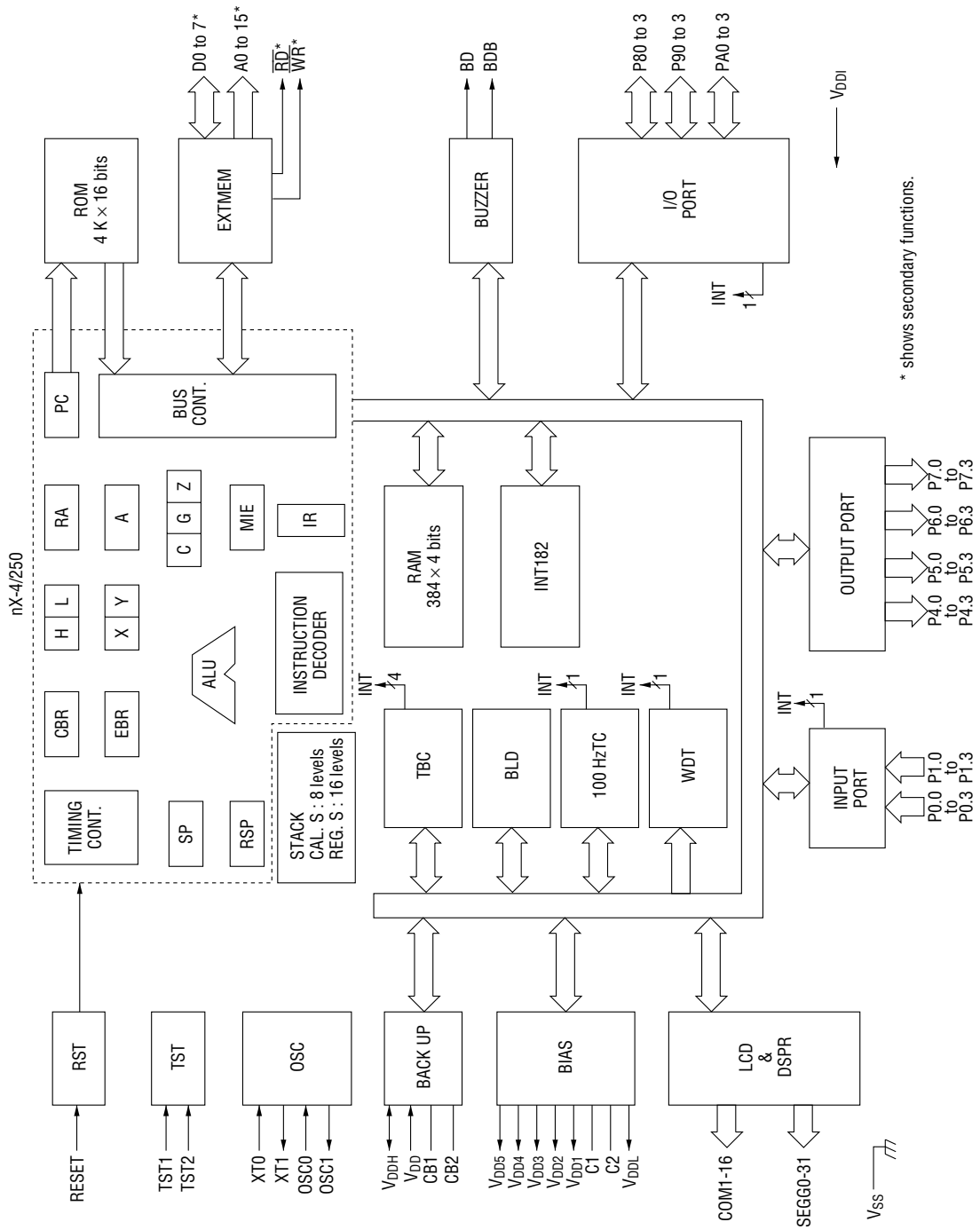
- Supply voltage
  With no backup : 0.9 V to 2.7 V (Maximum operating frequency 300 kHz)
  1.2 V to 2.7 V (Maximum operating frequency 500 kHz)
  1.5 V to 2.7 V (Maximum operating frequency 1 MHz)
  With backup : 1.8 V to 5.5 V (Maximum operating frequency 500 kHz)
  2.2 V to 5.5 V (Maximum operating frequency 1 MHz)
  2.7 V to 5.5 V (Maximum operating frequency 2 MHz)

- Package:
  128-pin Plastic QFP (QFP128-P-1420-0.50-K) (Product name : MSM63182-xxxGS-K)
  Chip (Product name : MSM63182-xxx)
  xxx indicates the code number.

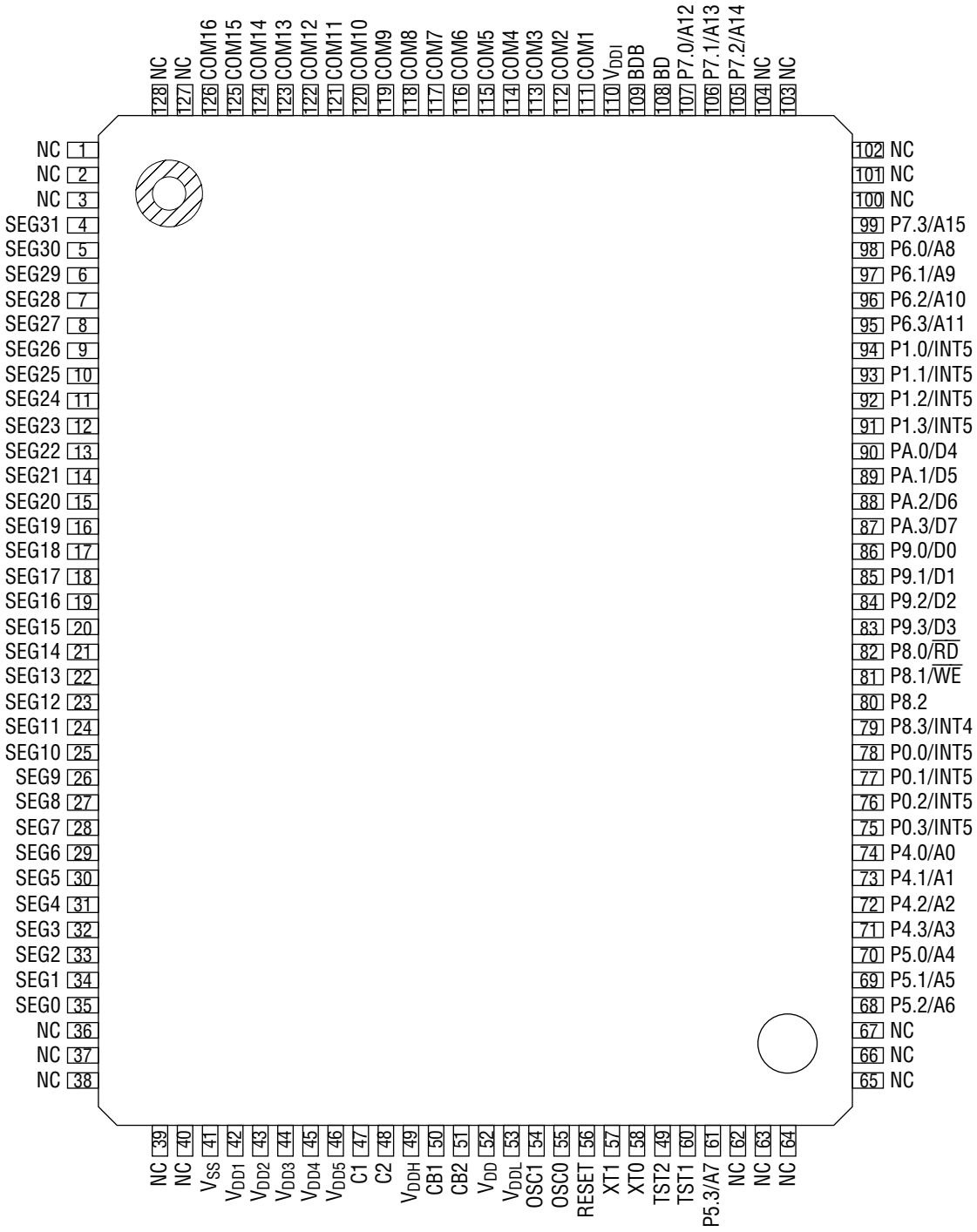
PROGRAM DEVELOPMENT ENVIRONMENT

- Cross assembler: ASM63KN
- Structured assembler: SASM63K
- Tool: EASE63180
- Debbuger: SID63K
- Loader: SETICE

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC: No-connection pin

128-Pin Plastic QFP

PIN DESCRIPTIONS

The basic functions of each pin on the MSM63182 are described in Table 1, and the secondary functions in Table 2.

Table 1-(a) Pin Descriptions (basic functions)

Function	Symbol	Pin	Type	Description
Power supply	V_{DD}	52	—	Positive power supply
	V_{SS}	41	—	Negative power supply
	V_{DD1}	42	—	LCD bias output
	V_{DD2}	43		
	V_{DD3}	44		
	V_{DD4}	45		
	V_{DD5}	46		
	C1	47	—	LCD bias output capacitor connection pin
	C2	48		
	V_{DDI}	110	—	External equipment interface supply (for ports P0 to PA)
	V_{DDL}	53	—	Positive power supply for internal logic (internally generated voltage)
	V_{DDH}	49	—	Step-up voltate supply
	CB1	50	—	Step-up voltage generation capacitor and connection
	CB2	51	—	
Oscillator	XT0	58	I	Low-speed clock oscillator pin: 32.768 kHz crystal oscillator and capacitor (C_G) connection
	XT1	57	O	
	OSC0	55	I	High-speed clock oscillator pin: Connect ceramic oscillator and capacitor (C_{L1}, C_{L2}) or external oscillation resistance (R_{OS}).
	OSC1	54	O	
Test	TST1	60	I	Test pin: Test pin: Pulled down to V_{SS} internally.
	TST2	59	I	
Reset	RESET	56	I	Reset input pin: When this pin drops from high to low impedance, internal reset occurs and execution begins from address 0000H. Pulled down to V_{SS} internally.
Buzzer	BD	108	O	Buzzer output pin: Output in normal or reversed phase.
	BDB	109	O	

Table 1-(b) Pin Descriptions (basic functions)

Function	Symbol	Pin	Type	Description
Ports	P0.0/INT5	78	I	4-bit input port: Selectable for pull-up resistor, pull-down resistor or high-impedance input for each bit. External interrupt is allocated as secondary functions.
	P0.1/INT5	77		
	P0.2/INT5	76		
	P0.3/INT5	75		
	P1.0/INT5	94	I	4-bit input port: Selectable for pull-up resistor, pull-down resistor or high-impedance input for each bit. External interrupt is allocated as secondary functions.
	P1.1/INT5	93		
	P1.2/INT5	92		
	P1.3/INT5	91		
	P4.0/A0	74	O	4-bit output port: Selectable for P-channel open drain output, N-channel open drain output or CMOS output for each bit. External memory access address bus allocated as secondary functions.
	P4.1/A1	73		
	P4.2/A2	72		
	P4.3/A3	71		
	P5.0/A4	70	O	4-bit output port: Selectable for P-channel open drain output, N-channel open drain output or CMOS output for each bit. External memory access address bus allocated as secondary functions.
	P5.1/A5	69		
	P5.2/A6	68		
	P5.3/A7	61		
	P6.0/A8	98	O	4-bit output port: Selectable for P-channel open drain output, N-channel open drain output or CMOS output for each bit. External memory access address bus allocated as secondary functions.
	P6.1/A9	97		
	P6.2/A10	96		
	P6.3/A11	95		
	P7.0/A12	107	O	4-bit output port: Selectable for P-channel open drain output, N-channel open drain output or CMOS output for each bit. External memory access address bus allocated as secondary functions.
	P7.1/A13	106		
	P7.2/A14	105		
	P7.3/A15	99		

Table 1-(c) Pin Descriptions (basic functions)

Function	Symbol	Pin	Type	Description
Port	P8.0/$\overline{RD}$	82	I/O	4-bit input-output port: For input mode, selectable for pull-up resistance, pull-down resistance or high-impedance input for each bit. For output mode, selectable for P-channel open drain output, N-channel open drain output or CMOS output for each bit. External memory access read/write signal and external interrupt allocated as secondary functions.
	P8.1/$\overline{WR}$	81		
	P8.2	80		
	P8.3/INT4	79		
	P9.0/D0	86	I/O	4-bit input-output port: For input mode, selectable for pull-up resistance, pull-down resistance or high-impedance input for each bit. For output mode, selectable for P-channel open drain output, N-channel open drain output or CMOS output for each bit. External memory access data bus signal allocated as secondary functions.
	P9.1/D1	85		
	P9.2/D2	84		
	P9.3/D3	83		
	PA.0/D4	90	I/O	4-bit input-output port: For input mode, selectable for pull-up resistance, pull-down resistance or high-impedance input for each bit. For output mode, selectable for P-channel open drain output, N-channel open drain output or CMOS output for each bit. External memory accrss data bus signal allocated as secondary functions.
	PA.1/D5	89		
	PA.2/D6	88		
	PA.3/D7	87		

Table 1-(d) Pin Descriptions (basic functions)

Funciton	Symbol	Pin	Type	Description
LCD	COM1	111	O	LCD common signal output pins
	COM2	112		
	COM3	113		
	COM4	114		
	COM5	115		
	COM6	116		
	COM7	117		
	COM8	118		
	COM9	119		
	COM10	120		
	COM11	121		
	COM12	122		
	COM13	123		
	COM14	124		
	COM15	125		
	COM16	126		
	SEG0	35	O	LCD segment signal output pins
	SEG1	34		
	SEG2	33		
	SEG3	32		
	SEG4	31		
	SEG5	30		
	SEG6	29		
	SEG7	28		
	SEG8	27		
	SEG9	26		
	SEG10	25		
	SEG11	24		
	SEG12	23		
	SEG13	22		
	SEG14	21		
	SEG15	20		
	SEG16	19		
	SEG17	18		
	SEG18	17		
	SEG19	16		
	SEG20	15		
	SEG21	14		
	SEG22	13		
	SEG23	12		
	SEG24	11		
	SEG25	10		
	SEG26	9		

Table 1-(e) Pin Descriptions (basic functions)

Function	Symbol	Pin	Type	Description
LCD	SEG27	8	O	LCD segment signal output pins
	SEG28	7		
	SEG29	6		
	SEG30	5		
	SEG31	4		

Table 2-(a) Pin Descriptions (secondary functions)

Function	Symbol	Pin	Type	Description
External interrupt	P0.0/INT5	78	I	P0.0 to P0.3, P1.0 to P1.3 secondary functions: External interrupt input pin. Interrupt to level change supported. Each bit may be enabled/disabled with port 0 interrupt enable register (P0IE) and port 1 interrupt enable register (P1IE).
	P0.1/INT5	77		
	P0.2/INT5	76		
	P0.3/INT5	75		
	P1.0/INT5	94		
	P1.1/INT5	93		
	P1.2/INT5	92		
	P1.3/INT5	91		
	P8.3/INT4	79	I	P8.3 secondary function: External interrupt input pin. Interrupt to level change supported.

Table 2-(b) Pin Descriptions (secondary functions)

Function	Symbol	Pin	Type	Description
External memory	P4.0/A0	74	O	P4, P5, P6, P7 secondary functions: Address bus signals for external memory access
	P4.1/A1	73		
	P4.2/A2	72		
	P4.3/A3	71		
	P5.0/A4	70		
	P5.1/A5	69		
	P5.2/A6	68		
	P5.3/A7	61		
	P6.0/A8	98		
	P6.1/A9	97		
	P6.2/A10	96		
	P6.3/A11	95		
	P7.0/A12	107		
	P7.1/A13	106		
	P7.2/A14	105		
	P7.3/A15	99		
	P9.0/D0	86	I/O	P9, PA secondary functions: Data bus signals for external memory access
	P9.1/D1	85		
	P9.2/D2	84		
	P9.3/D3	83		
	PA.0/D4	90		
	PA.1/D5	89		
	PA.2/D6	88		
	PA.3/D7	87		
	P8.0/$\overline{RD}$	82	O	P8.0 secondary function: Read signal (negative logic) for external memory access.
	P8.1/$\overline{WR}$	81	O	P8.1 secondary function: Write signal (negative logic) for external memory access.

MEMORY MAPS

Program memory space

The program memory space is used for program data.
It has a 16-bit data length, allocated from addresses 0H to 0FDFH. ROM table data, as well as the program data, can be stored in the program memory space. The program memory space configuration is indicated in Fig. 3.

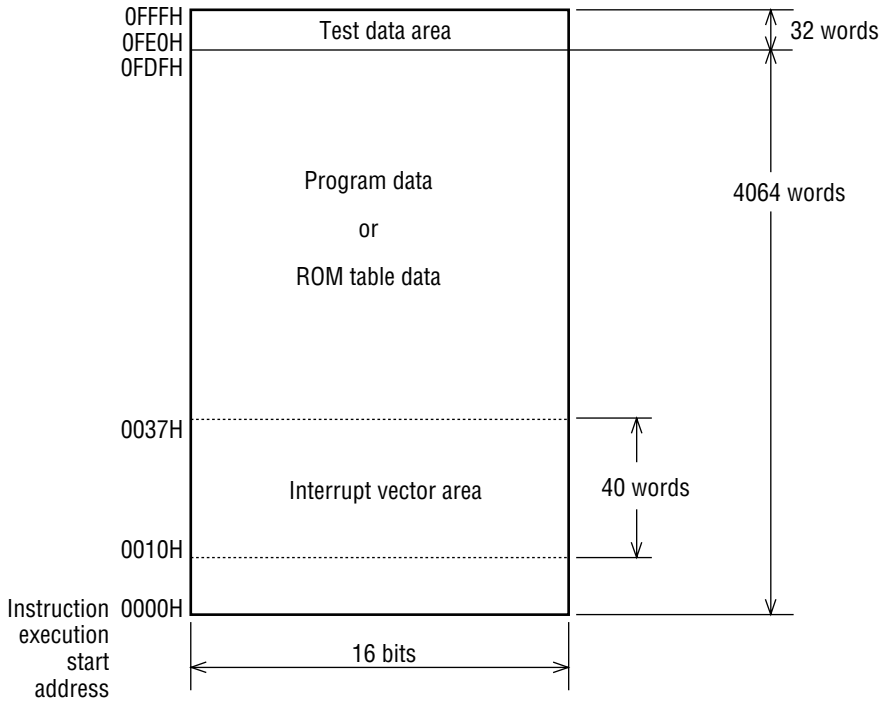


Fig. 3 Program Memory Space Configuration

Address 0000H is the instruction execution start address used after system reset. The interrupt area from 0010H to 0037H includes the interrupt processing routine start address when an send interrupt is generated.
ROM table data is transferred to data memory by the ROM table reference instruction. The 32 words from 0FE0H to 0FFFH are a test data area and cannot be used as a program memory area.

Data memory space

As indicated in Fig. 4, the data memory consists of 3.5 banks, with each bank unit having 256 nibbles in size. Bank 0 is assigned to SFR space, bank 1 is assigned to LCD display registers, and banks 2 to 3.5 (384 nibbles) are assigned to data RAM.

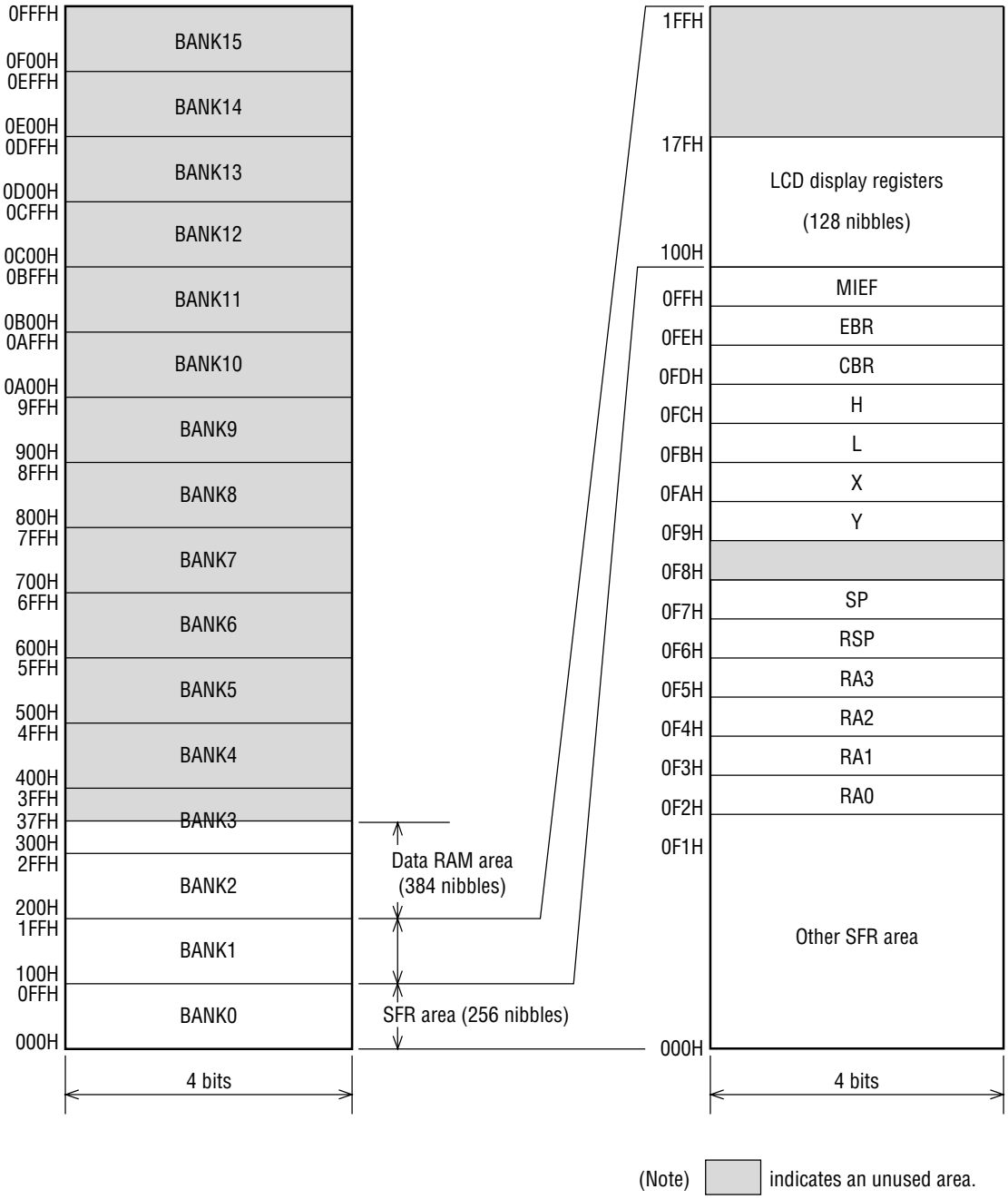


Fig. 4 Data Memory Space Configuration

External memory space

The external memory space has an 8-bit data length, allocated from address 0 to address 0FFFFH. It is configured as indicated in Fig. 5.

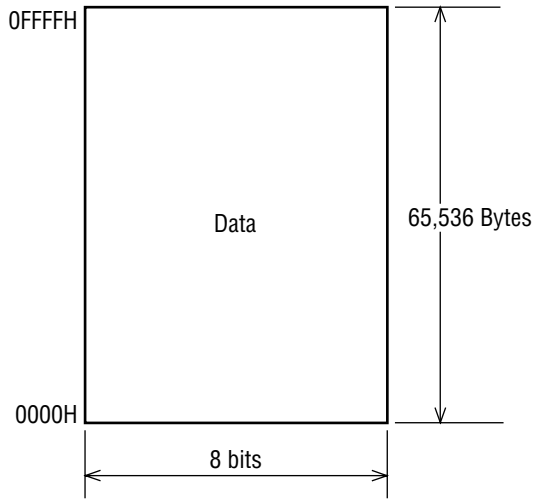


Fig. 5 External Memory Space Configuration

ABSOLUTE MAXIMUM RATINGS (when power supply is backed up or not)

(V_{SS}=0 V)

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage 1	V_{DD1}	Ta = 25°C	–0.3 to +1.6	V
Supply Voltage 2	V_{DD2}	Ta = 25°C	–0.3 to +2.9	V
Supply Voltage 3	V_{DD3}	Ta = 25°C	–0.3 to +4.2	V
Supply Voltage 4	V_{DD4}	Ta = 25°C	–0.3 to +5.5	V
Supply Voltage 5	V_{DD5}	Ta = 25°C	–0.3 to +6.8	V
Supply Voltage 6	V_{DD}	When backed up, Ta = 25°C	–0.3 to +3.0	V
		When not backed up, Ta = 25°C	–0.3 to +6.0	V
Supply Voltage 7	V_{DDI}	Ta = 25°C	–0.3 to +6.0	V
Supply Voltage 8	V_{DDH}	Ta = 25°C	–0.3 to +6.0	V
Supply Voltage 9	V_{DDL}	Ta = 25°C	–0.3 to +6.0	V
Input Voltage 1	V_{IN1}	V_{DD} Input, Ta=25°C	–0.3 to V_{DD}+0.3	V
Input Voltage 2	V_{IN2}	V_{DDI} Input, Ta=25°C	–0.3 to V_{DDI}+0.3	V
Output Voltage 1	V_{OUT1}	V_{DD1} Output, Ta=25°C	–0.3 to V_{DD1}+0.3	V
Output Voltage 2	V_{OUT2}	V_{DD2} Output, Ta=25°C	–0.3 to V_{DD2}+0.3	V
Output Voltage 3	V_{OUT3}	V_{DD3} Output, Ta=25°C	–0.3 to V_{DD3}+0.3	V
Output Voltage 4	V_{OUT4}	V_{DD4} Output, Ta=25°C	–0.3 to V_{DD4}+0.3	V
Output Voltage 5	V_{OUT5}	V_{DD5} Output, Ta=25°C	–0.3 to V_{DD5}+0.3	V
Output Voltage 6	V_{OUT6}	V_{DD} Output, Ta=25°C	–0.3 to V_{DD}+0.3	V
Output Voltage 7	V_{OUT7}	V_{DDI} Output, Ta=25°C	–0.3 to V_{DDI}+0.3	V
Output Voltage 8	V_{OUT8}	V_{DDH} Output, Ta=25°C	–0.3 to V_{DDH}+0.3	V
Storage Temperature	T_{STG}	—	–55 to +125	°C

RECOMMENDED OPERATING CONDITIONS (when power supply is backed up)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T_{op}	—	–20 to +70	°C
Operating Voltage	V_{DD}	—	0.9 to 2.7	V
	V_{DDI}	—	0.9 to 5.5	V
Crystal OSC Frequency	f_{XT}	—	30 to 35	kHz
Ceramic Oscillation Frequency	f_{CM}	V_{DD}=0.9 to 2.7 V	300k max.	Hz
		V_{DD}=1.2 to 2.7 V	500k max.	
		V_{DD}=1.5 to 2.7 V	1M max.	
RC Oscillator External Resistance	R_{OS}	V_{DD}=0.9 to 2.7 V	200 to 300	kΩ
		V_{DD}=1.2 to 2.7 V	100 to 300	
		V_{DD}=1.5 to 2.7 V	50 to 300	

RECOMMENDED OPERATING CONDITIONS (when power supply is backed up)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T_{op}	—	–20 to +70	°C
Operating Voltage	V_{DD}	—	1.8 to 5.5	V
	V_{DDI}	—	1.8 to 5.5	V
Crystal OSC Frequency	f_{XT}	—	30 to 35	kHz
Ceramic Oscillation Frequency	f_{CM}	V_{DD}=1.8 to 5.5 V	500k max.	Hz
		V_{DD}=2.2 to 5.5 V	1M max.	
		V_{DD}=2.7 to 5.5 V	2M max.	
RC Oscillator External Resistance	R_{OS}	V_{DD}=1.8 to 5.5 V	100 to 300	kΩ
		V_{DD}=2.2 to 5.5 V	50 to 300	
		V_{DD}=2.7 to 5.5 V	30 to 300	

ELECTRICAL CHARACTERISTICS

DC Characteristics (when power supply is backed up or not)

(V_{DD}=V_{DDI}=3.0 V, V_{SS}=0 V, Ta=–20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{DD1} Voltage	V_{DD1}	—	Typ.–0.2	1/2*V_{DD2}	Typ.+0.2	V	
V_{DD2} Voltage	V_{DD2}	—	Vr–0.2	Vr	Vr+0.2	V	
V_{DD3} Voltage	V_{DD3}	—	Typ.–0.3	3/2*V_{DD2}	Typ.+0.3	V	
V_{DD4} Voltage	V_{DD4}	—	Typ.–0.4	2*V_{DD2}	Typ.+0.4	V	
V_{DD5} Voltage	V_{DD5}	—	Typ.–0.5	5/2*V_{DD2}	Typ.+0.5	V	
V_{DDH} Voltage (with back up)	V_{DDH}	V_{DD}=1.5 V High-speed clock oscillaiton stops Ch, Cb12=1µF	2.8	—	3.0	V	
		V_{DD}=1.5 V High-speed clock oscillation Ceramic oscillation, 1 MHz Ch, Cb12=1µF	2.0	—	2.7	V	
V_{DDL} Voltage	V_{DDL}	High-speed clock oscillaiton stops	1.0	1.5	2.0	V	
		High-speed clock oscillation	1.8	—	5.5	V	1
XTOSC Oscillation Start Voltage	V_{STA}	Oscillation starts in 5 seconds.	0.9	—	—	V	
XTOSC Oscillation Hold Voltage	V_{HOLD}	With back up	0.85	—	—	V	
		With no back up	1.7	—	—	V	
XTOSC Stop Detect Time	T_{STOP}	—	0.1	—	1000	ms	
XTOSC External Capacitance	C_G	—	10	—	30	pF	
XTOSC Internal Capacitance	C_D	—	12	15	20	pF	
Ceramic Oscillation External Capacitance	CL0, 1	Ceramic oscillation 1 MHz, 2 MHz	—	30	—	pF	
RCOSC Internal Capacitance	C_{OS}	—	8	12	16	pF	
POR Voltage	V_{POR1}	V_{DD}=1.5 V	0	—	0.4	V	
		—	0	—	0.7	V	
Non-POR Voltage	V_{POR2}	V_{DD}=1.5 V	1.2	—	1.5	V	
		—	2.0	—	3.0	V	

Notes: 1. "Vr" changes in the range from 1.8 V to 2.4 V according to the value of Display Contrast Transistor (DSPCNT).
2. "XTOSC" indicates a 32.768 kHz crystal oscillation circuit.
3. T_{STOP} indicates that the system is reset if XTOSC is inoperative over the value of T_{STOP}.
4. "POR" denotes Power ON Reset.
5. "V_{POR1}" indicates that POR occurs when V_{DD} falls from 3.0 V (1.5 V) to V_{POR1} and again rises up to 3.0 V (1.5 V).
6. V_{POR2} indicates that POR does not occur when V_{DD} falls from 3.0 V (1.5 V) to V_{POR2} and again rises up to 3.0 V (1.5 V).

DC Characteristics (when power supply is backed up)

(V_{DD}=V_{DDI}=1.5 V, V_{SS}=0 V, Ta=–20 to +70°C unless otherwise specified)

(1/3)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Current Consumpiton 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stops)	—	6	35	µA	1
Current Consumption 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High frequency clock oscillation stops)	—	4.6	30	µA	
Current Consumpiton 3	I_{DD3}	CPU is in operating state. (High-speed clock oscillation stops)	—	17.0	40	µA	
Current Consumpiton 4	I_{DD4}	CPU is in operating at high-speed oscillaiton (RC oscillation, R_{OS}=51 kΩ)	—	550	700	µA	
Current Consumpiton 5	I_{DD5}	CPU is in operating at high-speed oscillaiton (Ceramic oscillation 1 MHz)	—	600	700	µA	

DC Characteristics (when power supply is backed up)

(V_{DD}=V_{DDI}=V_{DDL}=1.5 V, V_{SS}=0 V, V_{DD1}=1.1 V, V_{DD2}=2.2 V, V_{DD3}=3.3 V, V_{DD4}=4.4 V, V_{DD5}=5.5 V, V_{DDH}=3 V, Ta=–20 to +70°C unless otherwise specified)

(2/3)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P4.0 to P4.3) (P5.0 to P5.3) (P6.0 to P6.3) ⋮ (P9.0 to P9.3) (PA.0 to PA.3)	I_{OH1}	V_{OH1}=V_{DDI}–0.5 V	–2.0	–1.2	–0.4	mA	
	I_{OL1}	V_{OL1}=0.5 V	0.4	1.2	2.0	mA	
	I_{OH1S}	V_{DDI}=5 V, V_{OH1S}=V_{DDI}–0.5 V	–8	–4	–2	mA	
	I_{OL1S}	V_{DDI}=5 V, V_{OL1S}=0.5 V	2	4	8	mA	
Output Current 2 (BD, BDB)	I_{OH2}	V_{OH2}=V_{DD}–0.7 V	–2.5	–1.3	–0.5	mA	
	I_{OL2}	V_{OL2}=0.7 V	0.5	1.3	2.5	mA	
Output Current 3 (SEG0 to SEG31) (COM1 to COM16)	I_{OH3}	V_{DD3}=V_{DD5}–0.2 V(V_{DD5} level)	—	—	–4	µA	2
	I_{OHM3}	VOHM3=V_{DD4}+0.2 V(V_{DD4} level)	4	—	—	µA	
	I_{OHM3S}	VOHM3S=V_{DD4}–0.2 V(V_{DD4} level)	—	—	–4	µA	
	I_{OMH3}	VOMH3=V_{DD3}+0.2 V(V_{DD3} level)	4	—	—	µA	
	I_{OMH3S}	VOMH3S=V_{DD3}–0.2 V(V_{DD3} level)	—	—	–4	µA	
	I_{OML3}	VOML3=V_{DD2}+0.2 V(V_{DD2} level)	4	—	—	µA	
	I_{OML3S}	VOML3S=V_{DD2}–0.2 V(V_{DD2} level)	—	—	–4	µA	
	I_{OLM3}	VOLM3=V_{DD1}+0.2 V(V_{DD1} level)	4	—	—	µA	
	I_{OLM3S}	VOLM3S=V_{DD1}–0.2 V(V_{DD1} level)	—	—	–4	µA	
	I_{OL3}	V_{OL3}=V_{SS}+0.2 V(V_{SS} level)	4	—	—	µA	
Output Current 4 (OSC1)	I_{OH4R}	V_{OH4R}=V_{DDH}–0.5 V(RC osc mode)	–2.5	–1.5	–0.75	mA	
	I_{OL4R}	V_{OL4R}=0.5 V(RC osc mode)	0.75	1.5	2.5	mA	
	I_{OH4C}	V_{OH4C}=V_{DDH}–0.5 V(Ceramic osc mode)	–200	–100	–50	µA	
	I_{OL4C}	V_{OL4C}=0.5 V(Ceramic osc mode)	50	100	200	µA	
Output Leakage (P4.0 to P4.3) (P5.0 to P5.3) (P6.0 to P6.3) ⋮ (PA.0 to PA.3)	I_{OOH}	V_{OH}=V_{DDI}	—	—	0.3	µA	
	I_{OOL}	V_{OL}=V_{SS}	–0.3	—	—	µA	

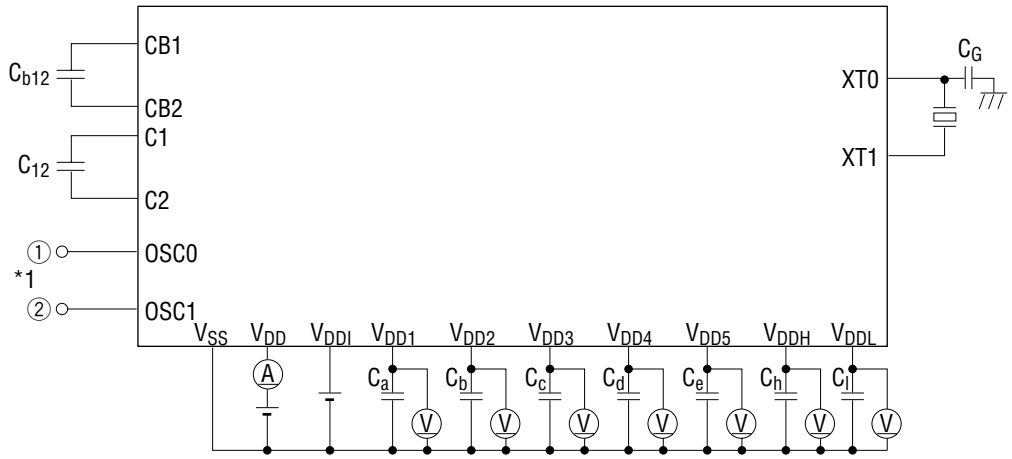
DC Characteristics (when power supply is backed up)

(V_{DD}=V_{DDI}=V_{DDL}=1.5 V, V_{SS}=0 V, V_{DD1}=1.1 V, V_{DD2}=2.2 V, V_{DD3}=3.3 V, V_{DD4}=4.4 V, V_{DD5}=5.5 V, V_{DDH}=3 V, Ta=–20 to +70°C unless otherwise specified)

(3/3)

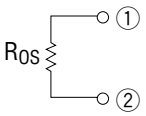
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0-P0.3) (P1.0-P1.3) (P8.0-P8.3) (P9.0-P9.3) ⋮ (PA.0-PA.3)	I_{IH1}	V_{IH1}=V_{DDI}(pulldown)	2	10	30	µA	3
	I_{IL1}	V_{IL1}=V_{SS}(pullup)	–30	–10	–2	µA	
	I_{IH1S}	V_{IH1}=V_{DDI}=5 V(pulldown)	70	250	600	µA	
	I_{IL1S}	V_{IL1}=0 V, V_{DDI}=5 V(pullup)	–600	–250	–70	µA	
	I_{IH1Z}	V_{IH1}=V_{DDI}(High impedance)	0	—	1	µA	
	I_{IL1Z}	V_{IL1}=V_{SS}(high impedance)	–1	—	0	µA	
Input Current 2 (OSC0)	I_{IL2}	V_{IL2}=V_{SS}(pullup)	–200	–110	–30	µA	
	I_{IH2R}	V_{IH2}=V_{DDH}(RC oscillation)	0	—	1	µA	
	I_{IL2R}	V_{IL2}=V_{SS}(RC oscillation)	–1	—	0	µA	
	I_{IH2C}	V_{IH2}=V_{DDH}(Ceramic oscillation)	0.1	0.5	1.0	µA	
	I_{IL2C}	V_{IL2}=V_{SS}(Ceramic oscillation)	–1	–0.5	–0.1	µA	
Input Current 3 (RESET)	I_{IH3}	V_{IH3}=V_{DD}	10	50	80	µA	
	I_{IL3}	V_{IL3}=V_{SS}	–1	—	0	µA	
Input Current 4 (TST1, TST2)	I_{IH4}	V_{IH4}=V_{DD}	50	150	300	µA	
	I_{IL4}	V_{IL4}=V_{SS}	–1	—	0	µA	
Input Voltage 1 (P0.0-P0.3) (P1.0-P1.3) (P8.0-P8.3) (P9.0-P9.3) ⋮ (PA.0-PA.3)	V_{IH1}	—	1.2	—	1.5	V	4
	V_{IL1}	—	0	—	0.3	V	
	V_{IH1S}	V_{DDI}=5 V	4	—	5	V	
	V_{IL1S}	V_{DDI}=5 V	0	—	1	V	
Input Voltage 2 (OSC0)	V_{IH2}	—	2.4	—	3.0	V	
	V_{IL2}	—	0	—	0.6	V	
Input Voltage 3 (RESET, TST1, TST2)	V_{IH3}	—	1.35	—	1.5	V	
	V_{IL3}	—	0	—	0.15	V	
Hysteresis Width 1 (P0.0-P0.3) (P1.0-P1.3) (P8.0-P8.3) ⋮ (PA.0-PA.3)	ΔVT1	—	0.05	0.1	0.3	V	
	ΔVT1S	V_{DDI}=5 V	0.25	1.0	1.5	V	
Hysteresis Width 2 (RESET, TST1, TST2)	ΔVT2	—	0.05	0.1	0.3	V	
Input Pin Capacitance (P0.0-P0.3) (P1.0-P1.3) (P8.0-P8.3) (P9.0-P9.3) ⋮ (PA.0-PA.3)	C_{IN}	—	—	—	5	pF	1

Measuring circuit 1

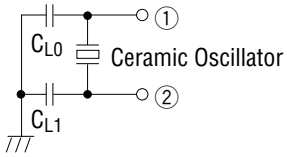


C_a, C_b, C_c, C_d, C_e, C_l, C_{12} :0.1 µF
C_{b12}, C_h :1 µF
C_G :15 pF
C_{L0} :30 pF
C_{L1} :30 pF
Ceramic Oscillator :CSB1000J (1 MHz)
(Murata-make)

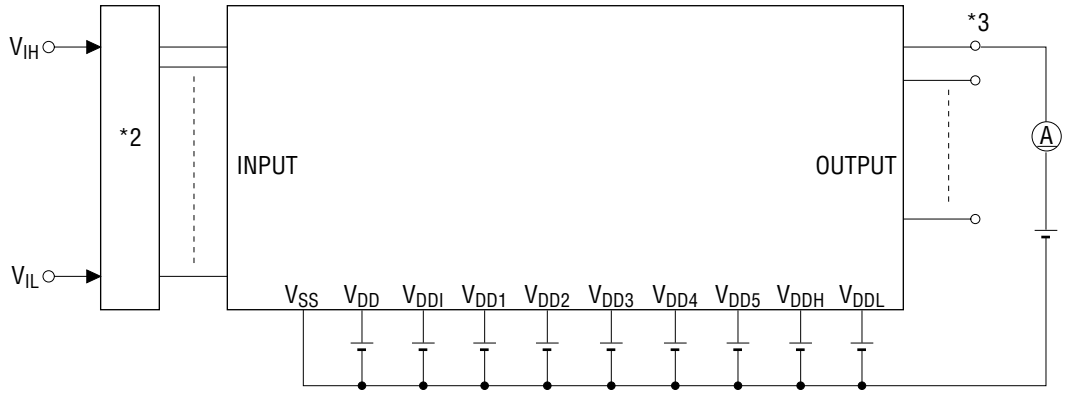
*1 RC Oscillator



Ceramic Oscillation

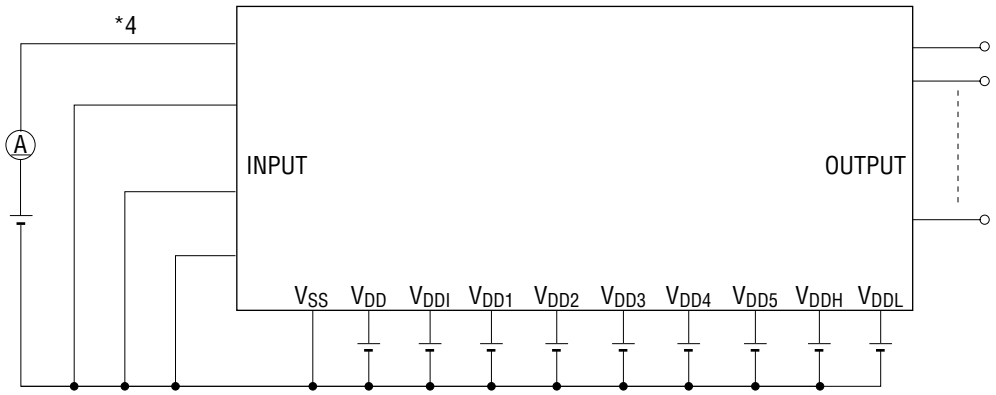


Measuring circuit 2

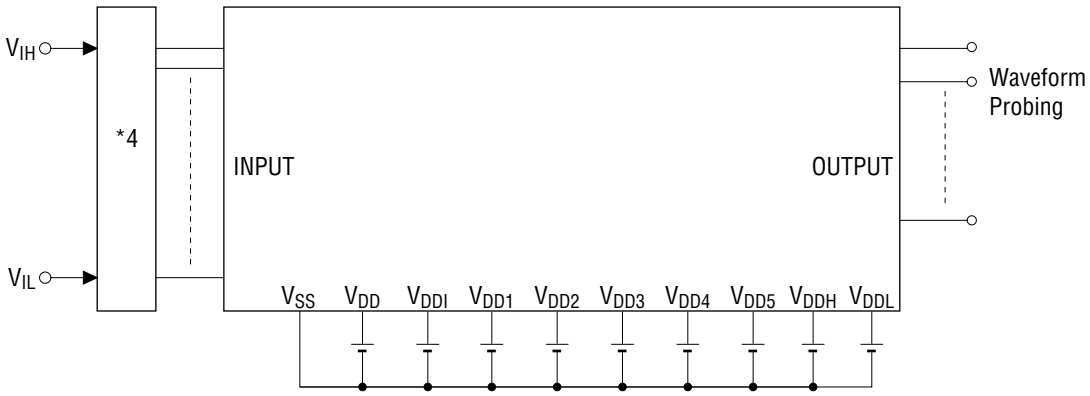


*2 Input logic to determine a specified state.
*3 To be repeated for the specified output pin.

Measuring circuit 3



Measuring circuit 4



*4 To be repeated for the specified input pin.

DC Characteristics (when power supply is not backed up)

(V_{DD}=V_{DDI}=V_{DDH}=3 V, V_{SS}=0 V, Ta=–20 to +70°C unless otherwise specified)

(1/3)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Current Consumpiton 1	I_{DD1}	CPU in HALT state (High-speed clock oscillation stops)	—	2.7	18	µA	1
Current Consumption 2	I_{DD2}	CPU in HALT state LCD in Power Down mode (High-speed clock oscillation stops)	—	2.0	15	µA	
Current Consumpiton 3	I_{DD3}	CPU in operating state (High-speed clock oscillation stops)	—	8.0	20	µA	
Current Consumpiton 4	I_{DD4}	CPU in operaton state at high-speed oscillation (RC oscillation, R_{OS}=51 kΩ)	—	380	500	µA	
Current Consumpiton 5	I_{DD5}	CPU in operation state at high-speed oscillation (Ceramic oscillation 2 MHz)	—	700	800	µA	

DC Characteristics (when power supply is not backed up)

(V_{DD}=V_{DDI}=V_{DDH}=3 V, V_{SS}=0 V, V_{DD1}=1.1 V, V_{DD2}=2.2 V, V_{DD3}=3.3 V, V_{DD4}=4.4 V, V_{DD5}=5.5 V, Ta=–20 to +70°C unless otherwise specified)

(2/3)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P4.0 to P4.3) (P5.0 to P5.3) (P6.0 to P6.3) ⋮ (P9.0 to P9.3) (PA.0 to PA.3)	I_{OH1}	V_{OH1}=V_{DDI}–0.5 V	–5.0	–3.0	–1.0	mA	
	I_{OL1}	V_{OL1}=0.5 V	1.0	3.0	5.0	mA	
	I_{OH1S}	V_{DDI}=5 V, V_{OH1S}=V_{DDI}–0.5 V	–8	–4	–2	mA	
	I_{OL1S}	V_{DDI}=5 V, V_{OL1S}=0.5 V	2	4	8	mA	
Output Current 2 (BD, BDB)	I_{OH2}	V_{OH2}=V_{DD}–0.7 V	–6	–4	–2	mA	
	I_{OL2}	V_{OL2}=0.7 V	2	4	6	mA	
Output Current 3 (SEG0 to SEG31) (COM1 to COM16)	I_{OH3}	V_{DD3}=V_{DD5}–0.2 V(V_{DD5} level)	—	—	–4	µA	2
	I_{OHM3}	V_{OHM3}=V_{DD4}+0.2 V(V_{DD4} level)	4	—	—	µA	
	I_{OHM3S}	V_{OHM3S}=V_{DD4}–0.2 V(V_{DD4} level)	—	—	–4	µA	
	I_{OMH3}	V_{OMH3}=V_{DD3}+0.2 V(V_{DD3} level)	4	—	—	µA	
	I_{OMH3S}	V_{OMH3S}=V_{DD3}–0.2 V(V_{DD3} level)	—	—	–4	µA	
	I_{OML3}	V_{OML3}=V_{DD2}+0.2 V(V_{DD2} level)	4	—	—	µA	
	I_{OML3S}	V_{OML3S}=V_{DD2}–0.2 V(V_{DD2} level)	—	—	–4	µA	
	I_{OLM3}	V_{OLM3}=V_{DD1}+0.2 V(V_{DD1} level)	4	—	—	µA	
	I_{OLM3S}	V_{OLM3S}=V_{DD1}–0.2 V(V_{DD1} level)	—	—	–4	µA	
	I_{OL3}	V_{OL3}=V_{SS}+0.2 V(V_{SS} level)	4	—	—	µA	
Output Current 4 (OSC1)	I_{OH4R}	V_{OH4R}=V_{DDH}–0.5 V(RC osc mode)	–2.5	–1.5	–0.75	mA	
	I_{OL4R}	V_{OL4R}=0.5 V(RC osc mode)	0.75	1.5	2.5	mA	
	I_{OH4C}	V_{OH4C}=V_{DDH}–0.5 V(Ceramic osc mode)	–240	–120	–60	µA	
	I_{OL4C}	V_{OL4C}=0.5 V(Ceramic osc mode)	60	120	240	µA	
Output Leakage (P4.0 to P4.3) (P5.0 to P5.3) (P6.0 to P6.3) ⋮ (PA.0 to PA.3)	I_{OOH}	V_{OH}=V_{DDI}	—	—	0.3	µA	
	I_{OOL}	V_{OL}=V_{SS}	–0.3	—	—	µA	

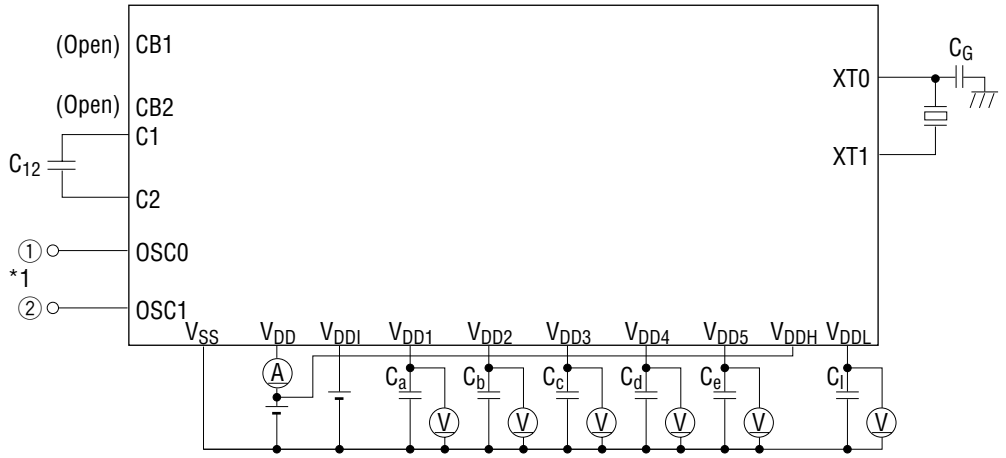
DC Characteristics (when power supply is not backed up)

(V_{DD}=V_{DDI}=V_{DDH}=3 V, V_{SS}=0 V, V_{DD1}=1.1 V, V_{DD2}=2.2 V, V_{DD3}=3.3 V, V_{DD4}=4.4 V, V_{DD5}=5.5 V, Ta=–20 to +70°C unless otherwise specified)

(3/3)

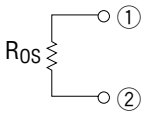
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) (P9.0 to P9.3) ⋮ (PA.0 to PA.3)	I_{IH1}	V_{IH1}=V_{DDI}(pulldown)	30	90	180	µA	3
	I_{IL1}	V_{IL1}=V_{SS}(pullup)	–180	–90	–30	µA	
	I_{IH1S}	V_{IH1}=V_{DDI}=5 V(pulldown)	70	250	600	µA	
	I_{IL1S}	V_{IL1}=0 V, V_{DDI}=5 V(pullup)	–600	–250	–70	µA	
	I_{IH1Z}	V_{IH1}=V_{DDI}(High impedance)	0	—	1	µA	
	I_{IL1Z}	V_{IL1}=V_{SS}(high impedance)	–1	—	0	µA	
Input Current 2 (OSC0)	I_{IL2}	V_{IL2}=V_{SS}(pullup)	–200	–110	–30	µA	
	I_{IH2Z}	V_{IH2}=V_{DDH}(RC oscillation)	0	—	1	µA	
	I_{IL2Z}	V_{IL2}=V_{SS}(RC oscillation)	–1	—	0	µA	
	I_{IH2C}	V_{IH2}=V_{DDH}(Ceramic oscillation)	0.75	1.5	3	µA	
	I_{IL2C}	V_{IL2}=V_{SS}(Ceramic oscillation)	–3	–1.5	–0.75	µA	
Input Current 3 (RESET)	I_{IH3}	V_{IH3}=V_{DD}	150	350	600	µA	
	I_{IL3}	V_{IL3}=V_{SS}	–1	—	0	µA	
Input Current 4 (TST1, TST2)	I_{IH4}	V_{IH4}=V_{DD}	0.5	1.0	1.5	mA	
	I_{IL4}	V_{IL4}=V_{SS}	–1	—	0	µA	
Input Voltage 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) (P9.0 to P9.3) ⋮ (PA.0 to PA.3)	V_{IH1}	—	2.4	—	3	V	4
	V_{IL1}	—	0	—	0.6	V	
	V_{IH1S}	V_{DDI}=5 V	4	—	5	V	
	V_{IL1S}	V_{DDI}=5 V	0	—	1	V	
Input Voltage 2 (OSC0)	V_{IH2}	—	2.4	—	3.0	V	
	V_{IL2}	—	0	—	0.6	V	
Input Voltage 3 (RESET, TST1, TST2)	V_{IH3}	—	2.4	—	3.0	V	
	V_{IL3}	—	0	—	0.6	V	
Hysteresis Width 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) ⋮ (PA.0 to PA.3)	ΔVT1	—	0.2	0.5	1	V	
	ΔVT1S	V_{DDI}=5 V	0.25	1.0	1.5	V	
Hysteresis Width 2 (RESET, TST1, TST2)	ΔVT2	—	0.2	0.5	1.0	V	
Input Pin Capacitance (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) (P9.0 to P9.3) ⋮ (PA.0 to PA.3)	C_{IN}	—	—	—	5	pF	1

Measuring circuit 1

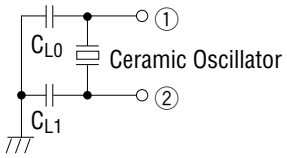


C_a, C_b, C_c, C_d, C_e, C_l, C_{12} :0.1 µF
C_G :15 pF
C_{L0} :30 pF
C_{L1} :30 pF
Ceramic Oscillator :CSA2.00MG (2 MHz)
(Murata-make)

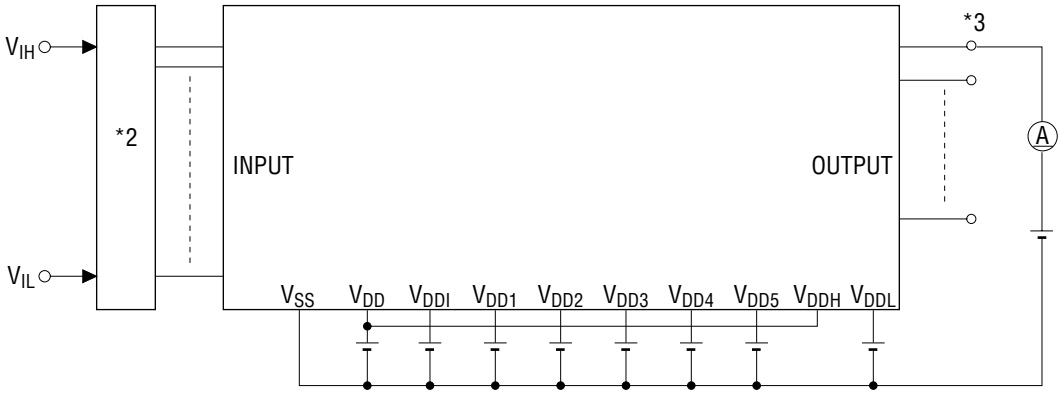
*1 RC Oscillation



Ceramic Oscillation

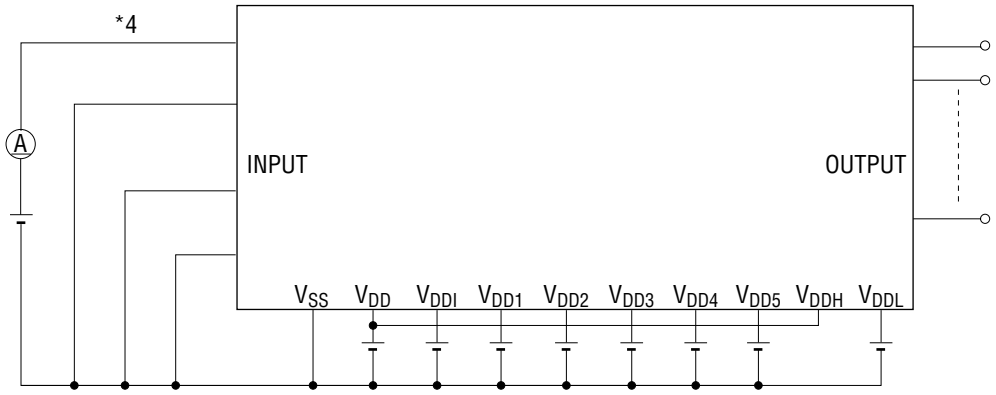


Measuring circuit 2

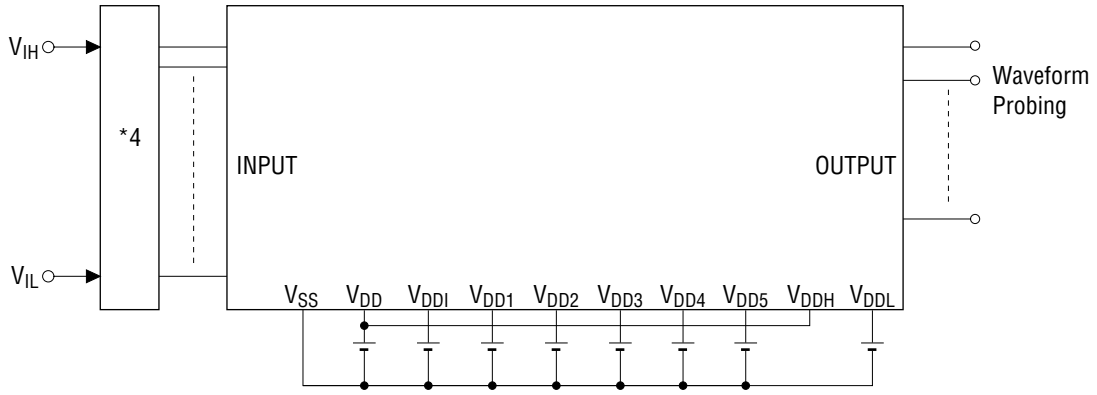


*2 Input logic to determine a specified state.
*3 To be repeated for the specified output pin.

Measuring circuit 3



Measuring circuit 4



*4 To be repeated for the specified input pin.

AC Characteristics (data transfer from/to external memory)

(V_{DD}=0.9 to 5.5 V, V_{SS}=0 V, V_{DDI}=5 V, Ta=–20 to +70°C)

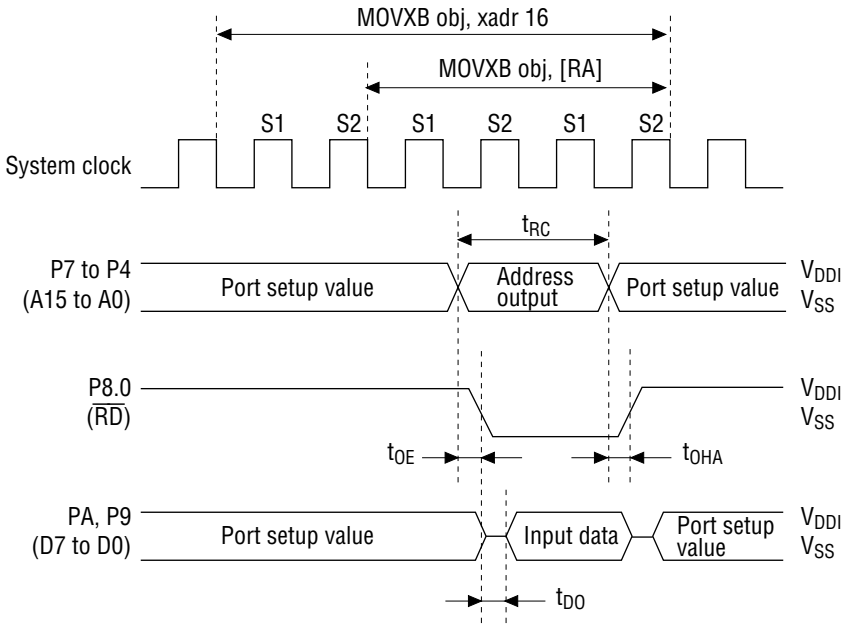
(1) Reading from external memory

(a) When the CPU operates at 32.768 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	—	61	—	µs
$\overline{RD}$ Output Delay Time	t_{OE}	—	—	—	5	µs
Output Enable Time	t_{OHA}	—	—	—	5	µs
External Memory Output Delay Time	t_{DO}	—	—	—	5	µs

(b) When the CPU operates at 2 MHz (V_{DD}=V_{DDH}=2.7 to 5.5 V).

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	1	—	—	µs
$\overline{RD}$ Output Delay Time	t_{OE}	—	—	—	100	µs
Output Enable Time	t_{OHA}	—	—	—	100	µs
External Memory Output Delay Time	t_{DO}	—	—	—	150	µs



("H" level=4 V, "L" level=1 V)

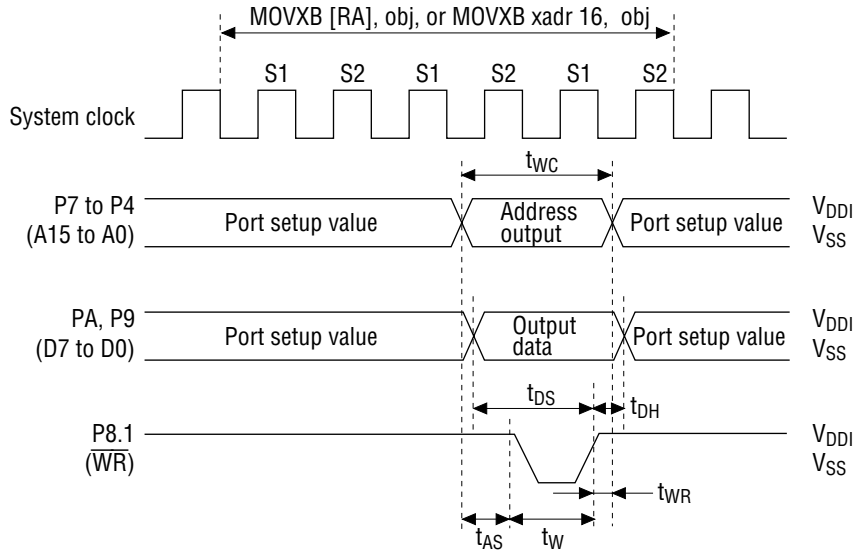
(2) Writing to external memory

(a) When the CPU operates at 32.768 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	—	61	—	µs
Address Setup Time	t_{AS}	—	—	30.5	—	µs
Write Time	t_{W}	—	—	15.3	—	µs
Write Recovery Time	t_{WR}	—	—	15.3	—	µs
Data Setup Time	t_{DS}	—	—	45.8	—	µs
Data Hold Time	t_{DH}	—	—	15.3	—	µs

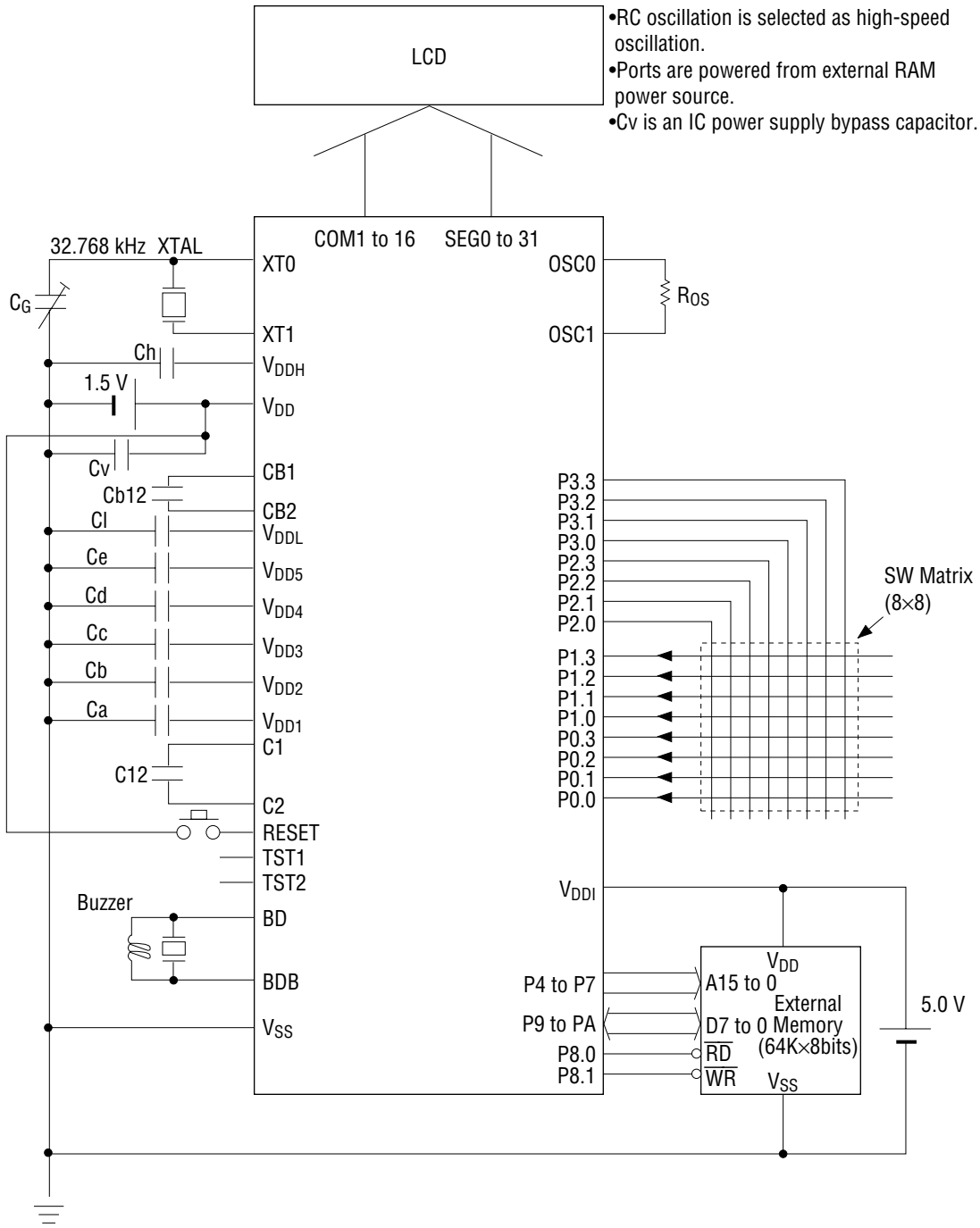
(b) When the CPU operates at 2 MHz (V_{DD}=V_{DDH}=2.7 to 5.5 V).

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	1	—	—	µs
Address Setup Time	t_{AS}	—	0.4	—	—	µs
Write Time	t_{W}	—	0.2	—	—	µs
Write Recovery Time	t_{WR}	—	0.2	—	—	µs
Data Setup Time	t_{DS}	—	0.7	—	—	µs
Data Hold Time	t_{DH}	—	0.2	—	—	µs

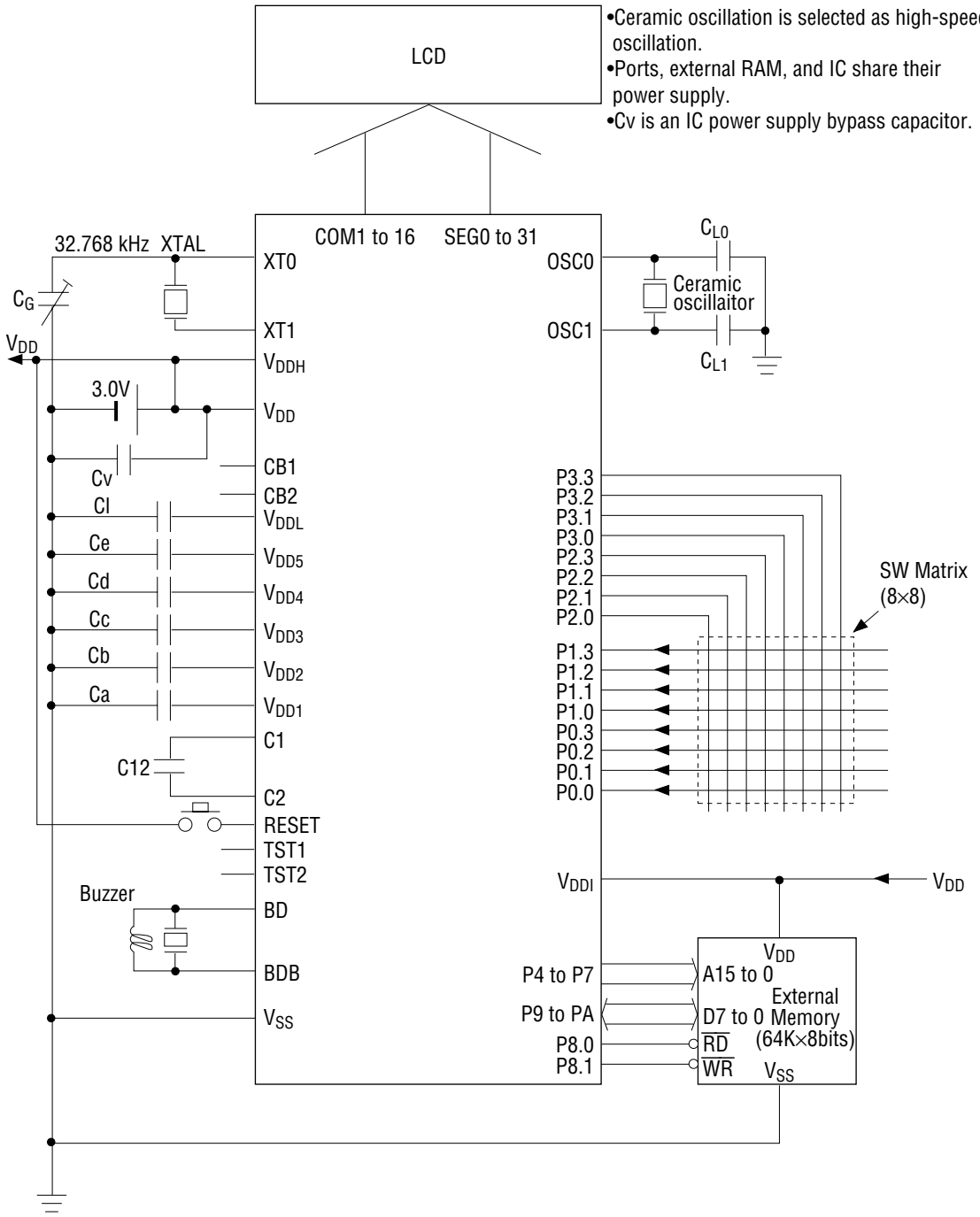


("H" level=4 V, "L" level=1 V)

APPLICATION CIRCUITS



Application Circuit Example with Power Supply Backup

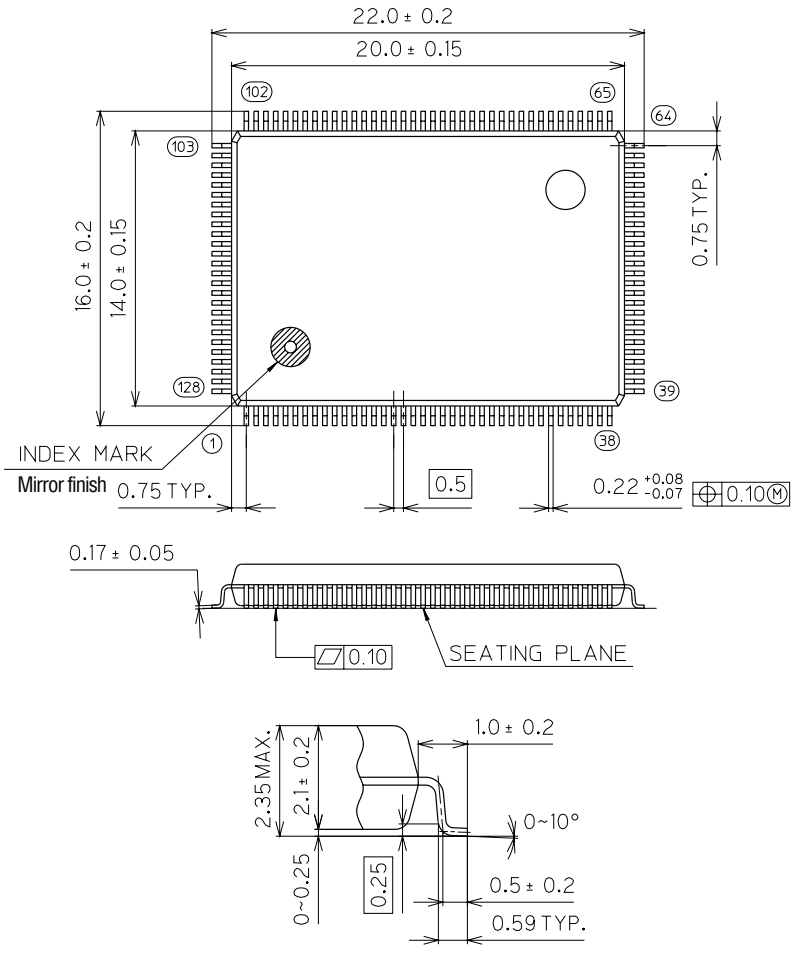


Application Circuit Example with No Power Supply Backup

PACKAGE DIMENSIONS

(Unit : mm)

QFP128-P-1420-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.19 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).