

10, 12 OR 14 BIT S/D OR R/D CONVERTER

This preliminary data sheet provides detailed functional capabilities for product currently in prototype production.

These specifications are being provided to aid electrical design, layout, and operation.

LOWER COST! PIN FOR PIN REPLACEMENT FOR SDC-630/632/634 SERIES. FOR ALL NEW DESIGNS!

DESCRIPTION

The SDC 630,632 and 634*A/ST series are low cost, low profile synchro to digital and resolver to digital tracking converters with standard pin configurations. They use a unique control transformer algorithm that provides inherently higher accuracy and jitter-free output. Utilizing a type II servo loop, these converters have no velocity lag up to the specified tracking rate and output data is always fresh and continuously available. Each unit is fully trimmed and requires no adjustments or calibrations in the field.

APPLICATIONS

These converters may be used wherever analog angle data from a synchro or resolver must be converted rapidly and accurately to digital form for transmission, storage or analysis. Because these units are extremely rugged and stable, and meet the requirements of MIL-STD-202E, they are suitable for the most severe industrial, commercial and military applications. Military ground support and avionics uses include ordnance control, radar tracking systems, navigations, and collision avoidance systems.

FEATURES

- INDUSTRY STANDARD LOW PROFILE MODULAR CONVERTERS
- ACCURACY

10 BIT:21 MINUTES 12 BIT:8.5 MINUTES 14 BIT:4 MIN 0.9 LSB OR 2.6 MIN (HIGH ACCURACY)

SIGNAL AND REF INPUT:

INTERNAL TRANSFORMER
ISOLATION (A VERSION) OR
LOW COST SOLID STATE
BUFFERS (ST VERSION)
ALL COMMON L-L LEVELS AND
FREQUENCIES

• OPTIONS (CONSULT FACTORY)

VELOCITY OUTPUT BIT -BUILT-IN-TEST 16 BIT RESOLUTION

* PATENTED

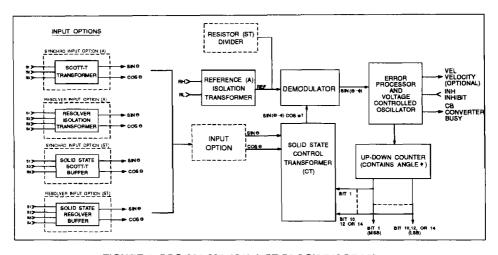


FIGURE 1. SDC-630/632/634* A/ST BLOCK DIAGRAM



up to 10% harmonic distortion in the reference	 		-				
PARAMETERS	VALUE						
	SDC-630	SDC-632	SDC-634				
RESOLUTION	10 bits	12 bits	14 bits				
ACCURACY							
Standard Units	±21 min	±8.5 min	±4 min ±0.9 LSB				
High Accuracy Option		_	±2.6 min				
	Signal Input						
SIGNAL AND REFERENCE INPUT	Signal Frequency Impedance (L-L						
	Range	Balanced,	Balanced, Resistive)				
		A*	ST				
Synchro Input	į į						
90V L-L, 400 Hz (Option H)	350-1000 Hz	148 KΩ min	123K				
	47-1000 Hz	148 KΩ min	123K				
90V L-L, 60 Hz (Option I)	350-1000 Hz	19 KΩ min	52K				
11.8V L-L, 400 Hz (Option L)	350-1000 Fiz	13 (22)(10)	JEN				
Resolver Input	050 4000 11-	148 1/0 = :-					
90V L-L, 400 Hz (Option H)	350-1000 Hz	148 KΩ min	-				
26V L-L, 400 Hz (Option M)	350-1000 Hz	42 KΩ min					
11.8V L-L, 400 Hz (Option L)	350-1000 Hz	19 KΩ min	70K				
Reference Input	Reference	Ref. Input Ir	mpedance				
	Voltage Range (Resistive)						
Options H,I	f :						
Options M,L	40-150V rms	300 KΩ min	270K				
	10-50V rms	80 KΩ min	60K				
*Transformer isolated. Other voltages and frequen	cies available on special order.						
DIGITAL/INPUT OUTPUT							
Logic Type		TTL/CMOS Compatable					
Inhibit Input (INH)	Logic "0" inhibits						
ninot input (itti)	Does not interrupt converter tracking						
		700 Pot Interrupt Controller Vaccus	' 8				
Outputs							
Туре		TTL/CMOS					
		11201100					
10,12, or 14 (16-Consult Factory)	Manual Constitution of the						
Parallel Data Bits		latural binary angle; positive logic					
Converter Busy (CB)	0.5 to 1.5msec	positive pulse. Data changes on	leading edge.				
Drive Capability	1 Std. TTL loads						
Built-In-Test (BIT) - Special Order Consult Factory	<u> </u>						
VELOCITY OUTPUT (ON SPECIAL ORDER ON	- v)						
Polarity							
	Postive output for incresing angle						
Std Voltage Range (full scale)	±4V Min	(Other ranges available consult	factory)				
For other Velocity Characteristics Consult Fac	tory						
POWER SUPPLIES							
Nominal Voltage	+15V Supply	-15V Supply	+5V Logic Supply				
Voltage Range	+11 to +16.5V	-11 to -16.5V	+4.5 to +5.5V				
Max. Voltage Without Damage	+18V	-18V	7V				
Current (ALL)	20mA	25mA	10mA				
TEMPERATURE RANGES		1	1011/7				
Operating	1						
-1 Option		5500 m 40500					
·	-55°C to +105°C						
-3 Option	0°C to +70°C						
Storage							
PHYSICAL CHARACTERISTICS							
Size (Encapsulated Module)		3.125 x 2.625 x 0.43 inch					
		(7.94 x 6.67 x 1.07 cm)					
Weight	4 oz (113g)						



	DYN	AMIC CHA	RACTER	STICS					
Bandwidth (nom F carrier)		60 Hz				400 Hz			
Carrier Frequency Range		47-1,000				360-1,000 (ST to 5k)			
Bandwidth (Closed Loop)		15				100			
Ka		1,100				48,000			
A1		-145				1			
A2		7,600				48,000			
A		33				220			
В		16.3				110			
RESOLUTION	10	12	14	16	10	12	14	16	впз
Tracking Rate (rps)									
typical	28.5	7.1	1.8	0.45	192	48	12	3	rps
minimum	24	6	1.5	0.37	160	40	10	2.5	rps
Acceleration (1 LSB lag)	370	93	23	5.8	17K	4,220	1,050	260	⁰ /s2
Settling time (1790 step, max)	500	600	900	2,200	90	100	140	320	msec

TECHNICAL INFORMATION

POWER SUPPLIES

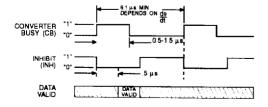
The main power supplies can vary over their specified ranges with no change in the converter specifications except for a proportional change in the maximum tracking rates.

When testing or evaluating the converters, it is advisable to limit the current to each of the three power supplies. Set each limit to 50% greater than the maximum current listed for that supply in the specifications table.

TIMING

The figure below shows the timing waveforms of the converter. Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 lsb, and generates a converter busy impulse (CB). The CB is a positive pulse 0.5 to 1.5u sec long. Data changes on the leading edge of the CB pulse, and data can be transferred 0.5µsec after the leading edge.

The simplest method of interfacing with a computer is to transfer data at a fixed time interval after the inhibit is applied. The converter will ignore an inhibit applied during the "busy" interval until that interval is over. Timing is as follows: (a) apply the inhibit, (b) wait 0.5µs, (c) transfer the data, and (d) release the inhibit. INH does not effect converter tracking.



SDC-630/632/634* A/ST TIMING DIAGRAM

SIGNAL INPUTS

To prevent damage to the inputs, the maximum steady state voltage should not exceed the specified input voltage by more than 30%.

ACCOMMODATING NON-STANDARD INPUT VOLTAGES (A ONLY)

The signal and reference input levels can be resistively scaled to accommodate non-standard voltages. A converter should be selected that is the next lower standard voltage and the voltage is then scaled up with resistors in series with the synchro and/or reference inputs.

For a synchro input (SDC), a resistor R SIG is added in series with S1, S2 and S3, which is determined as follows:

R_{SIG} = 1.11K (New L-L Voltage - Standard Unit Voltage)

That is 1.11K for each volt above that for which the standard unit is designed.

Example: An SDC-634A-L (11.8V) is to be used at 50V L-L

$$R_{SIG} - 1.11K (50-11.8) = 42.4K$$

The closest available high grade resistor with a low temperature coefficient of resistance should be used, and the three resistors should be matched to each other as closely as possible. In general, a 0.1% difference will introduce 1.7 arc minutes of additional error dur to the effect on SIN/COS ratio relationship.

The ABSOLUTE value of the resistor is not critical.

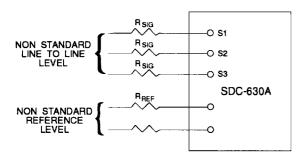
In the case of the RESOLVER version (RDC), the equation is:

R_{SIG} = 2.2K (New L-L level - Standard Unit L-L level)

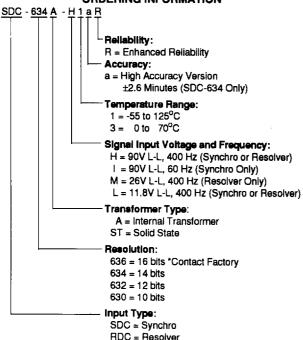
The calculated resistors are connected in series with S1 and S2 respectively. Note only two resistors required. The required resistor matching and its effect on accuracy, is the same as for a synchro input (See Figure). The Reference Voltage treatment is similar, but the value selected is not critical.

R_{Ref}=2.8K (New ref - standard ref)

Here, even a 10% tolerance is adequate.



ORDERING INFORMATION



^{*} For versions with Velocity or Built-in-Test Please Consult Factory. PRE-02-10/93

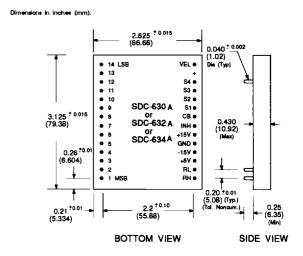


FIGURE 4. SDC-630/632/634A MECHANICAL OUTLINE