8M X 33 Bits DRAM SIMM Memory Module

FEATURES

- Performance range:

	t_{RAC}	t_{CAC}	t_{RC}
STI338000-60	60ns	15ns	110ns
STI338000-70	70ns	20ns	130ns
STI338000-80	80ns	20ns	150ns

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V ± 10% power supply
- 2048 cycles/32ms refresh
- JEDEC standard pinout

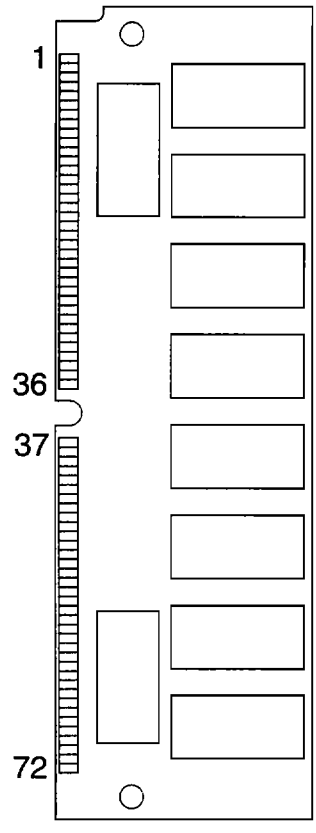
GENERAL DESCRIPTION

The Simple Technology STI338000 is a 8M x 33 bits Dynamic RAM high density memory module. The Simple Technology STI338000 consist of sixteen CMOS 4M x 4 DRAMs in 24-pin SOJ package and two CMOS 4M x 1 bit DRAMs in a 20-pin SOJ package mounted on a 72-pin glass epoxy substrate. A 0.1µF decoupling capacitor is mounted for each DRAM.

The STI338000 is a Single In-line Memory Module with tin or gold edge connections, 5V power supply, and 2K refresh. The STI338000 is intended for mounting into 72-pin edge connector sockets.

PIN CONFIGURATION

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	DQ_{22}	49	DQ_{8}
2	DQ_{0}	26	DQ_{7}	50	DQ_{24}
3	DQ_{16}	27	DQ_{23}	51	DQ_{9}
4	DQ_{1}	28	A_{7}	52	DQ_{25}
5	DQ_{17}	29	NC	53	DQ_{10}
6	DQ_{2}	30	V_{CC}	54	DQ_{26}
7	DQ_{18}	31	A_{8}	55	DQ_{11}
8	DQ_{3}	32	A_{9}	56	DQ_{27}
9	DQ_{19}	33	$\overline{RAS}_{3}$	57	DQ_{12}
10	V_{CC}	34	$\overline{RAS}_{2}$	58	DQ_{28}
11	NC	35	NC	59	V_{CC}
12	A_{0}	36	NC	60	DQ_{29}
13	A_{1}	37	NC	61	DQ_{13}
14	A_{2}	38	DQ_{32}	62	DQ_{30}
15	A_{3}	39	V_{SS}	63	DQ_{14}
16	A_{4}	40	$\overline{CAS}_{0}$	64	DQ_{31}
17	A_{5}	41	$\overline{CAS}_{2}$	65	DQ_{15}
18	A_{6}	42	$\overline{CAS}_{3}$	66	NC
19	A_{10}	43	$\overline{CAS}_{1}$	67	PD_{1}
20	DQ_{4}	44	$\overline{RAS}_{0}$	68	PD_{2}
21	DQ_{20}	45	$\overline{RAS}_{1}$	69	PD_{3}
22	DQ_{5}	46	NC	70	PD_{4}
23	DQ_{21}	47	$\overline{W}$	71	NC
24	DQ_{6}	48	NC	72	V_{SS}



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Pin Names

Pin Name	Pin Function
A_{0}-A_{10}	Address Inputs
DQ_{0}-DQ_{32}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_{0}$-$\overline{RAS}_{3}$	Row Adress Strobe
$\overline{CAS}_{0}$-$\overline{CAS}_{3}$	Column Address Strobe
PD_{1}-PD_{4}	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

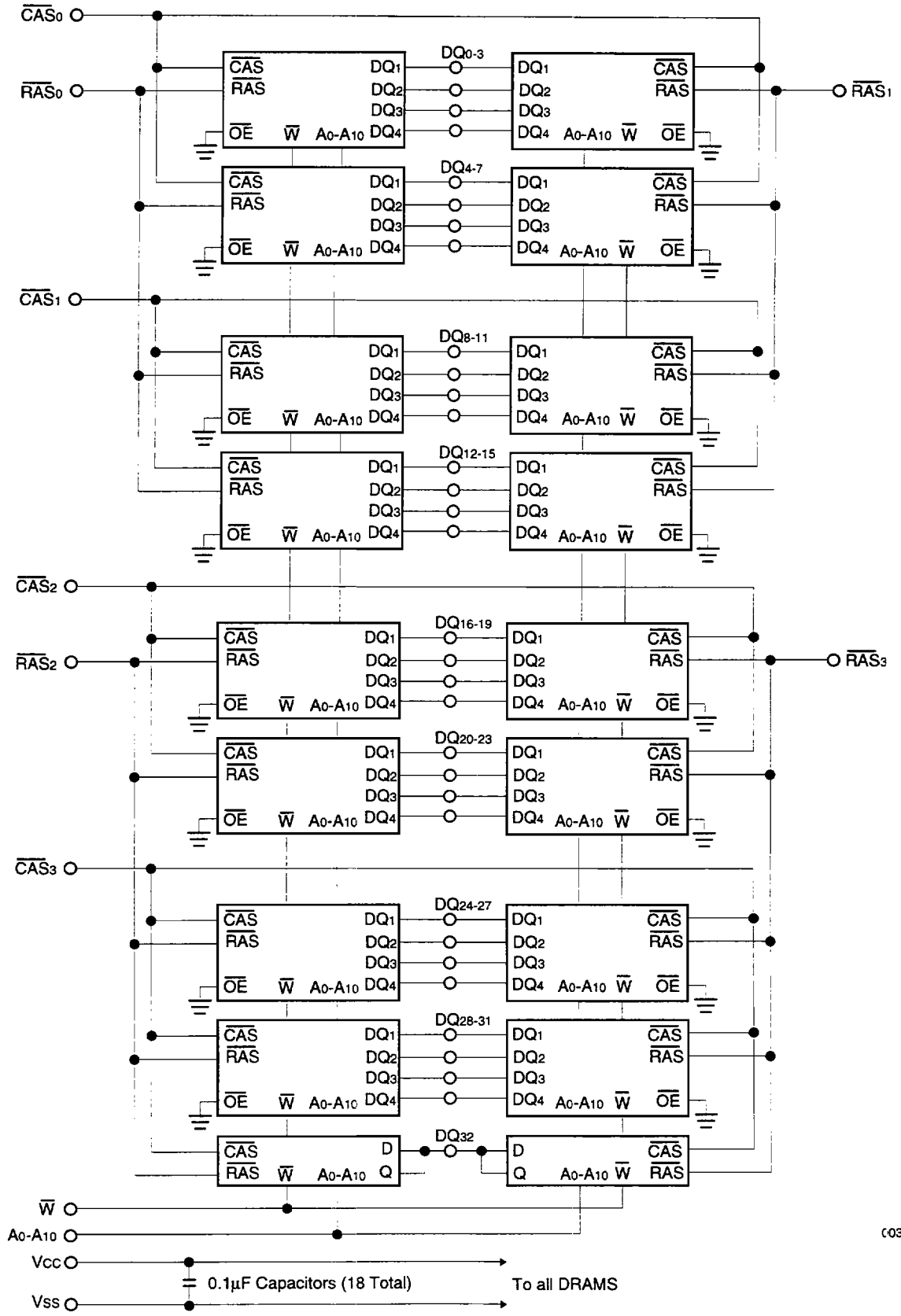
Presence Detect Pins*

(Optional)

Pin	60ns	70ns	80ns
PD_{1}	NC	NC	NC
PD_{2}	V_{SS}	V_{SS}	V_{SS}
PD_{3}	NC	V_{SS}	NC
PD_{4}	NC	NC	V_{SS}

* Pin Connection Changing Available

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	17.2	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the oprerational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1*	V
Input Low Voltage	V_{IL}	-1.0**	—	0.8	V

* V_{CC}+2.0V/20ns, Pulse width is measured at V_{CC}

** -2.0V/20ns, Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	STI338000-60	I_{CC1}	—	893	mA
	STI338000-70		—	803	mA
	STI338000-80		—	713	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}	—	36	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	STI338000-60	I_{CC3}	—	893	mA
	STI338000-70		—	803	mA
	STI338000-80		—	713	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=min.)	STI338000-60	I_{CC4}	—	713	mA
	STI338000-70		—	623	mA
	STI338000-80		—	533	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		I_{CC5}	—	18	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	STI338000-60	I_{CC6}	—	893	mA
	STI338000-70		—	803	mA
	STI338000-80		—	713	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0V)		I_{IL}	-90	90	µA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	-10	10	µA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

* I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycling rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle.

CAPACITANCE (T_A=25 °C, V_{CC}=5.0V, f=1MHz)

Item	Symbol	Min	Max	Units
Input Capacitance (A_0-A_{10})	C_{IN1}	—	90	pF
Input Capacitance ($\overline{W}$)	C_{IN2}	—	126	pF
Input Capacitance ($\overline{RAS}_0$, $\overline{RAS}_1$)	C_{IN3}	—	28	pF
Input Capacitance ($\overline{RAS}_2$, $\overline{RAS}_3$)	C_{IN4}	—	35	pF
Input Capacitance ($\overline{CAS}_0$-$\overline{CAS}_2$)	C_{IN5}	—	28	pF
Input Capacitance ($\overline{CAS}_3$)	C_{IN6}	—	42	pF
Input/Output Capacitance (DQ_0-DQ_{31})	C_{DQ1}	—	14	pF
Input/Output Capacitance (DQ_{32})	C_{DQ2}	—	28	pF

AC CHARACTERISTICS (0 °C≤T_A≤70 °C, V_{CC}=5.0V±10%, See notes 1, 2)

Parameter	Symbol	STI338000-60		STI338000-70		STI338000-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3, 4
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3, 4, 5
Access time from column address	t_{AA}		30		35		40	ns	3, 10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	8
Write command set-up time	t_{WCS}	0		0		0		ns	7
Write command hold time	t_{WCH}	10		15		15		ns	
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	

continued on the next page

AC CHARACTERISTICS (continued)

Parameter	Symbol	STI338000-60		STI338000-70		STI338000-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in set-up time	t_{DS}	0		0		0		ns	9
Data-in hold time	t_{DH}	10		15		15		ns	9
Refresh period	t_{REF}		32		32		32	ms	
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
$\overline{CAS}$ precharge time (fast page)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ pulse width (fast page)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	20		30		30		ns	

Notes:

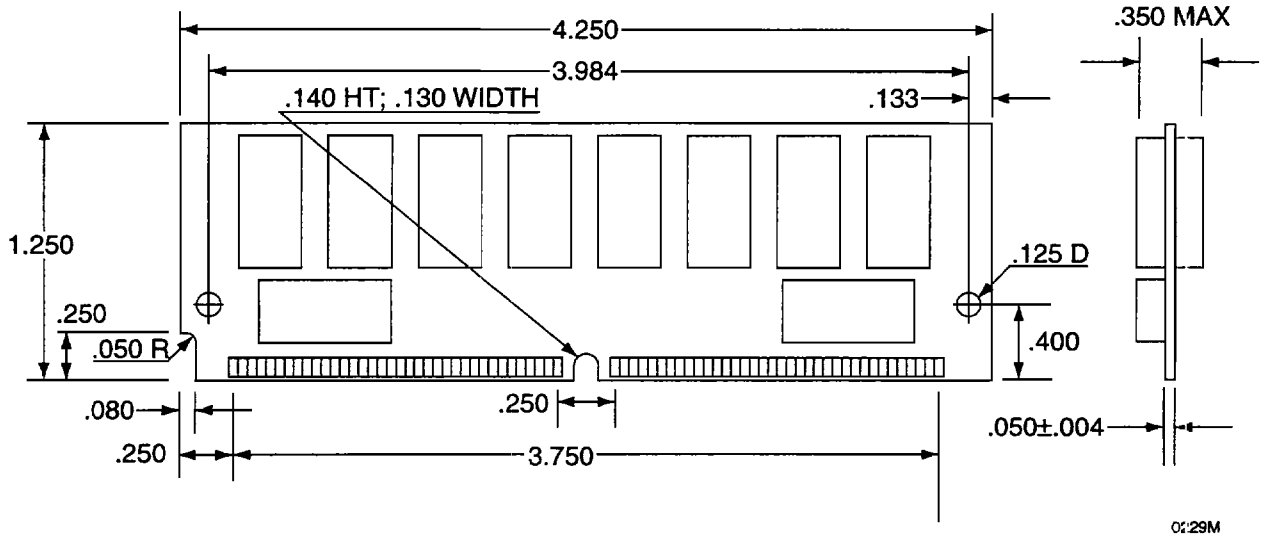
1. An initial pause of 200 ms is required after power-up followed by any 8 $\overline{RAS}$-Only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measure with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is a non-restrictive operating parameter. It is included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit then access time is controlled by t_{AA}.

TIMING DIAGRAMS

Please refer to attached Timing Chart I.

PACKAGE DIMENSIONS

Units: Inches



TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED