HardStore 8K x 8 nvSRAM Die

Features

- High-performance CMOS non-volatile static RAM 8192x 8 bits
- 25, 35 and 45 ns Access Times
- 12, 20 and 25 ns Output Enable Access Times
- Hardware STORE Initiation (STORE Cycle Time < 10 ms)
- Automatic STORE Timing
- 10^6 STORE cycles to EEPROM
- 100 years data retention in EEPROM
- Automatic RECALL on Power Up
- Hardware RECALL Initiation (RECALL Cycle Time < 20 μs)
- Unlimited RECALL cycles from EEPROM
- Unlimited SRAM Read and Write
- Single 5 V ± 10 % Operation
- Operating temperature ranges:
      0 to 70 °C
      -40 to 85 °C
- QS 90000 Quality Standard
- ESD protection > 2000 V (MIL STD 883C M3015.7-HBM)

Description

The U630H64 has two separate modes of operation: SRAM mode and non-volatile mode, determined by the state of the $\overline{NE}$ pad.

In SRAM mode, the memory operates as an ordinary static RAM. In non-volatile operation, data is transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM. In this mode SRAM functions are disabled.

The U630H64 is a fast static RAM (25, 35, 45 ns), with a non-volatile electrically erasable PROM (EEPROM) element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent non-volatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the STORE operation), or from the EEPROM to the SRAM (the RECALL operation) are initiated through the state of the $\overline{NE}$ pad.

The U630H64 combines the high performance and ease of use of a fast SRAM with non-volatile data integrity.

Once a STORE cycle is initiated, further input or output are disabled until the cycle is completed.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the non-volatile information is transferred into the SRAM cells.

The RECALL operation in no way alters the data in the EEPROM cells. The non-volatile data can be recalled an unlimited number of times.

The chips are tested with a restricted wafer probe program at room temperature only. Untested parameters are marked with a number sign (#).
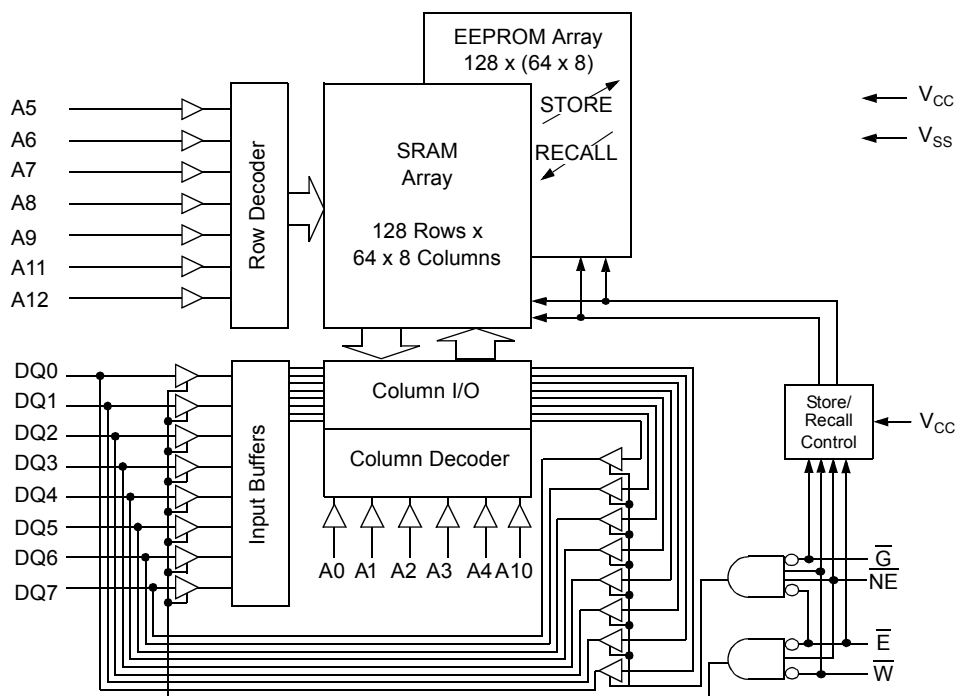
Pad Configuration
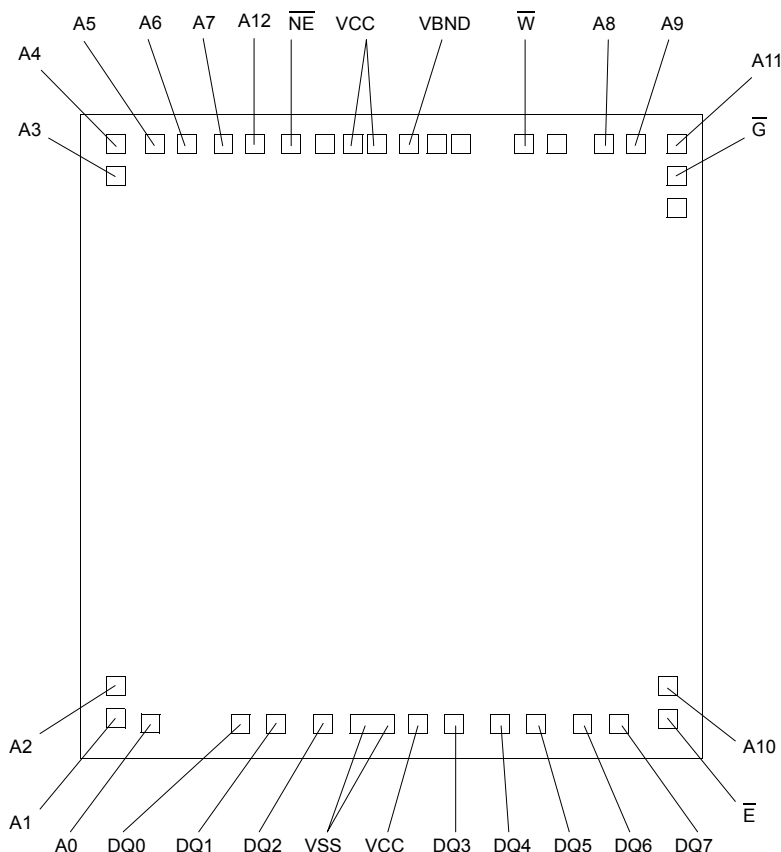
Pad Description

Signal Name	Signal Description
A0 - A12	Address Inputs
DQ0 - DQ7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{NE}$	Nonvolatile Enable
VCC	Power Supply Voltage
VSS	Ground
VBND	HardStore type enable

U630H64XS

Block Diagram

Truth Table for SRAM Operations

Operating Mode	$\overline{E}$	$\overline{NE}$	$\overline{W}$	$\overline{G}$	DQ0 - DQ7
Standby/not selected	H	*	*	*	High-Z
Internal Read	L	H	H	H	High-Z
Read	L	H	H	L	Data Outputs Low-Z
Write	L	H	L	*	Data Inputs High-Z

* H or L

Characteristics

All voltages are referenced to V_{SS} = 0 V (ground).

All characteristics are valid in the power supply voltage range and in the operating temperature range specified.

Dynamic measurements are based on a rise and fall time of $\leq$ 5 ns, measured between 10 % and 90 % of V_I, as well as input levels of V_{IL} = 0 V and V_{IH} = 3 V. The timing reference level of all input and output signals is 1.5 V, with the exception of the t_{dis}-times and t_{en}-times, in which cases transition is measured $\pm$ 200 mV from steady-state voltage.

Absolute Maximum Ratings[a]		Symbol	Min.	Max.	Unit
Power Supply Voltage		V_{CC}	-0.5	7	V
Input Voltage		V_I	-0.3	V_{CC}+0.5	V
Output Voltage		V_O	-0.3	V_{CC}+0.5	V
Power Dissipation		P_D		1	W
Operating Temperature	C-Type		0	70	°C
	K-Type	T_a	-40	85	°C
	A-Type		-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

a: Stresses greater than those listed under „Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	V_{CC}		4.5	5.5	V
Input Low Voltage	V_{IL}	-2 V at Pulse Width 10 ns permitted	-0.3	0.8	V
Input High Voltage	V_{IH}		2.2	V_{CC}+0.3	V

DC Characteristics	Symbol	Conditions		C-Type		K-Type		A-Type		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
Operating Supply Current[b]	I_{CC1}	V_{CC} = 5.5 V V_{IL} = 0.8 V V_{IH} = 2.2 V t_c = 25 ns t_c = 35 ns t_c = 45 ns		 90# 80# 75#		 95# 85# 80#		 - 85# -	mA mA mA
Average Supply Current during STORE[c]	I_{CC2}	V_{CC} = 5.5 V $\overline{E}$ ≥ V_{CC}-0.2 V $\overline{W}$ ≥ V_{CC}-0.2 V V_{IL} ≤ 0.2 V V_{IH} ≥ V_{CC}-0.2 V		6#		7#		7#	mA
Standby Supply Current[d] (Cycling TTL Input Levels)	$I_{CC(SB)1}$	V_{CC} = 5.5 V $\overline{E}$ ≥ V_{IH} t_c = 25 ns t_c = 35 ns t_c = 45 ns		 30# 23# 20#		 34# 27# 23#		 - 27# -	mA mA mA
Average Supply Current at t_{cR} = 200 ns[b] (Cycling CMOS Input Levels)	I_{CC3}	V_{CC} = 5.5 V $\overline{W}$ ≥ V_{CC}-0.2 V V_{IL} ≤ 0.2 V V_{IH} ≥ V_{CC}-0.2 V		15#		15#		15#	mA
Standby Supply Current[d] (Stable CMOS Input Levels)	$I_{CC(SB)}$	V_{CC} = 5.5 V $\overline{E}$ ≥ V_{CC}-0.2 V V_{IL} ≤ 0.2 V V_{IH} ≥ V_{CC}-0.2 V		1#		1#		2#	mA

b: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded. The current I_{CC1} is measured for WRITE/READ - ratio of 1/2.

c: I_{CC2} is the average current required for the duration of the STORE cycle (STORE Cycle Time).

d: Bringing $\overline{E}$ ≥ V_{IH} will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table. The current $I_{CC(SB)1}$ is measured for WRITE/READ - ratio of 1/2.

DC Characteristics	Symbol	Conditions		Min.	Max.	Unit
Output High Voltage Output Low Voltage	V_{OH} V_{OL}	V_{CC} I_{OH} I_{OL}	= 4.5 V =-4 mA = 8 mA	2.4#	 0.4#	V V
Output High Current Output Low Current	I_{OH} I_{OL}	V_{CC} V_{OH} V_{OL}	= 4.5 V = 2.4 V = 0.4 V	 8#	-4#	mA mA
Input Leakage Current High Low	 I_{IH} I_{IL}	V_{CC} V_{IH} V_{IL}	= 5.5 V = 5.5 V = 0 V	 -1	 1	 µA µA
Output Leakage Current High at Three-State- Output Low at Three-State- Output	 I_{OHZ} I_{OLZ}	V_{CC} V_{OH} V_{OL}	= 5.5 V = 5.5 V = 0 V	 -1	 1	 µA µA

SRAM Memory Operations

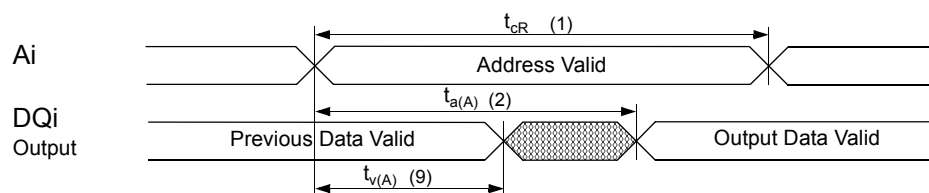| No.	Switching Characteristics Read Cycle	Symbol		25		35		45		Unit
		Alt.	IEC	Min.	Max.	Min.	Max.	Min.	Max.	
1	Read Cycle Time[f]	t_{AVAV}	t_{cR}	25#		35#		45#		ns
2	Address Access Time to Data Valid[g]	t_{AVQV}	$t_{a(A)}$		25#		35		45#	ns
3	Chip Enable Access Time to Data Valid	t_{ELQV}	$t_{a(E)}$		25#		35		45#	ns
4	Output Enable Access Time to Data Valid	t_{GLQV}	$t_{a(G)}$		12#		20#		25#	ns
5	$\overline{E}$ HIGH to Output in High-Z[h]	t_{EHQZ}	$t_{dis(E)}$		13#		17#		20#	ns
6	$\overline{G}$ HIGH to Output in High-Z[h]	t_{GHQZ}	$t_{dis(G)}$		13#		17#		20#	ns
7	$\overline{E}$ LOW to Output in Low-Z	t_{ELQX}	$t_{en(E)}$	5#		5#		5#		ns
8	$\overline{G}$ LOW to Output in Low-Z	t_{GLQX}	$t_{en(G)}$	0#		0#		0#		ns
9	Output Hold Time after Addr. Change[g]	t_{AXQX}	$t_{v(A)}$	3#		3#		3#		ns
10	Chip Enable to Power Active[e]	t_{ELICCH}	t_{PU}	0#		0#		0#		ns
11	Chip Disable to Power Standby[d, e]	t_{EHICCL}	t_{PD}		25#		35#		45#	ns

e: Parameter guaranteed but not tested.
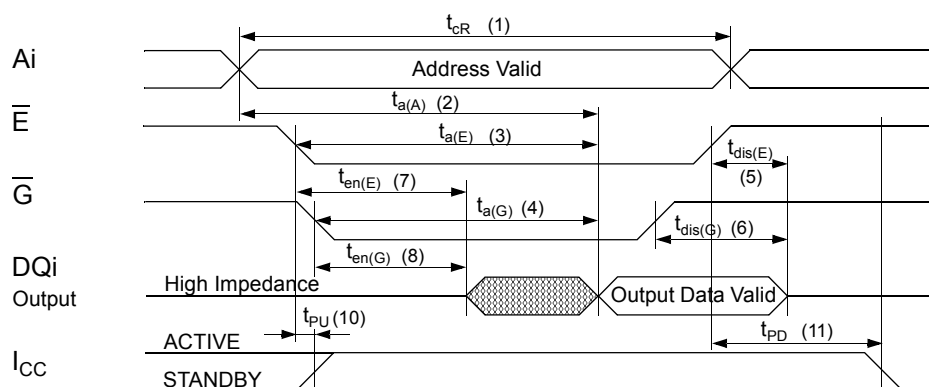f: Device is continuously selected with $\overline{E}$ and $\overline{G}$ both LOW.
g: Address valid prior to or coincident with $\overline{E}$ transition LOW.
h: Measured $\pm$ 200 mV from steady state output voltage.

Read Cycle 1: Ai-controlled (during Read cycle: $\overline{E}$ = $\overline{G}$ = V_{IL}, $\overline{W}$ = $\overline{NE}$ = V_{IH})[f]


**Read Cycle 2: $\overline{G}$-, $\overline{E}$-controlled (during Read cycle: $\overline{W}$ = $\overline{NE}$ = V_{IH})[g]**

No.	Switching Characteristics Write Cycle	Symbol			25		35		45		Unit
		Alt. #1	Alt. #2	IEC	Min.	Max.	Min.	Max.	Min.	Max.	
12	Write Cycle Time	t_{AVAV}	t_{AVAV}	t_{cW}	25#		35#		45#		ns
13	Write Pulse Width	t_{WLWH}		$t_{w(W)}$	20#		30#		35#		ns
14	Write Pulse Width Setup Time		t_{WLEH}	$t_{su(W)}$	20#		30#		35#		ns
15	Address Setup Time	t_{AVWL}	t_{AVEL}	$t_{su(A)}$	0#		0#		0#		ns
16	Address Valid to End of Write	t_{AVWH}	t_{AVEH}	$t_{su(A-WH)}$	20#		30#		35#		ns
17	Chip Enable Setup Time	t_{ELWH}		$t_{su(E)}$	20#		30#		35#		ns
18	Chip Enable to End of Write		t_{ELEH}	$t_{w(E)}$	20#		30		35#		ns
19	Data Setup Time to End of Write	t_{DVWH}	t_{DVEH}	$t_{su(D)}$	12#		18		20#		ns
20	Data Hold Time after End of Write	t_{WHDX}	t_{EHDX}	$t_{h(D)}$	0#		0#		0#		ns
21	Address Hold after End of Write	t_{WHAX}	t_{EHAX}	$t_{h(A)}$	0#		0#		0#		ns
22	$\overline{W}$ LOW to Output in High-Z[h, i]	t_{WLQZ}		$t_{dis(W)}$		10#		13#		15#	ns
23	$\overline{W}$ HIGH to Output in Low-Z	t_{WHQX}		$t_{en(W)}$	5#		5#		5#		ns

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Write Cycle #1: $\overline{W}$-controlled[j]
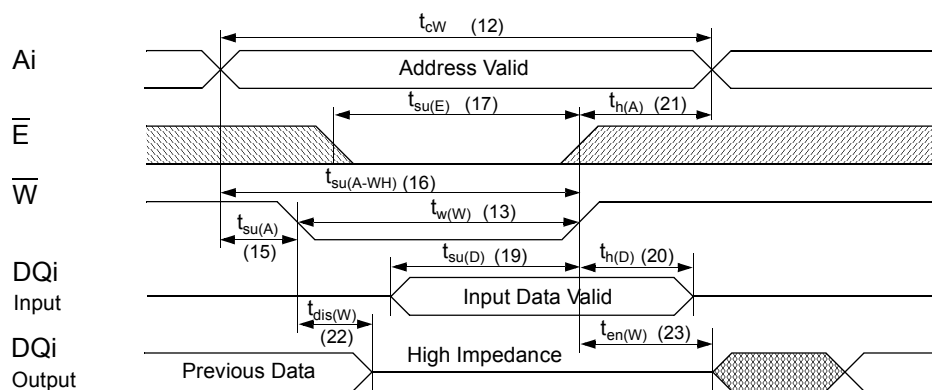
Write Cycle #2: $\overline{E}$-controlled[j]
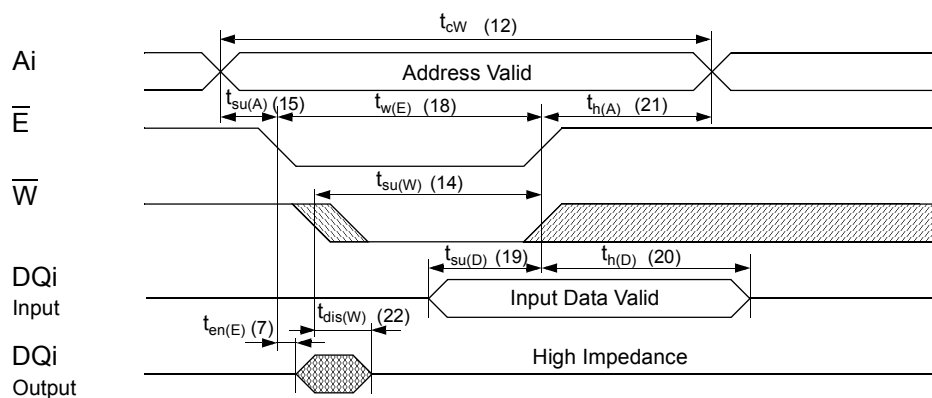
| undefined | L- to H-level | H- to L-level |

i: If $\overline{W}$ is LOW and when $\overline{E}$ goes LOW, the outputs remain in the high impedance state.
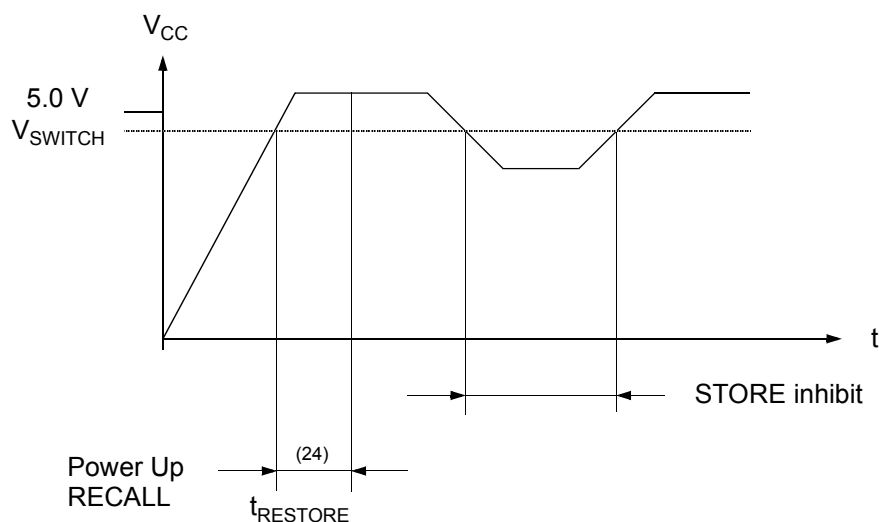
j: $\overline{E}$ or $\overline{W}$ and $\overline{NE}$ must be $\geq V_{IH}$ during address transitions.

Nonvolatile Memory Operations

No.	STORE Cycle Inhibit and Automatic Power Up RECALL	Symbol		Min.	Max.	Unit
		Alt.	IEC			
24	Power Up RECALL Duration[k, e]	$t_{RESTORE}$			650	µs
	Low Voltage Trigger Level	V_{SWITCH}		4.0	4.5	V

k: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.

STORE Cycle Inhibit and Automatic Power Up RECALL

Mode Selection

$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{NE}$	Mode	Power	Notes
L	H	L	L	Nonvolatile RECALL	Active	l
L	L	H	L	Nonvolatile STORE	I_{CC2}	
L
L	L
H	L
H	L
*	No operation	Active	

* H or L

l: An automatic RECALL also takes place at power up, starting when V_{CC} exceeds V_{SWITCH} and takes $t_{RESTORE}$. V_{CC} must not drop below V_{SWITCH} once it has been exceeded for the RECALL to function properly.

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STORE Cycles

No.	STORE Cycle $\overline{W}$-controlled	Symbol		Min.	Max.	Unit
		Alt.	IEC			
25	STORE Cycle Time[m]	t_{WLQX}	$t_{d(W)S}$		10#	ms
26	STORE Initiation Cycle Time[n]	t_{WLNH}	$t_{w(W)S}$	25#		ns
27	Output Disable Setup to $\overline{NE}$ Fall	t_{GHNL}	$t_{su(G)S}$	5#		ns
28	$\overline{NE}$ Setup	t_{NLWL}	$t_{su(N)S}$	5#		ns
29	Chip Enable Setup	t_{ELWL}	$t_{su(E)S}$	5#		ns

STORE Cycle: $\overline{W}$-controlled[o]
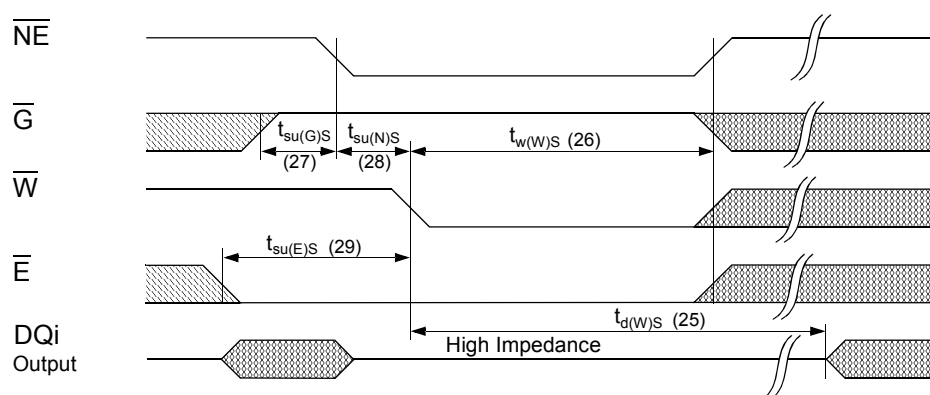
No.	STORE Cycle $\overline{E}$-controlled	Symbol		Min.	Max.	Unit
		Alt.	IEC			
30	STORE Cycle Time	t_{ELQXS}	$t_{d(E)S}$		10	ms
31	STORE Initiation Cycle Time	t_{ELNHS}	$t_{w(E)S}$	25#		ns
32	Output Disable Setup to $\overline{E}$ Fall	t_{GHEL}	$t_{su(G)S}$	5#		ns
33	$\overline{NE}$ Setup	t_{NLEL}	$t_{su(N)S}$	5#		ns
34	Write Enable Setup	t_{WLEL}	$t_{su(W)S}$	5#		ns

STORE Cycle: $\overline{E}$-controlled[o]

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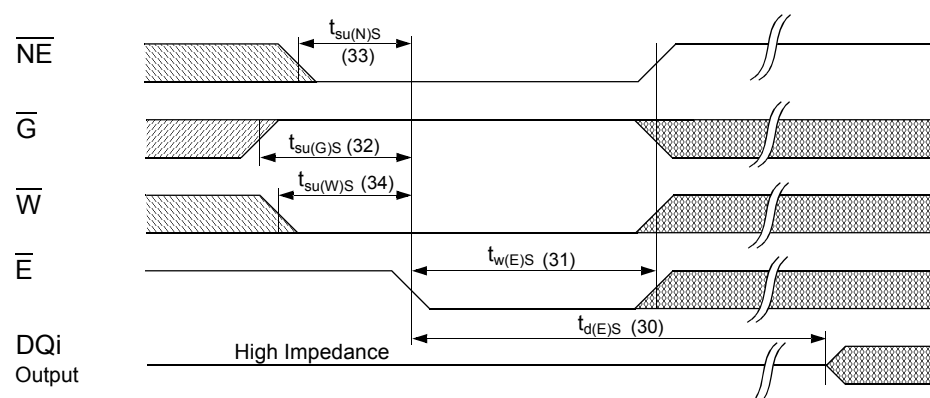
RECALL Cycles

No.	RECALL Cycle $\overline{NE}$-controlled	Symbol		Min.	Max.	Unit
		Alt.	IEC			
35	RECALL Cycle Time[p]	t_{NLQX}	$t_{d(N)R}$		20#	μs
36	RECALL Initiation Cycle Time[q]	t_{NLNH}	$t_{w(N)R}$	25#		ns
37	Output Enable Setup	t_{GLNL}	$t_{su(G)R}$	5#		ns
38	Write Enable Setup	t_{WHNL}	$t_{su(W)R}$	5#		ns
39	Chip Enable Setup	t_{ELNL}	$t_{su(E)R}$	5#		ns
40	$\overline{NE}$ Fall to Output Inactive	t_{NLQZ}	$t_{dis(N)R}$		25#	ns

RECALL Cycle: $\overline{NE}$-controlled[o]
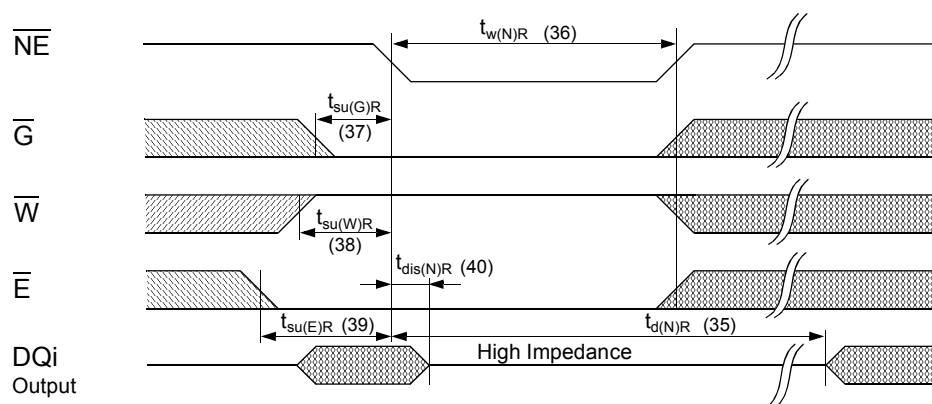
No.	RECALL Cycle $\overline{E}$-controlled	Symbol		Min.	Max.	Unit
		Alt.	IEC			
41	RECALL Cycle Time	t_{ELQXR}	$t_{d(E)R}$		20	μs
42	RECALL Initiation Cycle Time	t_{ELNHR}	$t_{w(E)R}$	25#		ns
43	$\overline{NE}$ Setup	t_{NLEL}	$t_{su(N)R}$	5#		ns
44	Output Enable Setup	t_{GLEL}	$t_{su(G)R}$	5#		ns
45	Write Enable Setup	t_{WHEL}	$t_{su(W)R}$	5#		ns

RECALL Cycle: $\overline{E}$-controlled[o]

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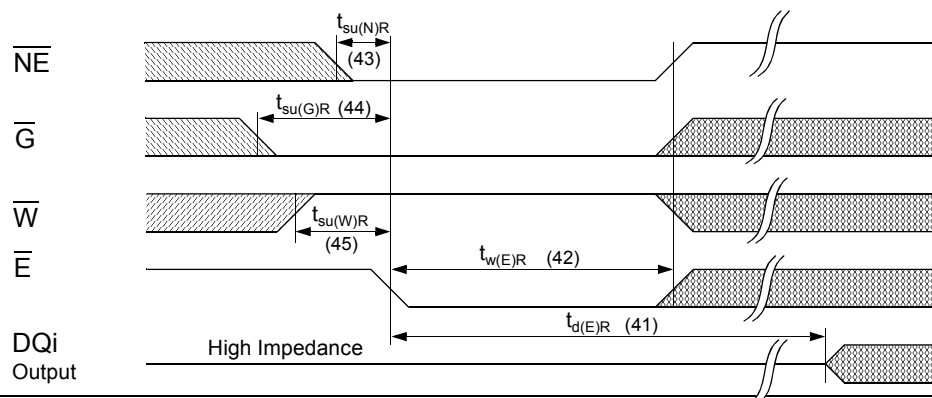
No.	RECALL Cycle G̅-controlled	Symbol		Min.	Max.	Unit
		Alt.	IEC			
46	RECALL Cycle Time	t_{GLQXR}	$t_{d(G)R}$		20#	µs
47	RECALL Initiation Cycle Time	t_{GLNH}	$t_{w(G)R}$	25#		ns
48	N̅E̅ Setup	t_{NLGL}	$t_{su(N)R}$	5#		ns
49	Write Enable Setup	t_{WHGL}	$t_{su(W)R}$	5#		ns
50	Chip Enable Setup	t_{ELGL}	$t_{su(E)R}$	5#		ns

RECALL Cycle: G̅-controlled[o, r]
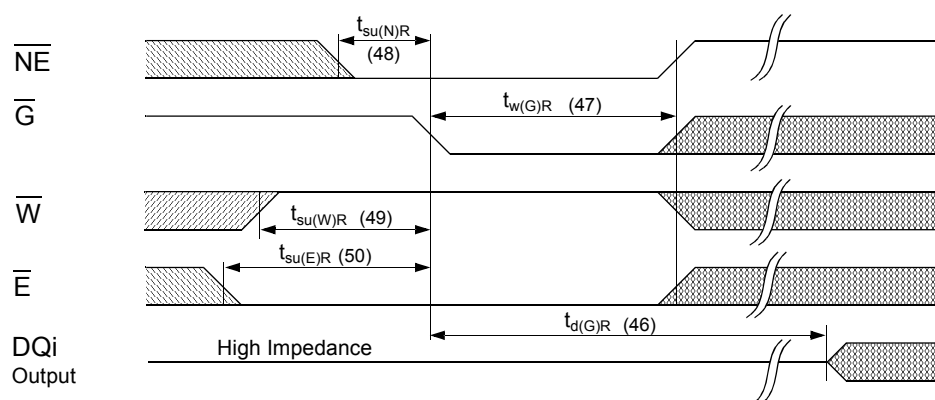
m: Measured with W̅ and N̅E̅ both returned HIGH, and G̅ returned LOW. Note that STORE cycles are inhibited/aborted by $V_{CC} < V_{SWITCH}$ (STORE inhibit).

n: Once $t_{w(W)S}$ has been satisfied by N̅E̅, G̅, W̅ and E̅, the STORE cycle is completed automatically. Any of N̅E̅, G̅, W̅ and E̅ may be used to terminate the STORE initiation cycle.

o: If E̅ is LOW for any period of time in which W̅ is HIGH while G̅ and N̅E̅ are LOW, than a RECALL cycle may be initiated. For E̅-controlled STORE during $t_{w(E)S}$ W̅, G̅, N̅E̅ have to be static.

p: Measured with W̅ and N̅E̅ both HIGH, and G̅ and E̅ LOW.

q: Once $t_{w(N)R}$ has been satisfied by N̅E̅, G̅, W̅ and E̅, the RECALL cycle is completed automatically. Any of N̅E̅, G̅ or E̅ may be used to terminate the RECALL initiation cycle.

r: If W̅ is LOW at any point in which both E̅ and N̅E̅ are LOW and G̅ is HIGH, than a STORE cycle will be initiated instead of a RECALL.

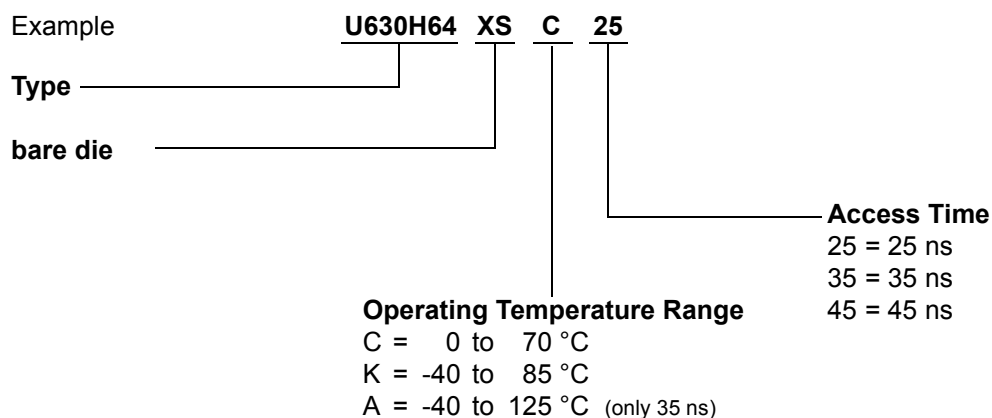**Test Configuration for Functional Check**
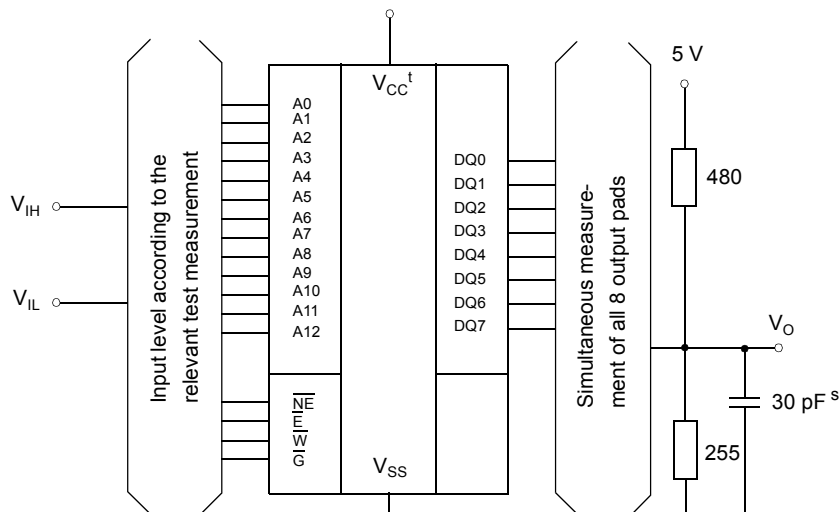
s: In measurement of t_{dis}-times and t_{en}-times the capacitance is 5 pF.

t: Between V_{CC} and V_{SS} must be connected a high frequency bypass capacitor 0.1 µF to avoid disturbances.

Capacitance[e]	Conditions		Symbol	Min.	Max.	Unit
Input Capacitance	V_{CC}	= 5.0 V	C_I		8	pF
	V_I	= V_{SS}				
Output Capacitance	f	= 1 MHz	C_O		7	pF
	T_a	= 25 °C				

All pads not under test must be connected with ground by capacitors.

Ordering Code

Example   **U630H64 XS   C   25**

Type

bare die

Access Time
25 = 25 ns
35 = 35 ns
45 = 45 ns

Operating Temperature Range
C =   0 to   70 °C
K = -40 to   85 °C
A = -40 to 125 °C (only 35 ns)

Bonding Instructions

The U630H64XS has 30 relevant bond pads and 5 additional pads.
The 5 additional pads must not be bonded.
Refer to the bond pad location and identification table for a complete list of bond pads and coordinates.
It is mandatory to use a bond wire on each VCC and two bond wires on VSS bond pad for noise immunity.
The backside of the die is connected to VCC and can be contacted with the substrate in case of the same potential.
The pad VBND has to be connected with VCC in order to enable the HardStore mode of the chip.

U630H64XS

Bond pad location and identification table (origin: down left corner)

Pad	x / µm	y / µm	Pad	x / µm	y / µm
A2	140	360	A3	140	3360
A1	140	170	A4	140	3550
A0	350	140	A5	375	3550
DQ0	875	140	A6	565	3550
DQ1	1085	140	A7	775	3550
DQ2	1360	140	A12	965	3550
VSS	1570	140	$\overline{NE}$	1175	3550
VSS	1725	140	VCC	1545	3550
VCC	1920	140	VCC	1685	3550
DQ3	2130	140	VBND	1870	3550
DQ4	2405	140	$\overline{W}$	2545	3550
DQ5	2615	140	A8	3015	3550
DQ6	2890	140	A9	3205	3550
DQ7	3100	140	A11	3440	3550
$\overline{E}$	3390	170	$\overline{G}$	3440	3550
A10	3390	360			
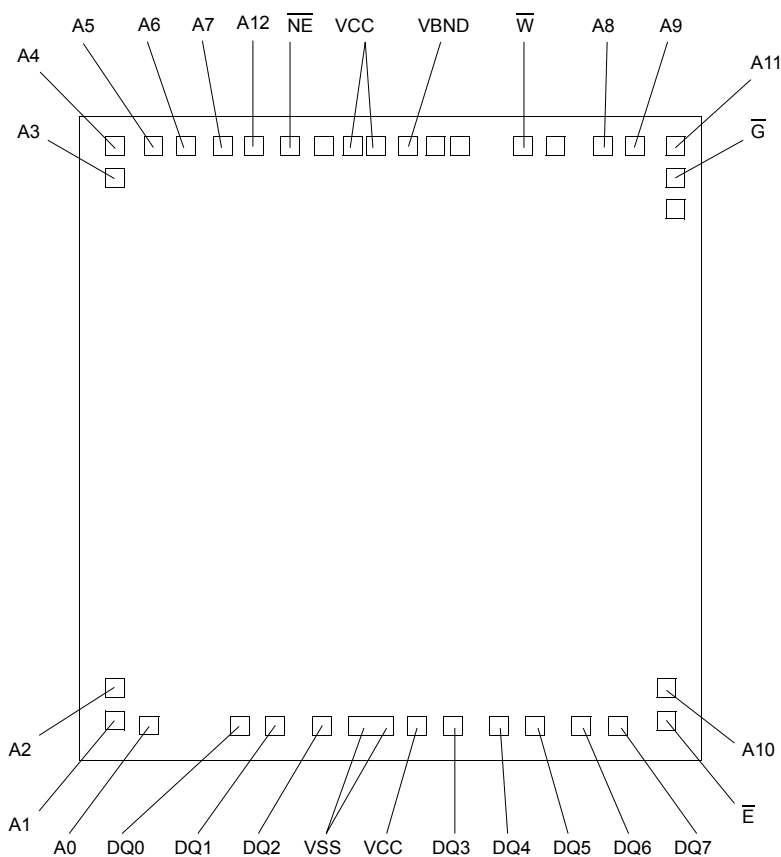
Wafer diameter: 150 mm

Wafer thickness: (390±10)µm

Die size: (3.66 x 3.79) mm (stepping interval)

Bond pad size: (110 x 110) µm

Passivation openings: (100 x 100) µm

Polyimid-passivation: (4±0.5) µm

SIMTEK

Chip Operation

The U630H64 has two separate modes of operation: SRAM mode and nonvolatile mode, determined by the state of the $\overline{NE}$ pad. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to EEPROM (the STORE operation) or from EEPROM to SRAM (the RECALL operation). In this mode SRAM functions are disabled.

SRAM READ

The U630H64 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are LOW while $\overline{W}$ and $\overline{NE}$ are HIGH. The address specified on pads A0 - A10 determines which of the 2048 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{cR}. If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at $t_{a(E)}$ or at $t_{a(G)}$, whichever is later. The data outputs will repeatedly respond to address changes within the t_{cR} access time without the need for transition on any control input pads, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or $\overline{W}$ or $\overline{NE}$ is brought LOW.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW and $\overline{NE}$ is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes HIGH at the end of the cycle. The data on pads DQ0 - 7 will be written into the memory if it is valid $t_{su(D)}$ before the end of a $\overline{W}$ controlled WRITE or $t_{su(D)}$ before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ is kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left LOW, internal circuitry will turn off the output buffers $t_{dis(W)}$ after $\overline{W}$ goes LOW.

Noise Consideration

The U630H64 is a high speed memory and therefore must have a high frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and V_{SS} using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal carefull routing of power, ground and signals will help prevent noise problems.

Hardware Nonvolatile STORE

A STORE cycle is performed when $\overline{NE}$, $\overline{E}$ and $\overline{W}$ are LOW while $\overline{G}$ is HIGH. While any sequence to achieve this state will initiate a STORE, only $\overline{W}$ initiation and $\overline{E}$ initiation are practical without risking an unintentional

SRAM WRITE that would disturb SRAM data. During a STORE cycle, previous nonvolatile data is erased and the SRAM contents are then programmed into nonvolatile elements. Once a STORE cycle is initiated, further input and output is disabled and the DQ0 - 7 pads are tristated until the cycle is completed.

If $\overline{E}$ and $\overline{G}$ are LOW and $\overline{W}$ and $\overline{NE}$ are HIGH at the end of the cycle, a READ will be performed and the outputs will go active, indicating the end of the STORE.

Hardware Nonvolatile RECALL

A RECALL cycle is performed when $\overline{E}$, $\overline{G}$ and $\overline{NE}$ are LOW while $\overline{W}$ is HIGH. Like the STORE cycle, RECALL is initiated when the last of the three clock-signals goes to the RECALL state. Once initiated, the RECALL cycle will take „RECALL Cycle Time" to complete, during which all inputs are ignored. When the RECALL completes, any READ or WRITE state on the input pads will take effect.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The RECALL in no way alters the data in the nonvolatile cells. The nonvolatile data can be recalled an unlimited number of times.

Like the STORE cycle, a transition must occur on some control pads to cause a RECALL, preventing inadvertend multi-triggering.

Automatic Power Up RECALL

On power up, once V_{CC} exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated. The voltage on the V_{CC} pad must not drop below V_{SWITCH} once it has risen above it in order for the RECALL to operate properly. Due to this automatic RECALL, SRAM operation cannot commence until $t_{RESTORE}$ after V_{CC} exceeds V_{SWITCH}. If the U630H64 is in a WRITE state at the end of power up RECALL, the SRAM data will be corrupted.

To help avoid this situation, a 10 KΩ resistor should be connected between $\overline{W}$ and system V_{CC}.

Hardware Protection

The U630H64 offers two levels of protection to suppress inadvertent STORE cycles. If the control signals ($\overline{E}$, $\overline{G}$, $\overline{W}$ and $\overline{NE}$) remain in the STORE condition at the end of a STORE cycle, a second STORE cycle will not be started. The STORE (or RECALL) will be initiated only after a transition on any one of these signals to the required state. In addition to multi-trigger protection, the U630H64 offers hardware protection through V_{CC} Sense. When $V_{CC} < V_{SWITCH}$ the externally initiated STORE operation will be inhibited.

U630H64XS

Low Average Active Power

The U630H64 has been designed to draw significantly less power when $\overline{E}$ is LOW (chip enabled) but the access cycle time is longer than 55 ns.

When $\overline{E}$ is HIGH the chip consumes only standby current.

The overall average current drawn by the part depends on the following items:

1. CMOS or TTL input levels
2. the time during which the chip is disabled ($\overline{E}$ HIGH)
3. the cycle time for accesses ($\overline{E}$ LOW)
4. the ratio of READs to WRITEs
5. the operating temperature
6. the V_{CC} level

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Change record

Date/Rev	Name	Change
01.11.2001	Ivonne Steffens	format revision and release for „Memory CD 2002"
11.08.2003	Matthias Schniebel	adding A-Type with I_{CC1} = 85mA; I_{CC2} = 7mA; I_{CC3} = 15mA; $I_{CC(SB)}$ = 2mA; $I_{CC(SB)1}$ = 27 mA
20.04.2004	Matthias Schniebel	adding „Leadfree Green Package" to ordering information adding „Device Marking"
7.4.2005	Stefan Günther	changing to 10^6 endurance cycles and 100a data retention, delete ESD classes, change ordering code, PDIP 300 on special request, RoHS and Pb- free added, C/K limitation for PDIP deleted
7.4.2005	Steffen Buschbeck	converted into bare die data sheet based on old version of June 11th 2001
7.4.2005	Steffen Buschbeck	converted U630H16XS into U630H64XS
1.0	Simtek	Assigned Simtek Document Control Number