

# UT54LVDM055LV Dual Driver and Receiver

Advanced Data Sheet

March 2005

www.aeroflex.com/lvds



## FEATURES

- ❑ Two drivers and two receivers with individual enables
- ❑ >400.0 Mbps (200 MHz) switching rates
- ❑  $\pm 340\text{mV}$  differential signaling
- ❑ 3.3 V power supply
- ❑ TTL compatible inputs
- ❑ 10mA LVDS output drivers
- ❑ TTL compatible outputs
- ❑ Cold spare all pins
- ❑ Ultra low power CMOS technology
- ❑ Radiation-hardened design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 300 krad(Si) and 1Mrad(Si)
  - Latchup immune ( $\text{LET} > 100 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ )
- ❑ Packaging options:
  - 18-lead flatpack (dual in-line)
- ❑ Standard Microcircuit Drawing 5962-TBD
  - QML Q and V compliant part

## INTRODUCTION

The UT54LVDM055LV Dual Driver/Dual Receiver is designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400.0 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The UT54LVDM055LV Driver accepts low voltage TTL input levels and translates them to low voltage (340mV) differential output signals. In addition, the driver supports a three-state function that may be used to disable the output stage, disabling the load current, and thus dropping the device to a low idle power state.

The UT54LVDM055LV Receiver accepts low voltage (350mV) differential input signals and translates them to 3V CMOS output levels. The receiver supports a three-state function that may be used to multiplex outputs. The receiver also supports OPEN, shorted and terminated ( $35 \Omega$ ) input fail-safe. Receiver output will be HIGH for all fail-safe conditions.

All pins have Cold Spare buffers. These buffers will be high impedance when  $V_{DD}$  is tied to  $V_{SS}$ .

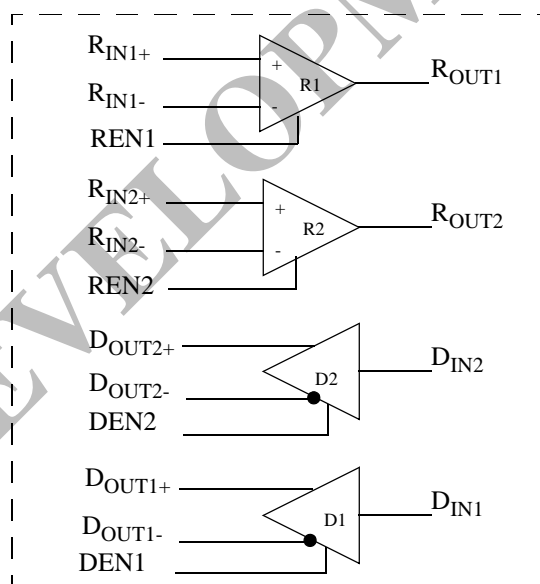
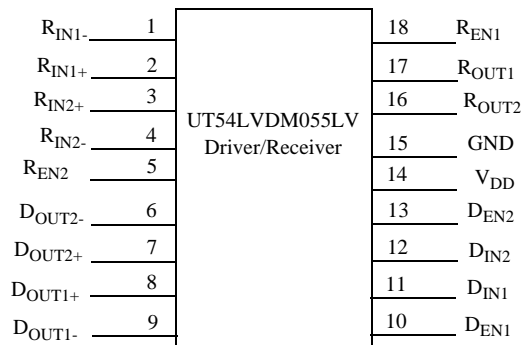


Figure 1. UT54LVDM055LV Dual Driver and Receiver Block Diagram



**Figure 2. UT54LVDM055LV Pinout**

## PIN DESCRIPTION

Pin No.	Name	Description
11, 12	D <sub>IN</sub>	Driver input pin, TTL/CMOS compatible
7, 8	D <sub>OUT+</sub>	Non-inverting driver output pin, LVDS levels
6, 9	D <sub>OUT-</sub>	Inverting driver output pin, LVDS levels
10, 13	D <sub>EN</sub>	Driver active high enable pin
2, 5	R <sub>IN+</sub>	Non-inverting receiver input pin
1, 4	R <sub>IN-</sub>	Inverting receiver input pin
16, 17	R <sub>OUT</sub>	Receiver output pin
5, 18	R <sub>EN</sub>	Receiver
14	V <sub>DD</sub>	Power supply pin, +3.3 ± 0.3V
15	V <sub>SS</sub>	Ground pin

## TRUTH TABLE

Enables	Input	Output	
D <sub>EN</sub>	D <sub>IN</sub>	D <sub>OUT+</sub>	D <sub>OUT-</sub>
L	X	Z	Z
All other combinations of ENABLE inputs	L	L	H
	H	H	L

Enables	Input	Output
R <sub>EN</sub>	R <sub>IN+</sub> - R <sub>IN-</sub>	R <sub>OUT</sub>
L	X	Z
All other combinations of ENABLE inputs	V <sub>ID</sub> ≥ 0.1V	H
	V <sub>ID</sub> ≤ -0.1V	L
	Full Fail-safe OPEN/SHORT or Terminated	H

## APPLICATIONS INFORMATION

The UT54LVDM055LV provides two drivers and two receivers in the same package. Each driver and each receiver has a dedicated output enable pin. This allows maximum flexibility for the device.

The intended application of these devices and signaling technique is for both point-to-point (single termination) and multi-point (double termination) data transmissions over controlled impedance media. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics.)

The UT54LVMS055LV differential line driver is a balanced current source design. A current mode driver, has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The current mode **requires** that a resistive termination be employed to terminate the signal and to complete the loop as shown in Figure 3. AC or unterminated configurations are not allowed. The 10mA loop current will develop a differential voltage of 350mV across the 35 $\Omega$  termination resistor which the receiver detects with a 250mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (350mV - 100mV = 250mV)). The signal is centered around +1.2V (Driver Offset, VOS) with respect to ground as shown in Figure 4. **Note:** The steady-state voltage (VSS) peak-to-peak swing is twice the differential voltage (VOD) and is typically 700mV.

The UT54LVDM055LV receiver's are capable of detecting signals as low as 100mV, over a +/- 1V common-mode range centered around +1.2V. Both receiver input pins should honor their specified operating input voltage range of 0V to +2.4V (measured from each pin to ground). The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. The termination resistor converts the current sourced by the driver into voltages that are detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities, as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

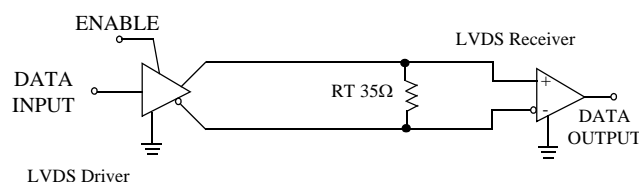


Figure 3. Point-to-Point Application

### Receiver Fail-Safe

The UT54LVDM055LV receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to TTL logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

**Open Input Pins.** The UT54LVDM055LV is a dual receiver device, and if an application requires only 1 receiver, the unused channel inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.

**Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a three-state or power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 35 $\Omega$  termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable offers better balance than flat ribbon cable.

**Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output remains in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device ( $V_{SS}$  to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**(Referenced to  $V_{SS}$ )

SYMBOL	PARAMETER	LIMITS
$V_{DD}$	DC supply voltage	-0.3 to 4.0V
$V_{I/O}$	Voltage on any pin during operation	-0.3 to ( $V_{DD} + 0.3V$ )
	Voltage on any pin during cold spare	-.3 to 4.0V
$T_{STG}$	Storage temperature	-65 to +150°C
$P_D$	Maximum power dissipation	1.25 W
$T_J$	Maximum junction temperature <sup>2</sup>	+150°C
$\Theta_{JC}$	Thermal resistance, junction-to-case <sup>3</sup>	10°C/W
$I_I$	DC input current	±10mA

**Notes:**

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and life test.
3. Test per MIL-STD-883, Method 1012.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS
$V_{DD}$	Positive supply voltage	3.0 to 3.6V
$T_C$	Case temperature range	-55 to +125°C
$V_{IN}$	DC input voltage, receiver inputs DC input voltage, logic inputs	2.4V 0 to $V_{DD}$ for EN, $\overline{EN}$

**DC ELECTRICAL CHARACTERISTICS DRIVER 1, 2**(V<sub>DD</sub> = 3.3V ± 0.3V; -55°C < T<sub>C</sub> < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V <sub>IH</sub>	High-level input voltage	(TTL)	2.0	V <sub>DD</sub>	V
V <sub>IL</sub>	Low-level input voltage	(TTL)	V <sub>SS</sub>	0.8	V
V <sub>OL</sub>	Low-level output voltage	R <sub>L</sub> = 35Ω	0.855		V
V <sub>OH</sub>	High-level output voltage	R <sub>L</sub> = 35Ω		1.750	V
I <sub>IN</sub>	Input leakage current	V <sub>IN</sub> = V <sub>DD</sub> or GND, V <sub>DD</sub> = 3.6V	-10	+10	μA
I <sub>CS</sub>	Cold Spare Leakage Current	V <sub>IN</sub> =3.6V, V <sub>DD</sub> =V <sub>SS</sub>	-20	+20	μA
V <sub>OD</sub> <sup>1</sup>	Differential Output Voltage	R <sub>L</sub> = 35Ω <sup>(figure 5)</sup>	250	400	mV
ΔV <sub>OD</sub> <sup>1</sup>	Change in Magnitude of V <sub>OD</sub> for Complementary Output States	R <sub>L</sub> = 35Ω <sup>(figure 5)</sup>		35	mV
V <sub>OS</sub>	Offset Voltage	R <sub>L</sub> = 35Ω, $(V_{OS} = \frac{V_{OH} + V_{OL}}{2})$	1.055	1.550	V
ΔV <sub>OS</sub>	Change in Magnitude of V <sub>OS</sub> for Complementary Output States	R <sub>L</sub> = 35Ω <sup>(figure 5)</sup>		35	mV
V <sub>CL</sub> <sup>3</sup>	Input clamp voltage	I <sub>CL</sub> = +18mA	-1.5		V
I <sub>OS</sub> <sup>2, 3</sup>	Output Short Circuit Current	V <sub>IN</sub> = V <sub>DD</sub> , V <sub>OUT+</sub> = 0V or V <sub>IN</sub> = GND, V <sub>OUT-</sub> = 0V		25	mA
I <sub>OZ</sub> <sup>3</sup>	Output Three-State Current	EN = 0.8V and $\overline{EN}$ = 2.0 V, V <sub>OUT</sub> = 0V or V <sub>DD</sub> , V <sub>DD</sub> = 3.6V	-10	+10	μA
I <sub>CCL</sub> <sup>3</sup>	Loaded supply current, drivers enabled	R <sub>L</sub> = 35Ω all channels V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> (all inputs)		50.0	mA
I <sub>CCZ</sub> <sup>3</sup>	Loaded supply current, drivers disabled	D <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> EN = V <sub>SS</sub> , $\overline{EN}$ = V <sub>DD</sub>		4.0	mA

**Notes:**

1. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages.
2. Output short circuit current (I<sub>OS</sub>) is specified as magnitude only, minus sign indicates direction only.
3. Guaranteed by characterization.

**AC SWITCHING CHARACTERISTICS DRIVER<sup>1, 2, 3</sup>**(V<sub>DD</sub> = +3.3V ± 0.3V, T<sub>A</sub> = -55 °C to +125 °C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t <sub>PHLD</sub> <sup>6</sup>	Differential Propagation Delay High to Low (figures 6 and 7)	0.3	3.0	ns
t <sub>PLHD</sub> <sup>6</sup>	Differential Propagation Delay Low to High (figures 6 and 7)	0.3	3.0	ns
t <sub>SKD</sub> <sup>4</sup>	Differential Skew (t <sub>PHLD</sub> - t <sub>PLHD</sub> ) (figures 6 and 7)	0	0.4	ns
t <sub>SK1</sub> <sup>1,4</sup>	Channel-to-Channel Skew (figures 6 and 7)	0	0.5	ns
t <sub>SK2</sub> <sup>4,5</sup>	Chip-to-Chip Skew (figure 6 and 7)		2.7	ns
t <sub>TLH</sub> <sup>4</sup>	Rise Time (figures 6 and 7)		1.5	ns
t <sub>THL</sub> <sup>4</sup>	Fall Time (figures 6 and 7)		1.5	ns
t <sub>PHZ</sub> <sup>4</sup>	Disable Time High to Z (figures 8 and 9)		5.0	ns
t <sub>PLZ</sub> <sup>4</sup>	Disable Time Low to Z (figures 8 and 9)		5.0	ns
t <sub>PZH</sub> <sup>4</sup>	Enable Time Z to High (figures 8 and 9)		7.0	ns
t <sub>PZL</sub> <sup>4</sup>	Enable Time Z to Low (figures 8 and 9)		7.0	ns

**Notes:**

1. Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.
2. Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z<sub>O</sub> = 50, t<sub>r</sub> ≤ 1ns, and t<sub>f</sub> ≤ 1ns.
3. C<sub>L</sub> includes probe and jig capacitance.
4. Guaranteed by characterization
5. Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.
6. May be tested at higher load capacitance and the limit interpolated from characterization data to guarantee this parameter.

**DC ELECTRICAL CHARACTERISTICS RECEIVER<sup>1, 2</sup>**(V<sub>DD</sub> = 3.3V ± 0.3V; -55°C < T<sub>C</sub> < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V <sub>IH</sub>	High-level input voltage	(TTL)	2.0		V
V <sub>IL</sub>	Low-level input voltage	(TTL)		0.8	V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 2mA, V <sub>DD</sub> = 3.0V		0.25	V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -0.4mA, V <sub>DD</sub> = 3.0V	2.7		V
I <sub>IN</sub>	Logic input leakage current	Enables = EN/ $\overline{\text{EN}}$ = 0 and 3.6V, V <sub>DD</sub> = 3.6	-10	+10	μA
I <sub>I</sub>	Receiver input Current	V <sub>IN</sub> = 2.4V	-15	+15	μA
I <sub>CS</sub>	Cold Spare Leakage Current	V <sub>IN</sub> =3.6V, V <sub>DD</sub> =V <sub>SS</sub>	-20	+20	μA
V <sub>TH</sub> <sup>3</sup>	Differential Input High Threshold	V <sub>CM</sub> = +1.2V		+100	mV
V <sub>TL</sub> <sup>3</sup>	Differential Input Low Threshold	V <sub>CM</sub> = +1.2V	-100		mV
I <sub>OZ</sub> <sup>3</sup>	Output Three-State Current	Disabled, V <sub>OUT</sub> = 0 V or V <sub>DD</sub>	-10	+10	μA
V <sub>CL</sub>	Input clamp voltage	I <sub>CL</sub> = +18mA	-1.5		V
I <sub>OS</sub> <sup>2, 3</sup>	Output Short Circuit Current	Enabled, V <sub>OUT</sub> = 0 V <sup>2</sup>	-15	-130	mA
I <sub>CC</sub> <sup>3</sup>	Supply current, receivers enabled	EN, $\overline{\text{EN}}$ = V <sub>DD</sub> or V <sub>SS</sub> Inputs Open		15	mA
I <sub>CCZ</sub> <sup>3</sup>	Supply current, receivers disabled	EN = V <sub>SS</sub> , $\overline{\text{EN}}$ = V <sub>DD</sub> Inputs Open		4	mA

**Notes:**

1. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.
2. Output short circuit current (I<sub>OS</sub>) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.
3. Guaranteed by characterization.

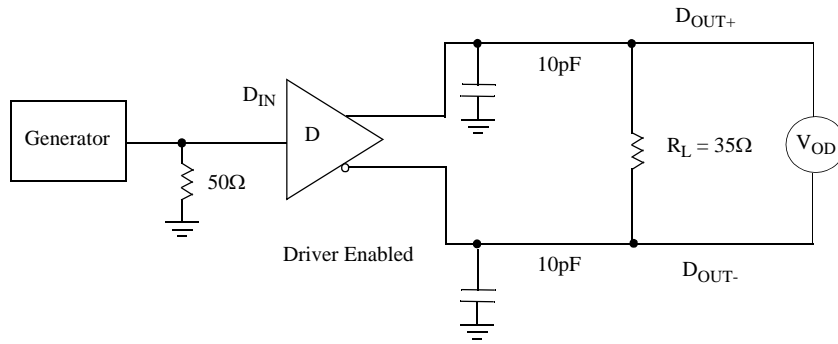
**AC SWITCHING CHARACTERISTICS RECEIVER<sup>1, 2, 3</sup>**(V<sub>DD</sub> = +3.3V ± 0.3V, T<sub>A</sub> = -55 °C to +125 °C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t <sub>PHLD</sub> <sup>6</sup>	Differential Propagation Delay High to Low CL = 10pf (figures 4 and 5)	1.0	4.0	ns
t <sub>PLHD</sub> <sup>6</sup>	Differential Propagation Delay Low to High CL = 10pf (figures 4 and 5)	1.0	4.0	ns
t <sub>SKD</sub> <sup>4</sup>	Differential Skew (t <sub>PHLD</sub> - t <sub>PLHD</sub> ) (figures 4 and 5)	0	0.35	ns
t <sub>SK1</sub> <sup>1,4</sup>	Channel-to-Channel Skew (figures 4 and 5)	0	0.5	ns
t <sub>SK2</sub> <sup>4,5</sup>	Chip-to-Chip Skew (figures 4 and 5)		1.5	ns
t <sub>TLH</sub> <sup>4</sup>	Rise Time (figures 4 and 5)		1.2	ns
t <sub>THL</sub> <sup>4</sup>	Fall Time (figures 4 and 5)		1.2	ns
t <sub>PHZ</sub> <sup>4</sup>	Disable Time High to Z (figures 6 and 7)		12	ns
t <sub>PLZ</sub> <sup>4</sup>	Disable Time Low to Z (figures 6 and 7)		12	ns
t <sub>PZH</sub> <sup>4</sup>	Enable Time Z to High (figures 6 and 7)		12	ns
t <sub>PZL</sub> <sup>4</sup>	Enable Time Z to Low (figures 6 and 7)		12	ns

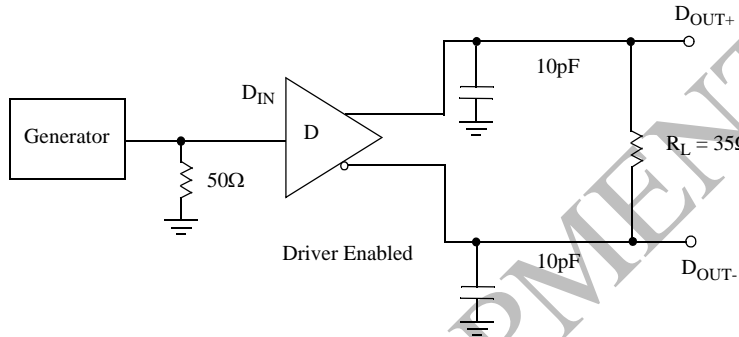
**Notes:**

1. Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.
2. Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z<sub>0</sub> = 50Ω, t<sub>r</sub> and t<sub>f</sub> (0% - 100%) ≤ 1ns for R<sub>IN</sub> and t<sub>r</sub> and t<sub>f</sub> ≤ 1ns for EN or EN̄.
3. C<sub>L</sub> includes probe and jig capacitance.
4. Guaranteed by characterization.
5. Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.
6. May be tested at higher load capacitance and the limit interpolated from characterization data to guarantee this parameter.

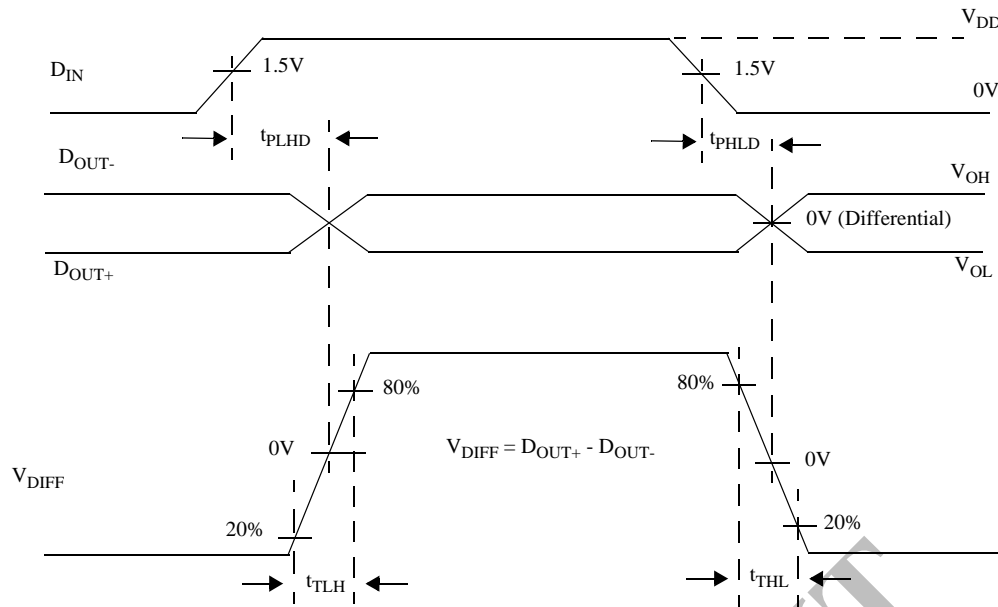




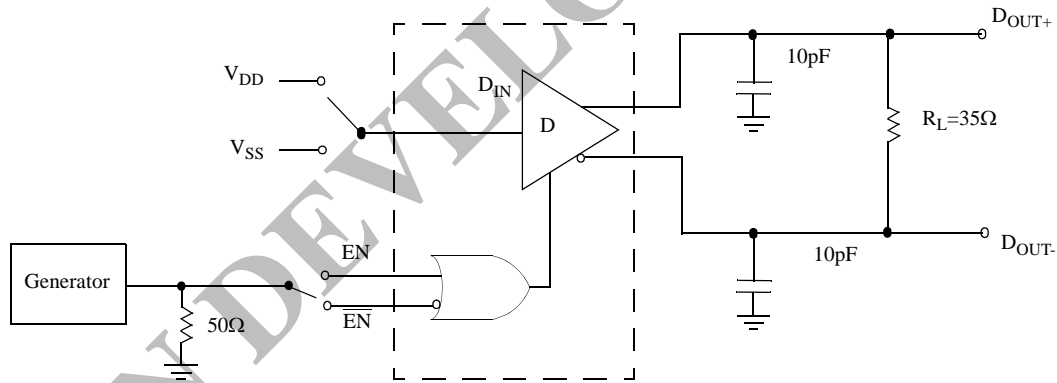
**Figure 4. Driver  $V_{OD}$  and  $V_{OS}$  Test Circuit or Equivalent Circuit**



**Figure 5. Driver Propagation Delay and Transition Time Test Circuit or Equivalent Circuit**



**Figure 6. Driver Propagation Delay and Transition Time Waveforms**



**Figure 7. Driver Three-State Delay Test Circuit or Equivalent Circuit**

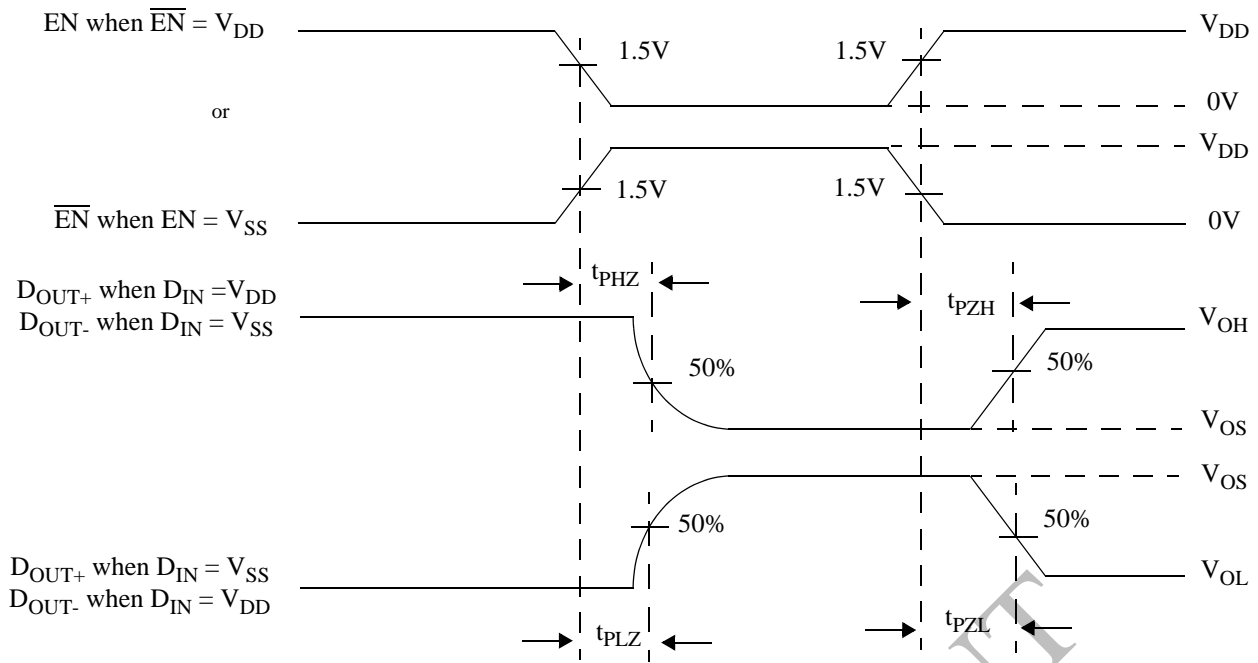
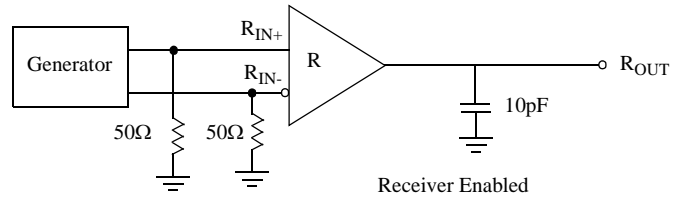
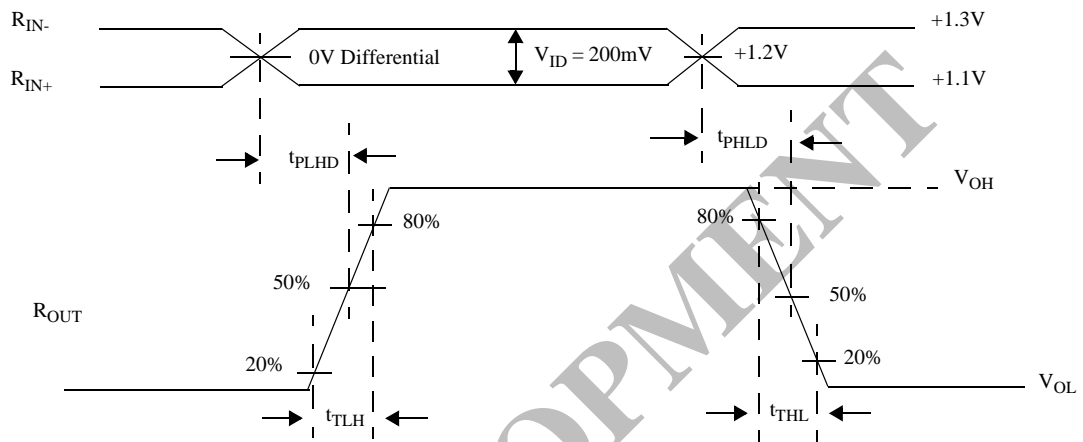


Figure 8. Driver Three-State Delay Waveform

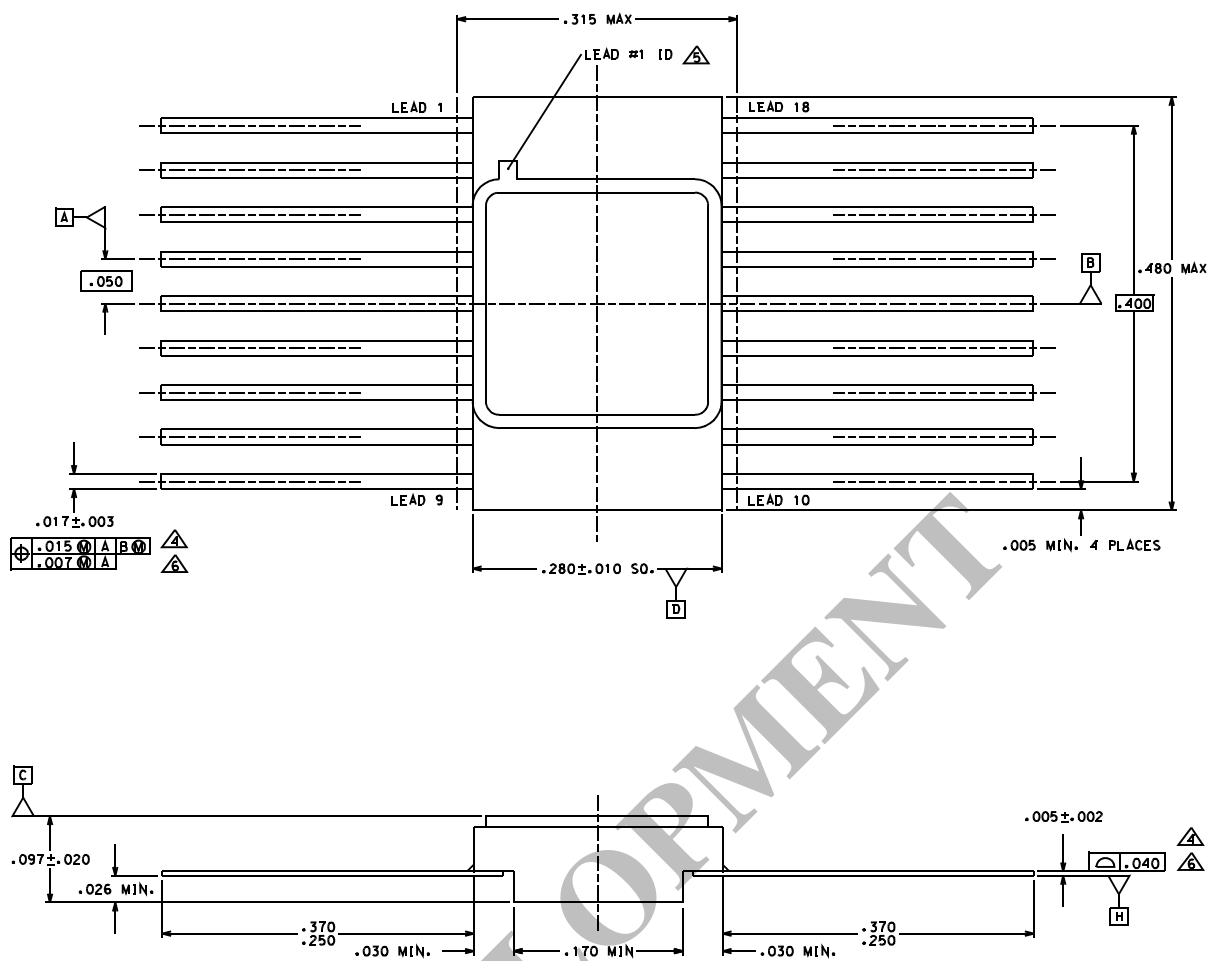


**Figure 9. Receiver Propagation Delay and Transition Time Test Circuit or Equivalent Circuit**



**Figure 10. Receiver Propagation Delay and Transition Time Wave-**





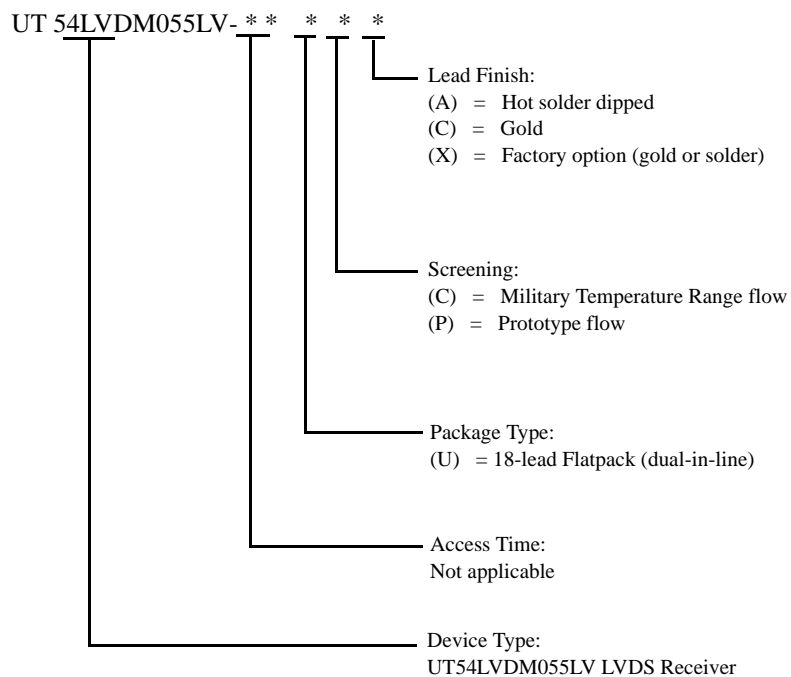
#### Notes:

1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to VSS.
3. Lead finishes are in accordance to MIL-PRF-38535.
4. Lead position and coplanarity are not measured.
5. ID mark symbol is vendor option and may be different than shown.
6. With solder, increase maximum by 0.003.
7. Package weight 0.8 grams.

Figure 13. 18-pin Ceramic Flatpack

## ORDERING INFORMATION

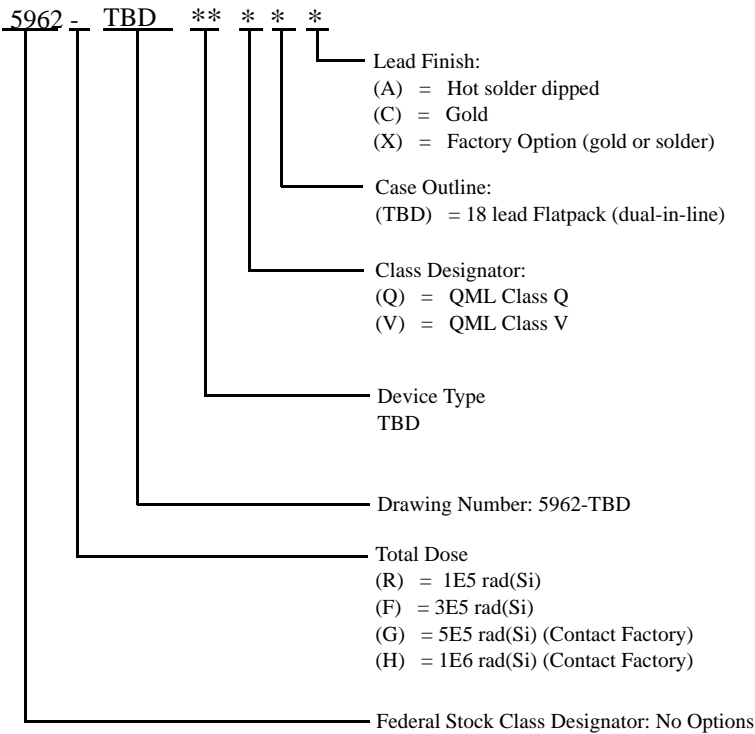
### UT54LVDM055LV DUAL DRIVER/RECEIVER:



#### Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per Aeroflex Colorado Springs Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

**UT54LVDM055LV DUAL DRIVER/RECEIVER: SMD**



- Notes:**
- 1. Lead finish (A, C, or X) must be specified.
  - 2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
  - 3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.



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