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Intel® LXT905 Universal 10BASE-T Transceiver with 3.3 V Support

Datasheet

The Intel® LXT905 Universal 10BASE-T Transceiver is designed for IEEE 802.3 physical layer applications. It provides, in a single CMOS device, all of the active circuitry for interfacing most standard IEEE 802.3 controllers to 10BASE- T media.

The LXT905 functions include the following:

- Manchester encoding/decoding
- Receiver squelch and transmit pulse shaping,
- Jabber
- Link integrity testing
- Reversed polarity detection/correction.

The LXT905 drives the 10BASE-T twisted-pair cable, with only a simple isolation transformer, using a single 3.3 V or 5 V power supply. Integrated filters simplify the design work required for FCC-compliant EMI performance.

The LXT905 is part of the Intel Carrier Class Ethernet family of products. The LXT905 Universal Transceiver offers 10BASE-T connectivity solutions that support operations over an extended temperature range, while providing features that increase reliability. The device has an operational lifetime of at least ten years, with less than 100 failures per billion hours, and is available a minimum of five years after the introduction of the product.

Intel Carrier Class Ethernet products are ideal for applications where equipment must function reliably under environmentally controlled conditions, such as base stations, telecom/network switches, factory floor equipment, and industrial computers.

Applications

- Access devices (DSL, Cable Modems, and Set-top Boxes)
- Routers/Bridges/Switches/Hubs
- Telecom Backplane
- USB to Ethernet Converters

Product Features

- Transparent 3.3V or 5V operation
- Integrated filters – Simplifies FCC compliance
- Integrated Manchester encoder/decoder
- 10BASE-T compliant transceiver
- Automatic polarity correction
- SQE enable/disable
- Four LED drivers
- Full-duplex capability
- Power-down mode with tri-state
- Available in 28-pin PLCC and 32-pin LQFP packages
- Commercial Temperature Range (0 to +70ºC)
- Extended Temperature Range (-40 to +85ºC)

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Revision History

Revision Number: 004 Revision Date: 19-Oct-2005	
Page	**Description**
37	Added Section 6.0, "Top-Label Device Marking" and Figure 29 through Figure 32.
39	Modified Table 16 "Product Information" and Figure 33 "Ordering Information - Sample" with RoHS information.

Revision Number: 003 Revision Date: February 6, 2004	
Page	**Description**
37	Modified Table 16 "Product Information" under Section 6.0, "Ordering Information" (replaced MM numbers).

Revision Number: 002 Revision Date: June 2001	
Page	**Description**
1	New information under "Applications".
1	Added new carrier class information (paragraphs 3 and 4).
22	Added +5V to Line Status, Figure 8.
23	Added +5V to Line Status, Figure 9.
25	Added second paragraph under Test Specifications "Note" regarding Quality and Reliability issues.
25	Deleted Ambient operating temperatures from Table 5.
37	Added new diagram and table for LXT905PC/PE mechanical specifications.

Figure 1. Block Diagram
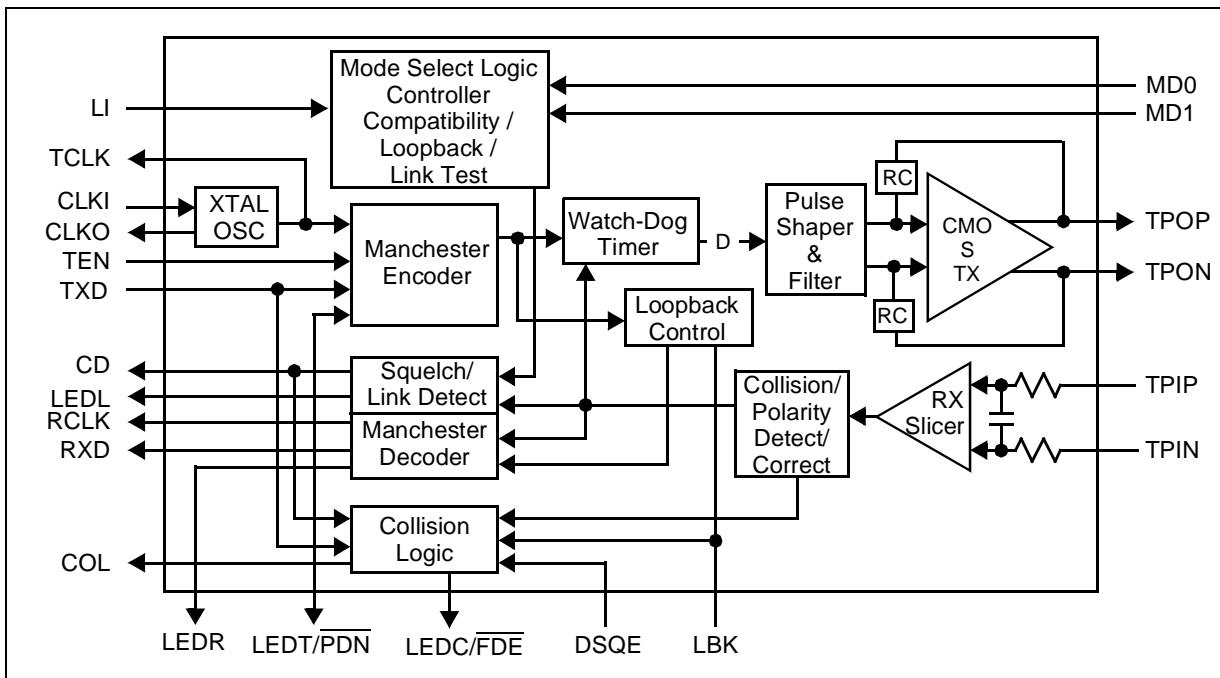
1.0   Pin Assignments and Signal Descriptions

Figure 2. Pin Assignments
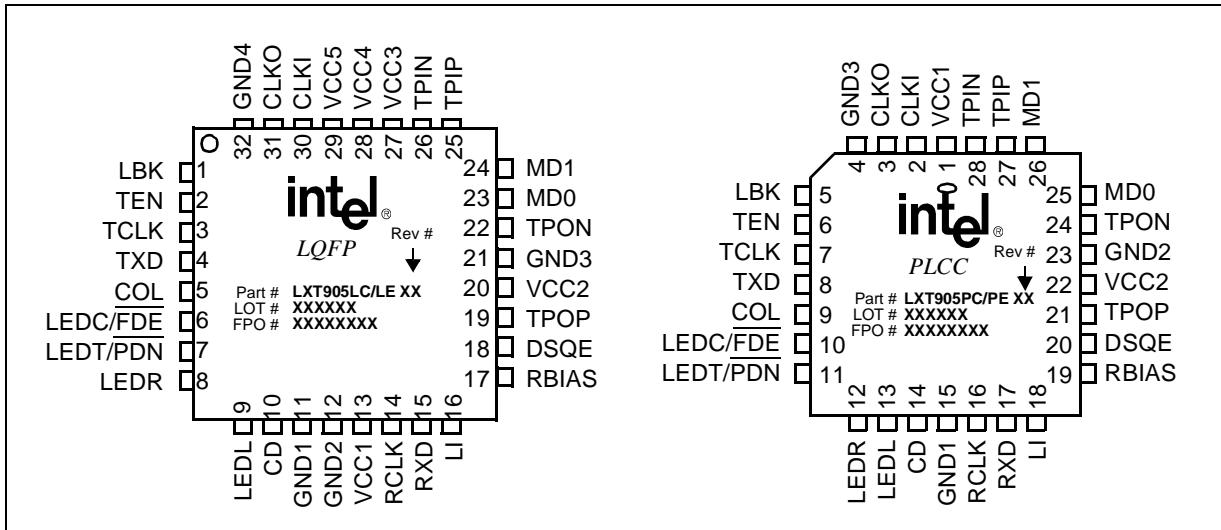
Table 1. Signal Descriptions (Sheet 1 of 2)

LQFP Pin #	PLCC Pin #	Symbol	I/O	Description
13	1	VCC1	–	**Power Inputs 1 through 5.** Power supply inputs of 3.3 V or 5 V.
20	22	VCC2	–	
27	–	VCC3	–	
28	–	VCC4	–	
29	–	VCC5	–	
30	2	CLKI	I	**Crystal Oscillator.** Connect a 20 MHz crystal across these pins, or apply a 20 MHz clock at CLKI, with CLKO left open.
31	3	CLKO	O	
11	15	GND1	–	**Ground.**
12	23	GND2	–	
21	4	GND3	–	
32	–	GND4	–	
1	5	LBK	I	**Loopback.** When High, forces internal loopback. Disables collision and the transmission of both data and link pulses. Pulled Low internally.[1]
2	6	TEN	I	**Transmit Enable.** Enables data transmission and starts the Watch-Dog Timer (WDT). Synchronous to TCLK. Pulled Low internally[1].
3	7	TCLK	O	**Transmit Clock.** A 10 MHz clock output. Connect this clock signal directly to the transmit clock input of the controller.
4	8	TXD	I	**Transmit Data.** Input signal containing NRZ data to transmit on the network. Connect TXD directly to the transmit data output of the controller. Pulled Low internally[1].
5	9	COL	O	**Collision Signal.** Output that drives the collision detect input of the controller.
6	10	LEDC/$\overline{\text{FDE}}$	O I	**LED Collision or Full-Duplex Enable.** **LEDC** is an open drain driver for the collision indicator, and pulls Low during collision. Extends LED "on" (which is Low output) time by approximately 100 ms. $\overline{\text{FDE}}$ enables full-duplex mode (external loopback) if tied Low externally. Pulled High internally[1].
7	11	LEDT/$\overline{\text{PDN}}$	O I	**LED Transmit or Power Down.** **LEDT** is an open drain driver for the transmit indicator. Extends LED "on" (which is Low output) time by approximately 100 ms. Pulls output Low during transmit.[2] If externally tied Low, the LXT905 goes to power down state ($\overline{\text{PDN}}$). In power-down mode, LEDT tristates all logic inputs and outputs.
8	12	LEDR	O	**LED Receive.** Open drain driver for the receive indicator LED. Extends LED "on" (which is Low output) time by approximately 100 ms. Pulls output Low during receive. Pulled High internally[1].
9	13	LEDL	O	**LED Link.** Open drain driver for link integrity indicator. Pulls output Low during link test pass. Pulled High internally[1].

1. Externally pull-up or pull-down each pin separately using a 10 k Ω, 1% termination resistor, or tie directly to VCC or ground.
2. Do not allow this pin to float. If unused, tie High.

Table 1. Signal Descriptions (Sheet 2 of 2)

LQFP Pin #	PLCC Pin #	Symbol	I/O	Description
10	14	CD	O	**Carrier Detect.** An output for notifying the controller that activity exists on the network.
14	16	RCLK	O	**Receive Clock.** A recovered 10 MHz clock that is synchronous to the received data and connects to the controller receive clock input.
15	17	RXD	O	**Receive Data.** Output signal connected directly to the receive data input of the controller.
16	18	LI	I	**Link Enable.** Controls link integrity test. • Enabled when LI is High. • Disabled when LI is Low.
17	19	RBIAS	I	**Bias Circuitry.** A 7.5 kW 1% resistor to ground at this pin controls operating circuit bias.
18	20	DSQE	I	**SQE Disable.** • When DSQE is High, the SQE function is disabled. • When DSQE is Low, the SQE function is enabled. Disable SQE for normal operation in Hub/Switch/Repeater applications. Pulled Low internally[1].
19 22	21 24	TPOP TPON	O O	**Twisted-Pair Outputs.** Differential outputs to the twisted-pair cable. The outputs are pre-equalized.
23 24	25 26	MDO MDI	I I	**Mode Select 0 and 1.** Mode select pins determine controller compatibility mode in accordance with Table 2. Pulled Low internally[1].
25 26	27 28	TPIP TPIN	I I	**Twisted-Pair Inputs.** A differential input pair from the twisted-pair cable. Receive filter is integrated on-chip. Does not require external filters.

1. Externally pull-up or pull-down each pin separately using a 10 k Ω, 1% termination resistor, or tie directly to V_{CC} or ground.
2. Do not allow this pin to float. If unused, tie High.

2.0 Functional Description

2.1 Introduction

The Intel® LXT905 Universal 10BASE-T Transceiver performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions, as defined in the *IEEE 802.3* specification. It functions as an integrated PLS/MAU for use with 10BASE-T twisted-pair networks.

The LXT905 interfaces a back-end controller to a twisted-pair (TP) cable. The controller interface includes a transmit and receive clock and NRZ data channels, and mode control logic and signaling. The twisted-pair interface comprises the following two circuits:

- Twisted-Pair Input (TPI)
- Twisted-Pair Output (TPO).

In addition to the two basic interfaces, the LXT905 contains an internal crystal oscillator, and four LED drivers for visual status reporting.

The back-end controller side of the interface defines functions.

- The LXT905 transmit function refers to data transmitted by the back-end to the twisted-pair network.
- The LXT905 receive function refers to data received by the back-end of the twisted-pair network.

The LXT905 performs all required functions defined in the *IEEE 802.3 10BASE-T MAU* specification as follows:

- Collision detection
- Link integrity testing
- Signal quality error messaging
- Jabber control
- Loopback

Figure 3. TPO Output Waveform
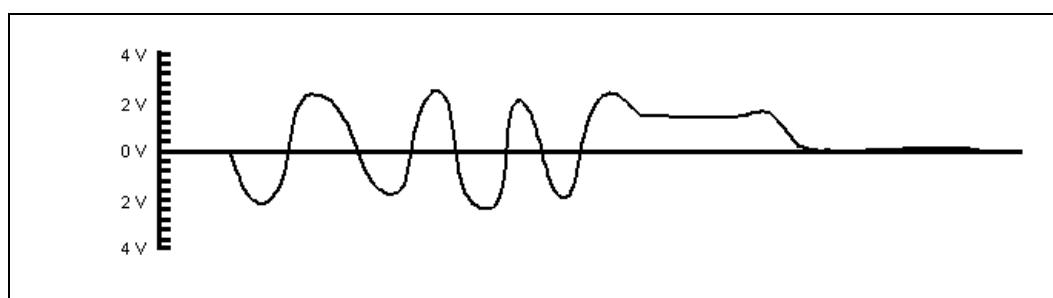
2.2   Controller Compatibility Modes

The LXT905 is compatible with most industry standard controllers, including devices from Advanced Micro Devices* (AMD), Fujitsu*, National Semiconductor*, Seeq*, Motorola*, and Texas Instruments*. Four different control signal timing and polarity schemes (Modes 1 through 4) provide this compatibility. The MD0 and MD1 mode select pins determine controller compatibility modes (see Table 2). Refer to Section 4.0, "Test Specifications" on page 23 for timing diagrams and parameters.

2.3   Transmit Function

The LXT905 receives NRZ data from the controller at the TXD input, as shown in Figure 1 "Block Diagram" on page 6, and passes it through a Manchester encoder. The LXT905 then transfers encoded data to the twisted-pair network (TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP, as shown in Figure 3 "TPO Output Waveform" on page 10. The TPO output is pre-distorted and pre-filtered to meet the 10BASE-T jitter template. An internal, continuous resistor-capacitor filter removes any high-frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC compliant EMI performance. During idle periods, the LXT905 transmits link integrity test pulses on the TPO circuit (if LI is enabled and LBK is disabled).

Table 2.   Controller Compatibility Mode Options

Controller Mode	MD1	MD0
Mode 1 - For Motorola* MC68EN360 or compatible controllers (AMD* AM7990)	Low	Low
Mode 2 - For Intel* 82596 or compatible controllers[1]	Low	High
Mode 3 - For Fujitsu* MB86950, MB86960 or compatible controllers (Seeq* 8005)[2]	High	Low
Mode 4 - For TI* TMS380C26 or compatible controllers	High	High
1. Refer to the MAC Interface Design Guide for Intel Controllers Application Note when designing with Intel controllers. 2. SEEQ* controllers require inverters on CLKI, LBK, RCLK, and COL.		

2.4 Jabber Control Function

Figure 4 is a state diagram of the LXT905 jabber control function. The LXT905 on-chip Watch-Dog Timer (WDT) prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the WDT disables the transmit and loopback functions and activates the COL pin. Once the LXT905 is in the jabber state, the TXD circuit must remain idle for a period of 0.25 to 0.75 seconds before it exits the jabber state.

Figure 4. Jabber Control Function

```
                        Power On

                    ┌──────────────┐
                    │  No Output   │
                    └──────────────┘
                           │ DO=Active
                    ┌──────────────────────┐
                    │  Nonjabber Output     │
                    ├──────────────────────┤
                    │ Start_XMIT_MAX_Timer  │
                    └──────────────────────┘
       DO=Idle                │ DO=Active ∗
                              │ XMIT_Max_Timer_Done
                    ┌──────────────┐
                    │     Jab      │
                    ├──────────────┤
                    │ XMIT=Disable │
                    │ LPBK=Disable │
                    │ CI=SQE       │
                    └──────────────┘
                           │ DO=Idle
                    ┌──────────────────────┐
                    │   Unjab Wait          │
                    ├──────────────────────┤
                    │ Start_Unjab_Timer     │
                    │ XMIT=Disable          │
                    │ LPBK=Disable          │
                    │ CI=SQE                │
                    └──────────────────────┘

     Unjab_ Timer_Done        DO=Active ∗
                              Unjab_Timer_Not_Done
```
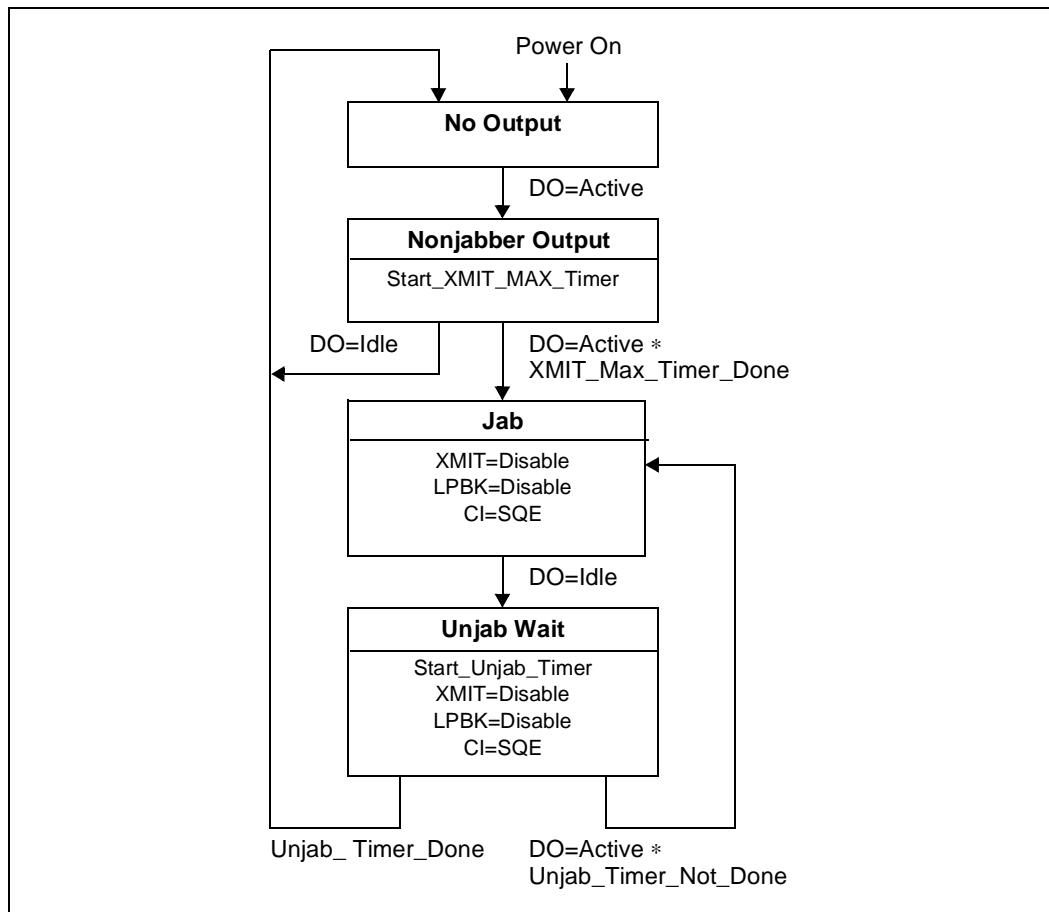
2.5   SQE Function

The LXT905 supports the Signal Quality Error (SQE) function (see Figure 5). After every successful transmission on the 10BASE-T network, the LXT905 transmits the SQE signal for 10 bit times (BT) ± 5BT on the COL pin of the device.

- To disable the SQE function for repeater/switch applications, set DSQE High.
- To enable the SQE function, set DSQE Low.

Figure 5. SQE Function
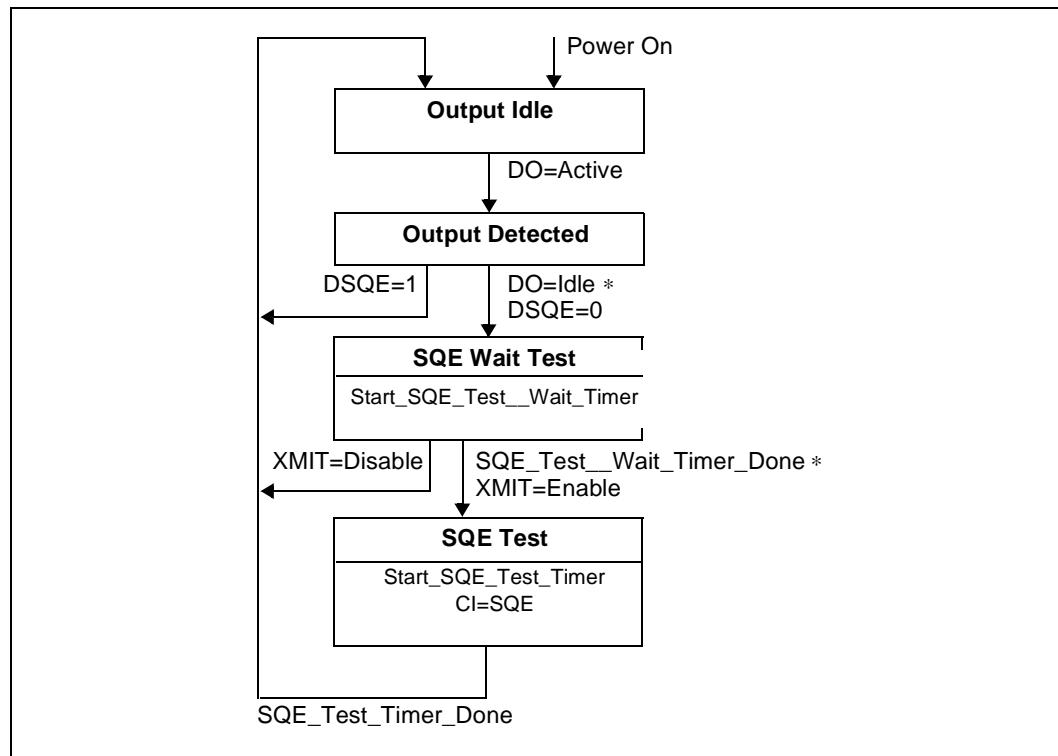
2.6   Receive Function

The LXT905 receive function acquires timing and data from the twisted-pair network (TPI circuit). The LXT905 passes valid received signals through the on-chip filters and Manchester decoder, then outputs them as decoded NRZ data on the RXD pin, and as receive timing on the RCLK pin.

An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. The receive function activates only when receiving valid data streams above the squelch level with proper timing.

If the differential signal at the TPI circuit inputs falls below 85 percent of the threshold level (unsquelched) for 8 bit times (typical), the LXT905 receive function enters the idle state. The LXT905 automatically corrects reversed polarity on the TPI circuit.

2.7 Polarity Reverse Function

The LXT905 polarity reverse function uses both link pulses and end-of-frame data to determine the polarity of the received signal.

- If you disable Link Integrity testing, polarity detection is based only on received data. A reversed polarity condition exists if the LXT905 detects eight consecutive opposite receive link pulses, without receiving a link pulse of the expected polarity.

- Reversed polarity also occurs if the LXT905 receives four consecutive frames with a reversed start-of-idle.

- Whenever the LXT905 receives a correct polarity frame or a correct link pulse, it resets these two counters to zero.

- If the LXT905 enters the link fail state, and does not receive any valid data or link pulses within 96 to 128 ms, it resets the polarity to the default non-flipped condition.

Polarity correction is always enabled.

2.8 Collision Detection Function

A collision is the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT905 reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data passes to the back-end over the RXD circuit, disabling normal loopback. Figure 6 is a state diagram of the LXT905 collision detection function.

Figure 6. Collision Detection Function
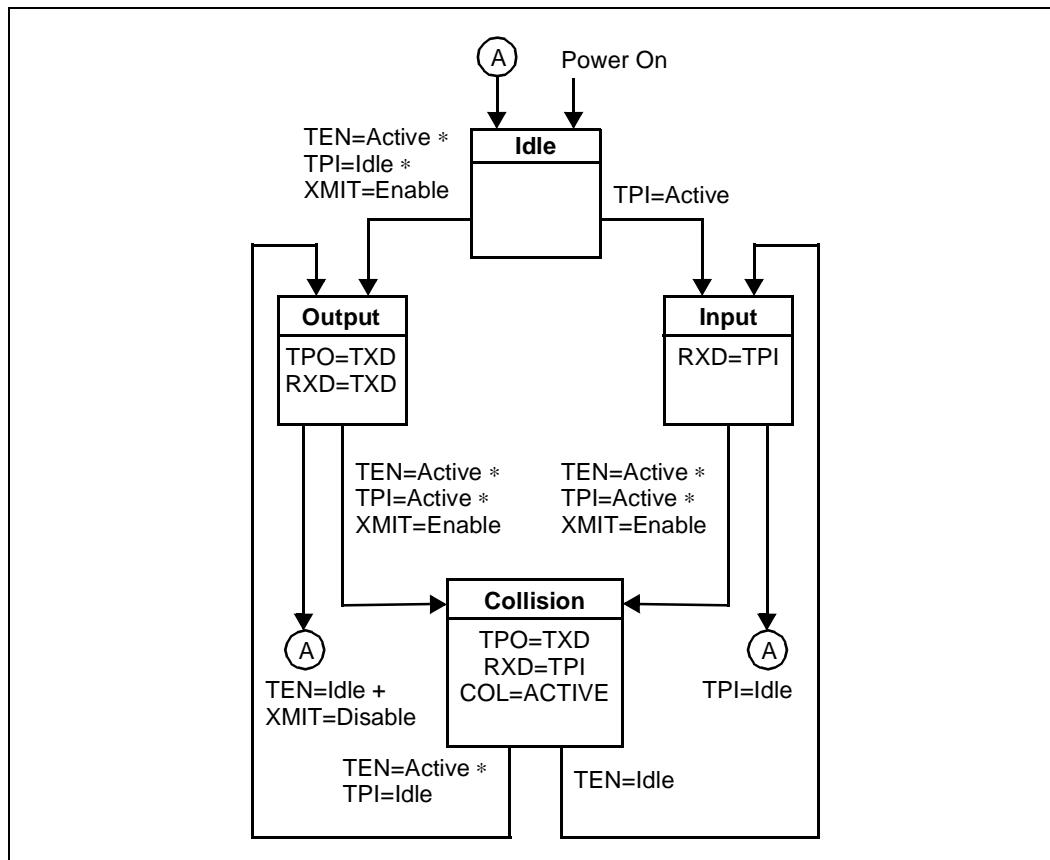
2.9   Loopback Functions

2.9.1   Internal Loopback

The LXT905 provides a standard loopback mode, as specified in the IEEE specification for the twisted-pair port. It also provides a forced internal loopback mode. Loopback mode operates in conjunction with the transmit function. The LXT905 internally loops back data that the MAC transmits, from the TXD pin, through the Manchester encoder/decoder, to the RXD pin, and returning to the MAC.

A data collision disables standard loopback mode, clearing the RXD circuit for the TPI data. Link fail, jabber, and full-duplex states also disable standard loopback. Loopback is always enabled during forced internal loopback mode.

2.9.2   External Loopback/Full Duplex

The LXT905 also provides an external loopback test mode for system-level testing. When both LEDC/$\overline{\text{FDE}}$ and LBK are Low, the LXT905 enables external loopback and full-duplex mode, and disables internal loopback circuits, SQE, and collision detection. Refer to Table 3 for a summary of loopback and duplex modes.

Table 3. Loopback Modes

Pin Settings		Mode Description
LBK	LEDC/FDE	
Low	Low	**Disable internal loopback.** Enable external loopback test mode and full-duplex mode.
Low	High	**Standard loopback mode (default).** Internally loops back data that the MAC transmitted, and returns the data to the MAC, except during collision. A data collision disables standard loopback, clearing RXD for data on the twisted-pair port.
High	Low	**Not Used.**
High	High	**Forced internal loopback.** Loops-back transmit data on the receive data bus, and ignores the twisted-pair port.

2.10   Link Integrity Test Function

Figure 7 is a state diagram of the LXT905 link integrity test function. The link integrity test determines the status of the receive side twisted-pair cable. Link integrity testing is enabled when LI is tied High. When enabled, the receiver recognizes link integrity pulses that transmit in the absence of receive traffic. If the LXT905 does not detect any serial data stream or link integrity pulses within 50~150 ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The LXT905 ignores any link integrity pulse with an interval less than 2~7 ms. The LXT905 remains in the link fail state until it detects either a serial data packet, or two or more link integrity pulses.

Figure 7. Link Integrity Test Function
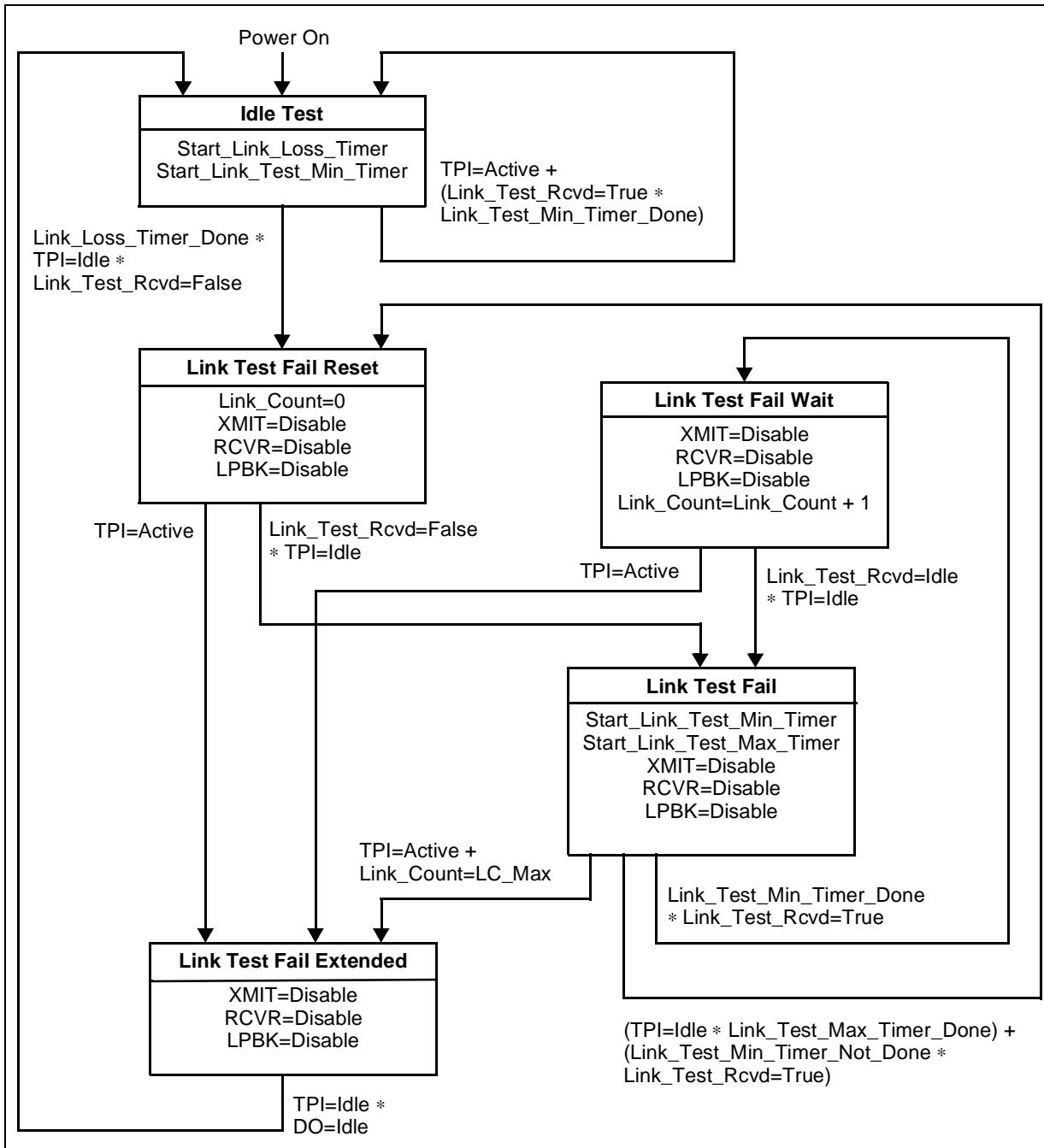
3.0   Application Information

3.1   Introduction

Figure 8 "Intel® Controller Application (Mode 2)" on page 20 through Figure 10 "Intel® LXT905 PHY/Motorola* MC68EN360 Interface for Full-Duplex 10BASE-T (Mode 1)" on page 22 show typical LXT905 applications. These diagrams group similar pins; they do not portray the actual chip pinout. The controller interface pins [Transmit Data (TXD), Transmit Clock (TCLK) Transmit Enable (TEN), Receive Data (RXD), Receive Clock (RCLK), Collision Signal (COL), and Carrier Detect (CD)] are at the upper left of the diagram.

Power and ground pins are at the bottom of each diagram. $V_{CC}1$ and $V_{CC}2$ use a single power supply, with decoupling capacitors installed between the power and ground buses. Either a 5 V or 3.3 V supply can power Vcc.

3.1.1   Termination Circuitry

The LXT905 pulls several I/O pins up or down internally, to keep the signals from floating. Intel recommends hard-wiring these pins either High or Low. Externally pull-up pins (LEDT/PDN, LEDC/FDE, LEDR, LEDL) and pull-down pins (LBK, TEN, TXD, DSQE, MDO, MDI) separately, using a 10 k Ω, 1% resistor, or tie them directly to V_{CC} or ground.

3.1.2   Twisted-Pair Interface

The Twisted-Pair interface (TPOP/N and TPIP/N) is at the upper right of the diagram. The I/O pairs have impedance-matching resistors for 100 Ω UTP, but do not require any external filters.

3.1.3   RBIAS Pin

The RBIAS pin sets the levels for the LXT905 output drivers. The LXT905 requires a 7.5 k Ω, 1% resistor directly connected between the RBIAS pin and ground. Locate this resistor as close to the device as possible. Keep the traces as short as possible, isolated from all other high-speed signals.

3.1.4   Crystal Information

Table 4 lists some suitable crystals based on limited evaluation. Test and validate all crystals before committing to a specific component.

Table 4.   Suitable Crystals

Manufacturer	Part Number
MTRON	MP-1
	MP-2

3.1.5   Magnetic Information

The LXT905 requires a 1:1 turns ratio for the receive transformer, and a 1:2 turns ratio for the transmit transformer. The Intel® Magnetic Manufacturers Application Note (document number 248991) lists transformers suitable for the applications described in this datasheet.

Note: Test and validate all magnetics before committing to a specific component.

3.2   Typical 10BASE-T Application

Figure 8 is a typical LXT905 application. The DTE connects to a 10BASE-T network through the twisted-pair RJ-45 connector. With MD0 tied high and MD1 grounded, this example sets the LXT905 logic and framing to Mode 2 (compatible with Intel* 82596 controllers). Connect a 20 MHz system clock input at CLKI (leave CLKO open). The LI pin externally controls the link test function.

Note: Refer to the Intel® MAC Interface Design Guide for Intel Controllers Application Note (document number 249007) when designing with Intel controllers.

Figure 8. Intel® Controller Application (Mode 2)

intel®
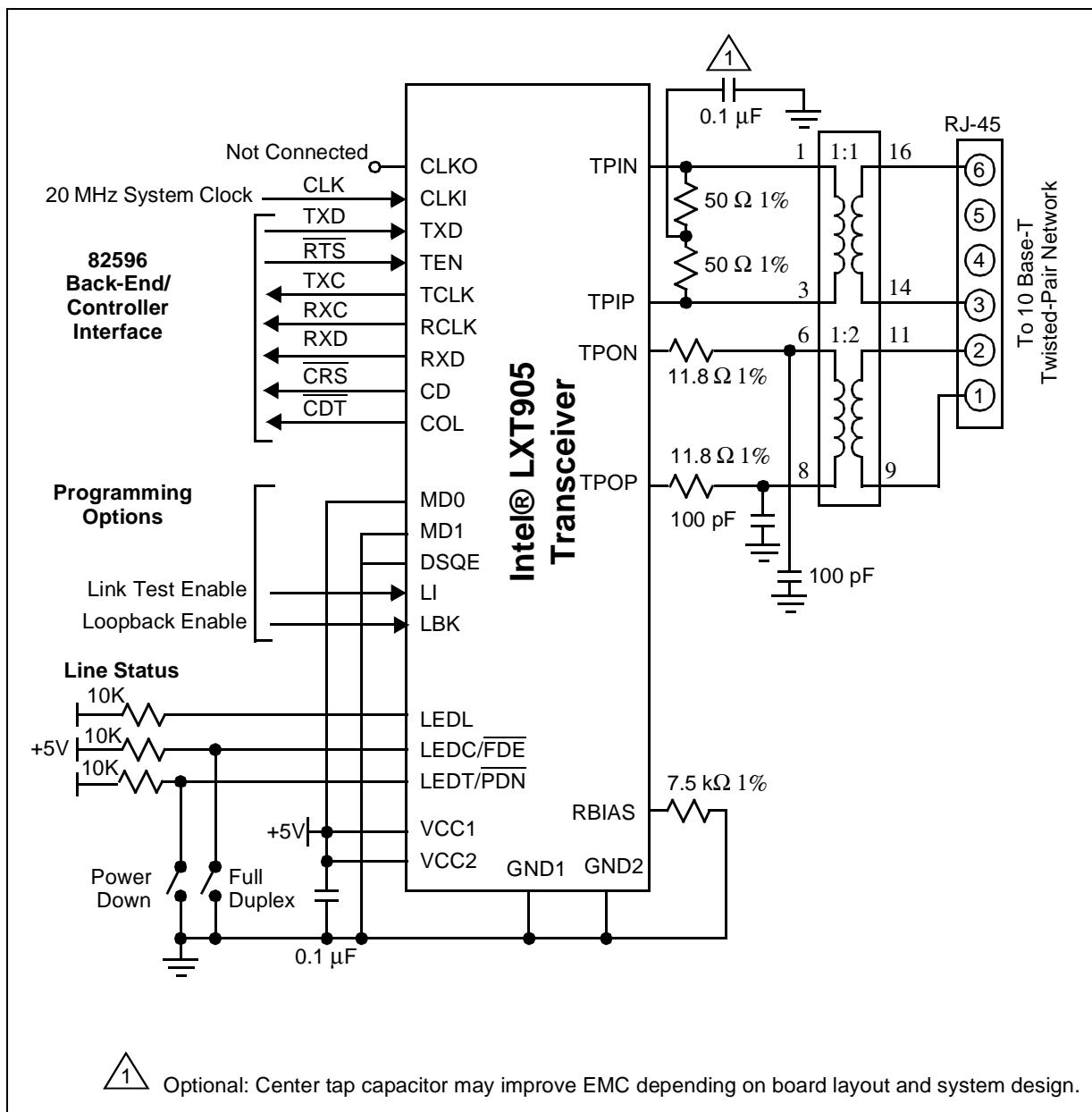
3.3 Dual Network Support - 10BASE-T and Token Ring

Figure 9 on page 21 shows the LXT905 with a Texas Instruments* 380C26 CommProcessor. The 380C26 is compatible with Mode 4 (MD0 and MD1 both high). When you use the LXT905 with the 380C26, you can tie both the LXT905 and a TMS38054* Token Ring transceiver to a single RJ-45, allowing dual network support from a single connector.

Figure 9. Intel® LXT905 PHY/Texas Instruments* 380C26 Interface for Dual 10BASE-T and Token Ring Support (Mode 4)

1. Optional: Center tap capacitor may improve EMC depending on board layout and system design.

2. Additional magnetics and switching logic (not shown) are required to implement the dual network solution.
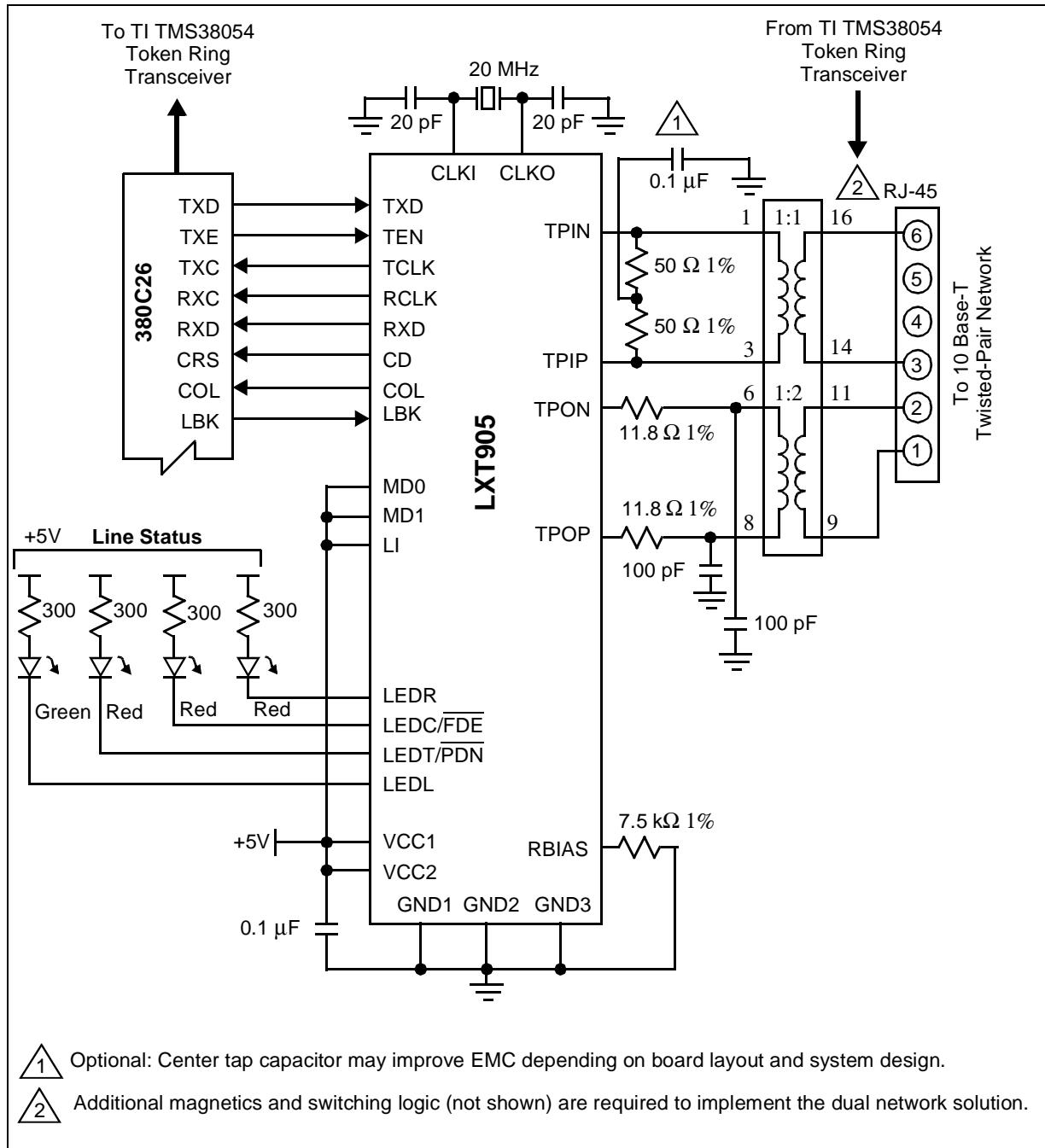
3.4 Simple 10BASE-T Connection

Figure 10 shows a simple 10BASE-T application, using an LXT905 transceiver and a Motorola*
MC68EN360. The MC68EN360 is compatible with Mode 1 (MD0 and MD1 both Low).

Figure 10. Intel® LXT905 PHY/Motorola* MC68EN360 Interface for Full-Duplex 10BASE-T (Mode 1)
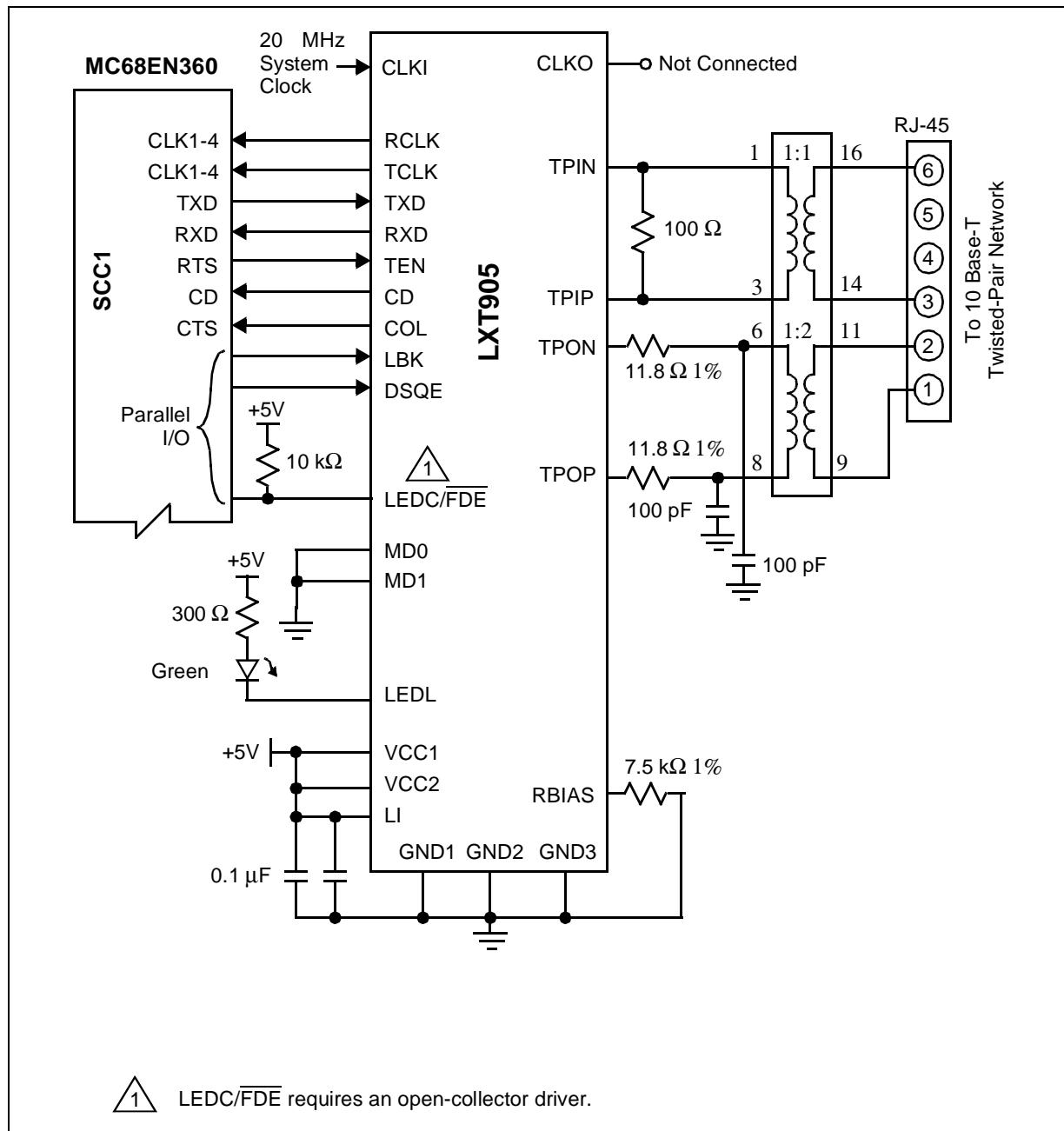
4.0 Test Specifications

Note: The minimum and maximum values in Table 5 through Table 13 on page 26 and Figure 11 on page 27 through Figure 26 on page 34 represent the performance specifications of the LXT905. These specifications are guaranteed by test, except where noted by design. Minimum and maximum values in Table 7 through Table 13 on page 26 apply over the recommended operating conditions specified in Table 6.

For all Quality and Reliability issues (for example, parts packaging and thermal specifications), please send your questions to Intel at the following e-mail address: qr.requests@intel.com.

Table 5. Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage	V_{CC}	-0.3	+6	V
Storage temperature	T_{ST}	-65	+150	ºC

Caution: Exceeding these values can cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.

Table 6. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Recommended supply voltage[1]	V_{CC}	3.135	5.0	5.25	V
Recommended operating temperature (Commercial)	T_{OP}	0	–	+70	ºC
Recommended operating temperature (Extended)	T_{OP}	-40	–	+85	ºC

1. Voltage is with respect to ground, unless otherwise specified.

Table 7. I/O Electrical Characteristics (Sheet 1 of 2)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Input low voltage[2]		V_{IL}	–	–	0.8	V	
Input high voltage[2]		V_{IH}	2.0	–	–	V	
Output low voltage		V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
		V_{OL}	–	–	10	%V_{CC}	I_{OL} < 10 μA
Output low voltage (Open drain LED driver)		V_{OLL}	–	–	0.7	%V_{CC}	I_{OLL} = 10 mA
Output high voltage		V_{OH}	2.4	–	–	V	I_{OH} = 40 μA
		V_{OH}	90	–	–	%V_{CC}	I_{OH} < 10 μA
Output rise time	CMOS	–	–	3	15	ns	C_{LOAD} = 20 pF
TCLK & RCLK	TTL	–	–	2	15	ns	

1. Typical values are at 25 °C, are for design aid only, are not guaranteed, and are not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V. This applies to all inputs except TPIP and TPIN.

Table 7. I/O Electrical Characteristics (Sheet 2 of 2)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Output fall time TCLK & RCLK	CMOS	–	–	3	15	ns	C$_{LOAD}$= 20 pF
	TTL	–	–	2	15	ns	
CLKI rise time (externally driven)		–	–	–	10	ns	
CLKI duty cycle (externally driven)		–	–	50/50	40/60	%	
Supply current	Normal Mode	ICC	–	40	80	mA	Idle Mode
		ICC	–	70	100	mA	Transmitting on TP
	Power Down Mode	ICC	–	0.01	1	µA	

1. Typical values are at 25 °C, are for design aid only, are not guaranteed, and are not subject to production testing.
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V. This applies to all inputs except TPIP and TPIN.

Table 8. TP Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	Z$_{OUT}$	–	5	–	Ω	–
Transmit timing jitter addition[2]	–	–	±6.4	±10	ns	0 line length for internal MAU
Transmit timing jitter that the MAU and PLS sections add[2, 3]	–	–	±3.5	±5.5	ns	After line model specified in *IEEE 802.3 for 10BASE-T internal MAU*
Receive input impedance	Z$_{IN}$	–	24	–	kΩ	Between TPIP/TPIN
Differential squelch threshold	V$_{DS}$	300	420	585	mV	5 MHz square wave input

1. Typical values are at 25 °C, are for design aid only, are not guaranteed, and are not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. *IEEE 802.3* specifies maximum jitter additions at 0.5 ns from the encoder, and 3.5 ns from the MAU.

Table 9. Switching Characteristics

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Jabber Timing	Maximum transmit time	–	20	–	150	ms
	Unjab time	–	250	–	750	ms
Link Integrity Timing	Time link loss receive	–	50	–	150	ms
	Link min receive	–	2	–	7	ms
	Link max receive	–	50	–	150	ms
	Link transmit period	–	8	10	24	ms

1. Typical values are at 25 °C, are for design aid only, are not guaranteed, and are not subject to production testing.

Table 10. RCLK/Start-of-Frame Timing

Parameter		Symbol	Min	Typ[1]	Max	Units
Decoder acquisition time		tDATA	–	1300	1500	ns
CD turn-on delay		tCD	–	400	550	ns
Receive data setup from RCLK	Mode 1	tRDS	60	70	–	ns
	Modes 2, 3, and 4	tRDS	30	45	–	ns
Receive data hold from RCLK	Mode 1	tRDH	10	20	–	ns
	Modes 2, 3, and 4	tRDH	30	45	–	ns
RCLK shut off delay from CD assert (Mode 3)		tsws	–	±100	–	ns

1. Typical values are at 25 °C, are for design aid only, are not guaranteed, and are not subject to production testing.

Table 11. RCLK/End-of-Frame Timing

Parameter	Type	Sym	Mode 1	Mode 2	Mode 3	Mode 4	Units
RCLK after CD off	Min	tRC	5	1	–	5	BT
Rcv data through-put delay	Max	tRD	400	375	375	375	ns
CD turn-off delay [2]	Max	tCDOFF	500	475	475	475	ns
Receive block out after TEN off [3]	Typical[1]	tIFG	5	50	–	–	BT
RCLK switching delay after CD off	Typical[1]	tswe	–	–	120 (±80)	–	ns

1. Typical figures are at 25 °C, are for design aid only are not guaranteed, and are not subject to production testing.
2. CD Turnoff delay, measured from the middle of the last bit: timing specification. The value of the last bit does not affect this value.
3. Disables blocking of Carrier Detect during full-duplex operation.

Table 12. Transmit Timing

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
TEN setup from TCLK	tEHCH	22	–	–	ns
TXD setup from TCLK	tDSCH	22	–	–	ns
TEN hold after TCLK	tCHEL	5	–	–	ns
TXD hold after TCLK	tCHDU	5	–	–	ns
Transmit start-up delay	tSTUD	–	350	450	ns
Transmit through-put delay	tTPD	–	338	350	ns

1. Typical values are at 25 °C, are for design aid only, are not guaranteed, and are not subject to production testing.

Table 13. Miscellaneous Timing

Parameter	Symbol	Minimum	Typical[1]	Maximum	Units
COL (SQE) Delay after TEN off [2]	t_{SQED}	0.65	–	1.6	μs
COL (SQE) Pulse Duration[2]	t_{SQEP}	500	–	1500	ns
Power Down recovery time	t_{PDR}	–	25	–	ms

1. Typical values are at 25 °C, are for design aid only, are not guaranteed, and are not subject to production testing.
2. When SQE is enabled (DSQE is Low).

4.1 Timing Diagrams for Mode 1 (MD1 = Low, MD0 = Low)

Timing diagrams for Mode 1 include Figure 11 through Figure 14.

**Figure 11. Mode 1 RCLK/Start-of-Frame Timing**
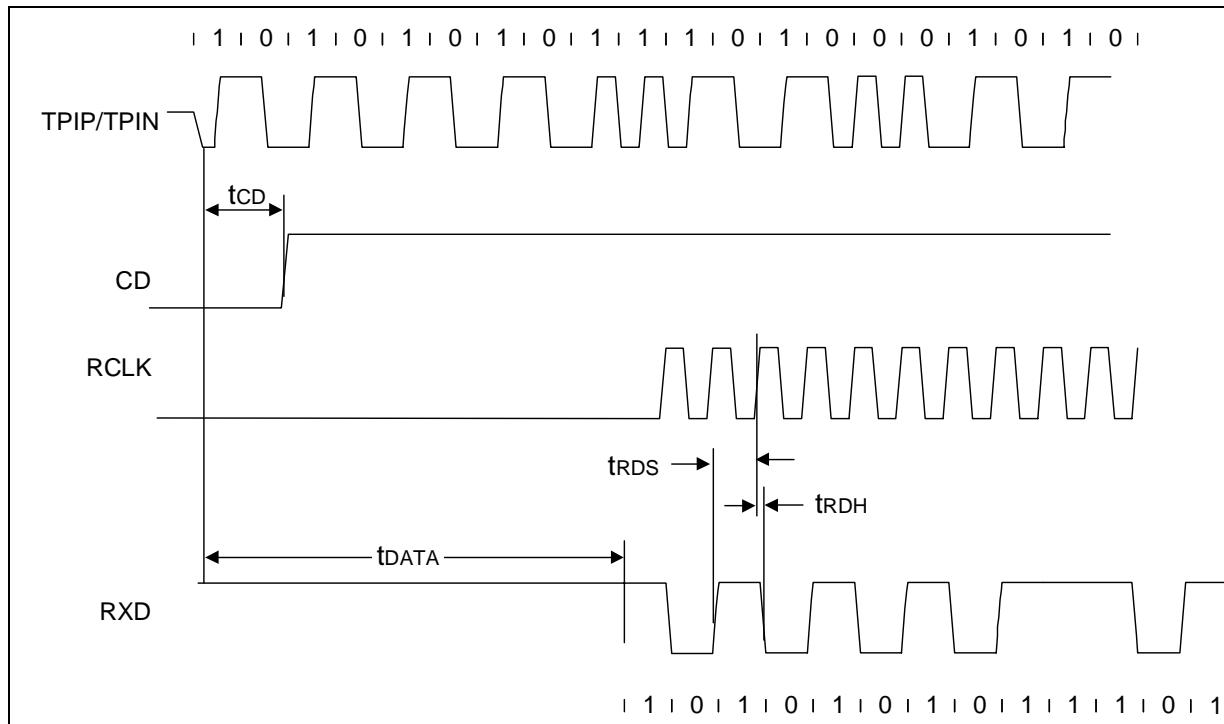
Figure 12. Mode 1 RCLK/End-of-Frame Timing
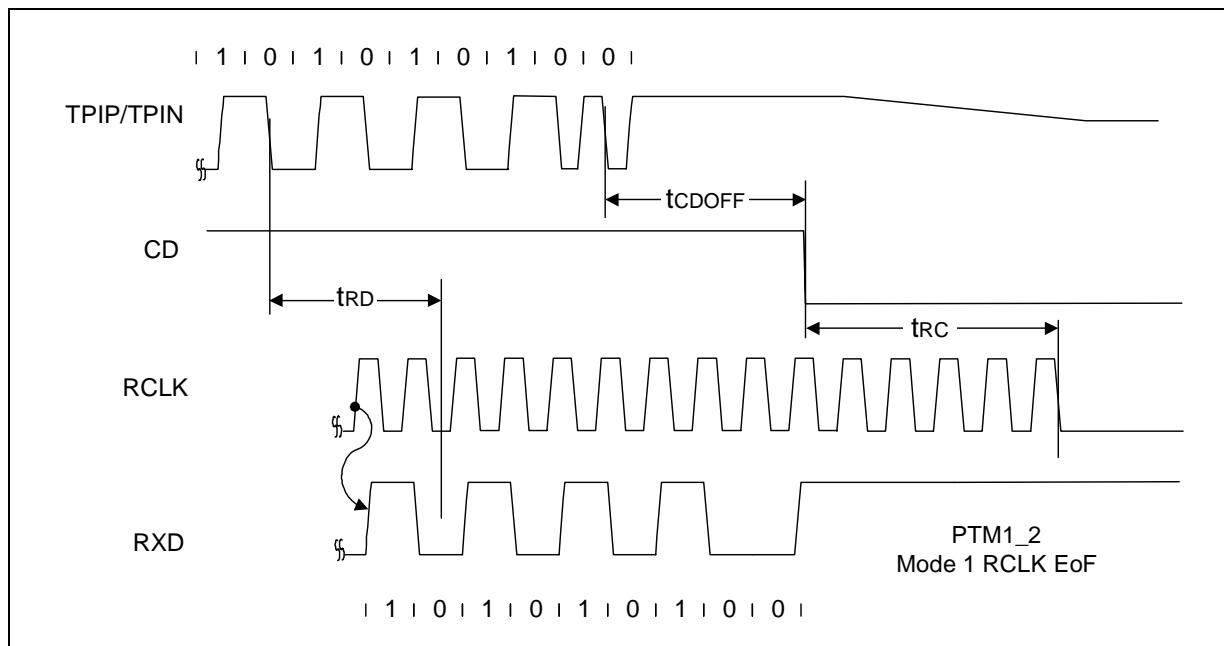
**Figure 13. Mode 1 Transmit Timing**
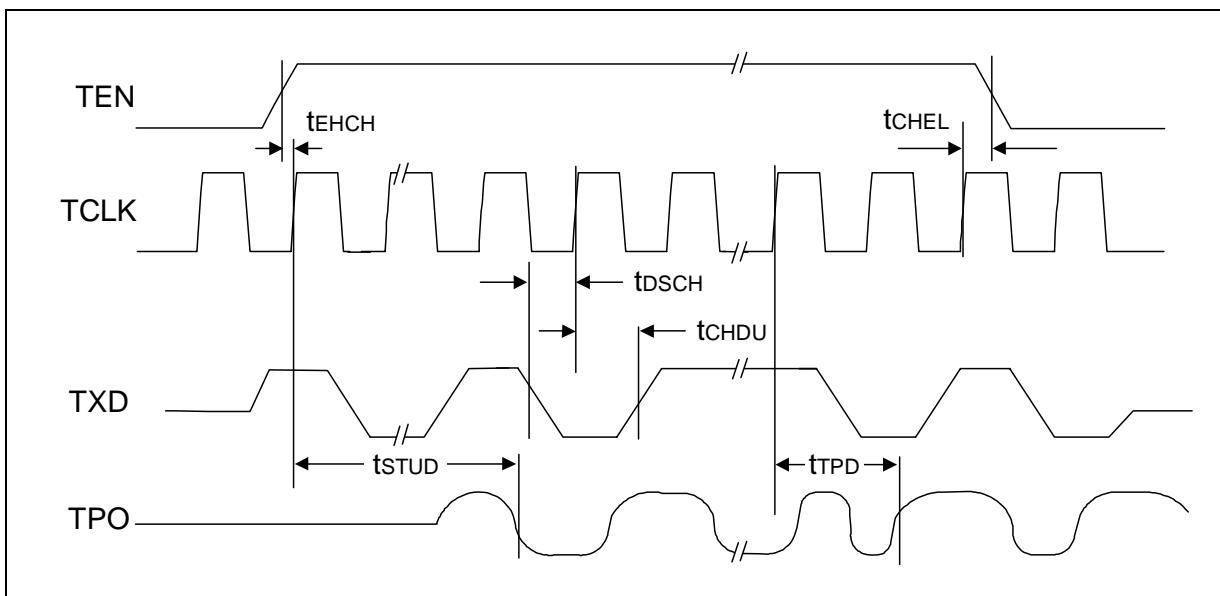
Figure 14. Mode 1 COL Output Timing
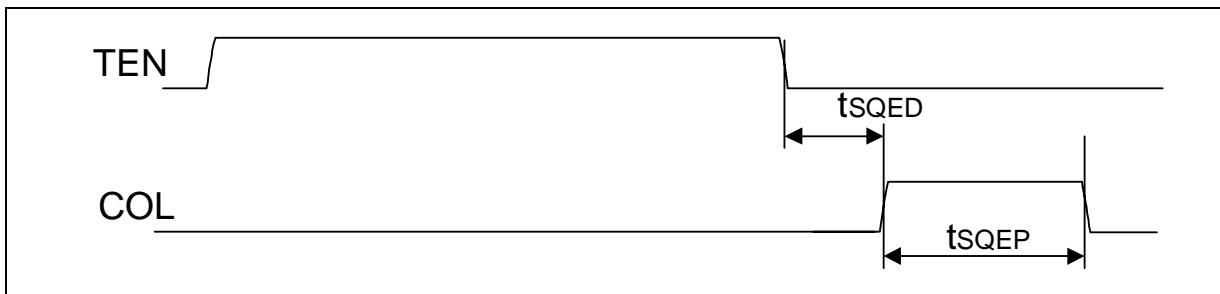
4.2 Timing Diagrams for Mode 2 (MD1 = Low, MD0 = High)

Timing diagrams for Mode 2 include Figure 15 through Figure 18.

Figure 15. Mode 2 RCLK/Start-of-Frame

NOTE:
1. RXD changes at the rising edge of RCLK. Mode 2 samples the controller at the falling edge.
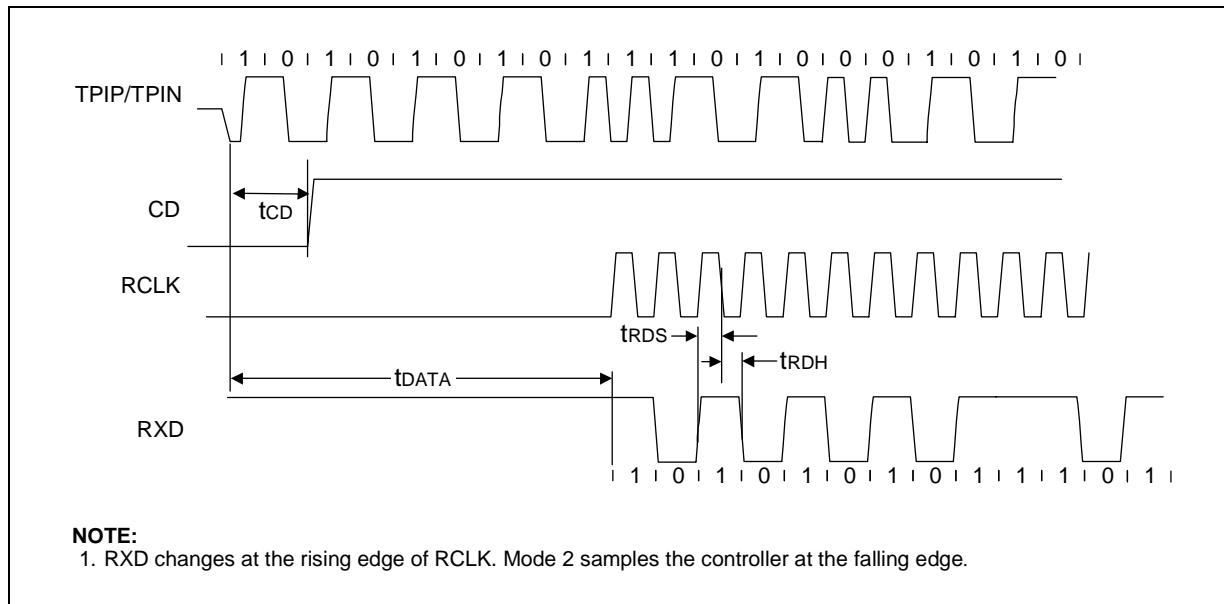
Figure 16. Mode 2 RCLK/End-of-Frame Timing

NOTE:
1. RXD changes at the rising edge of RCLK. Mode 2 samples the controller at the falling edge.
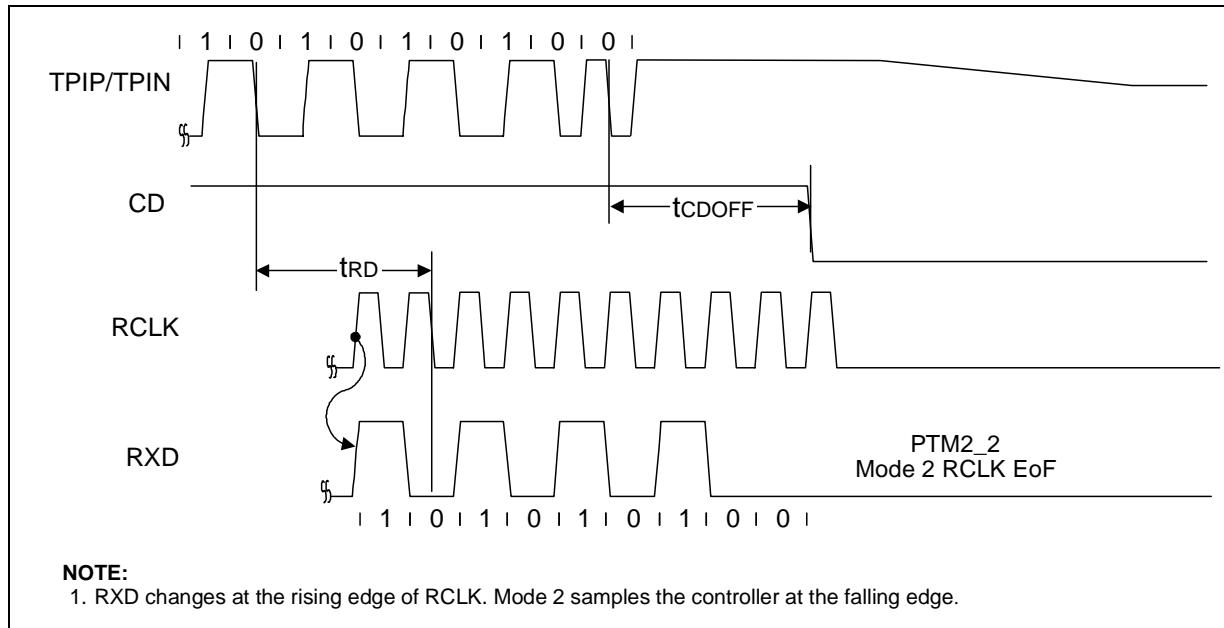
Figure 17. Mode 2 Transmit Timing
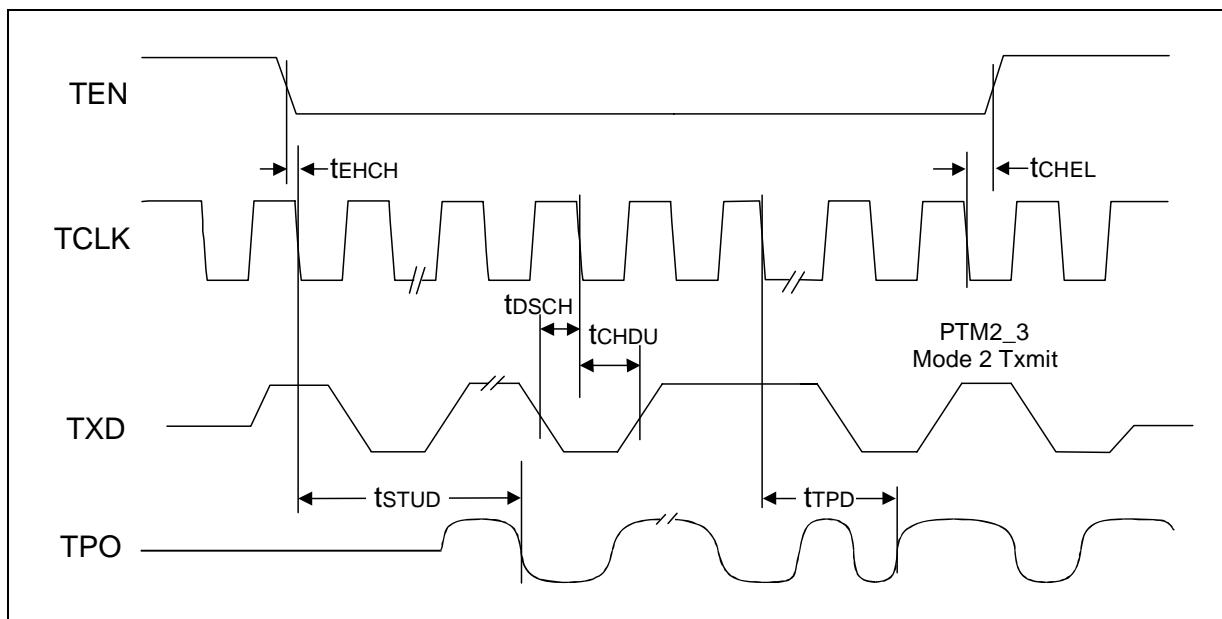
Figure 18. Mode 2 COL Output Timing

NOTE:
 1. CD output is disabled for a maximum of 55 bit times after TEN turns off.
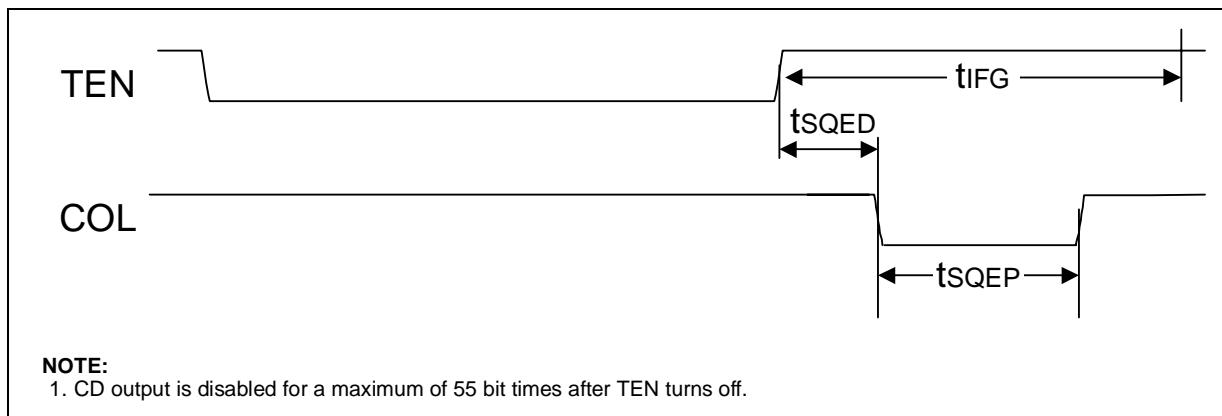
4.3 Timing Diagrams for Mode 3 (MD1 = High, MD0 = Low)

Timing diagrams for Mode 3 include Figure 19 through Figure 22.

Figure 19. Mode 3 RCLK/Start-of-Frame Timing

NOTE:
1. RXD changes at the rising edge of RCLK. Mode 3 samples the controller at the falling edge.
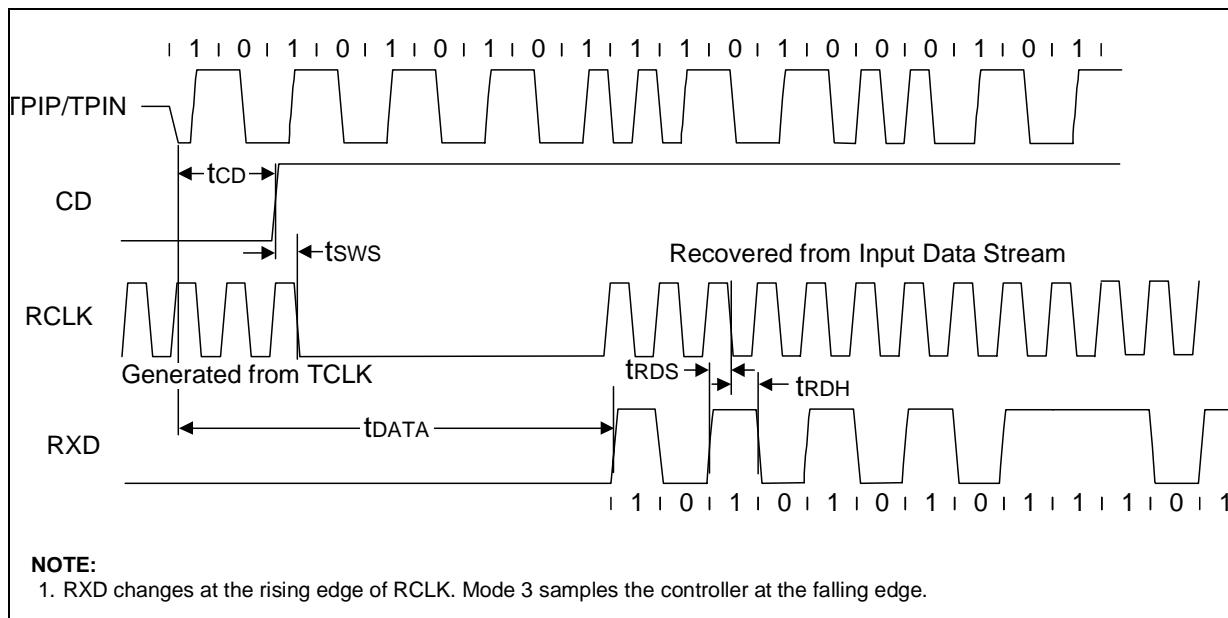
Figure 20. Mode 3 RCLK/End-of-Frame Timing

NOTE:
1. RSD changes at the rising edge of RCLK. Mode 3 samples the controller at the falling edge.
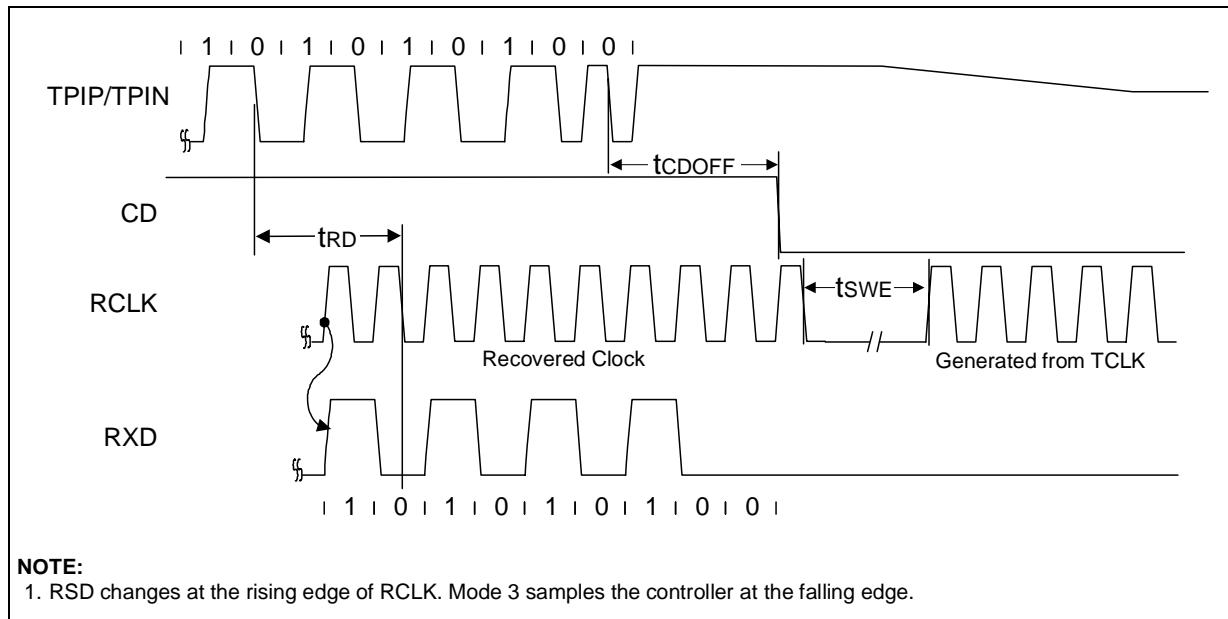
**Figure 21. Mode 3 Transmit Timing**
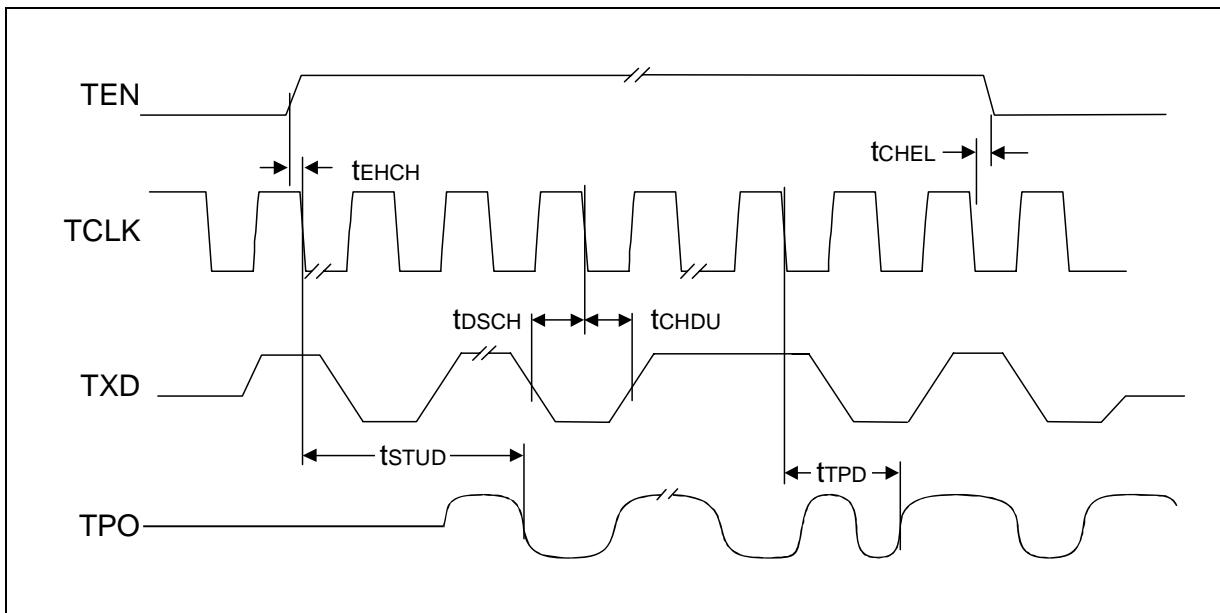
Figure 22. Mode 3 COL Output Timing
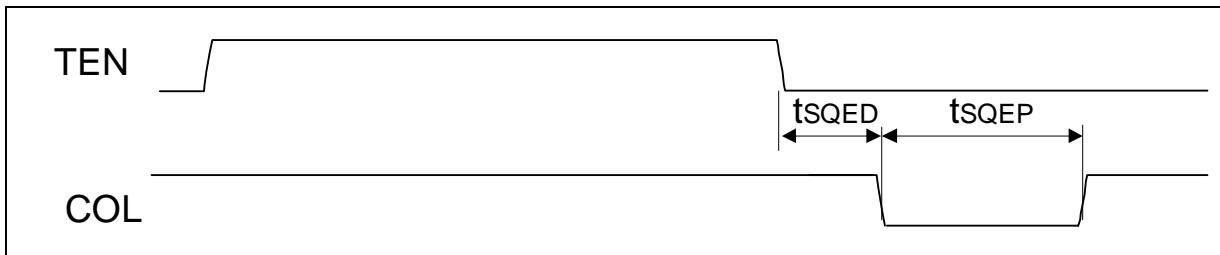
4.4 Timing Diagrams for Mode 4 (MD1 = High, MD0 = High)

Timing diagrams for Mode 4 include Figure 23 through Figure 26.

Figure 23. Mode 4 RCLK/Start-of-Frame Timing

NOTE:
1. RXD changes at the falling edge of RCLK. Mode 4 samples the controller at the rising edge.
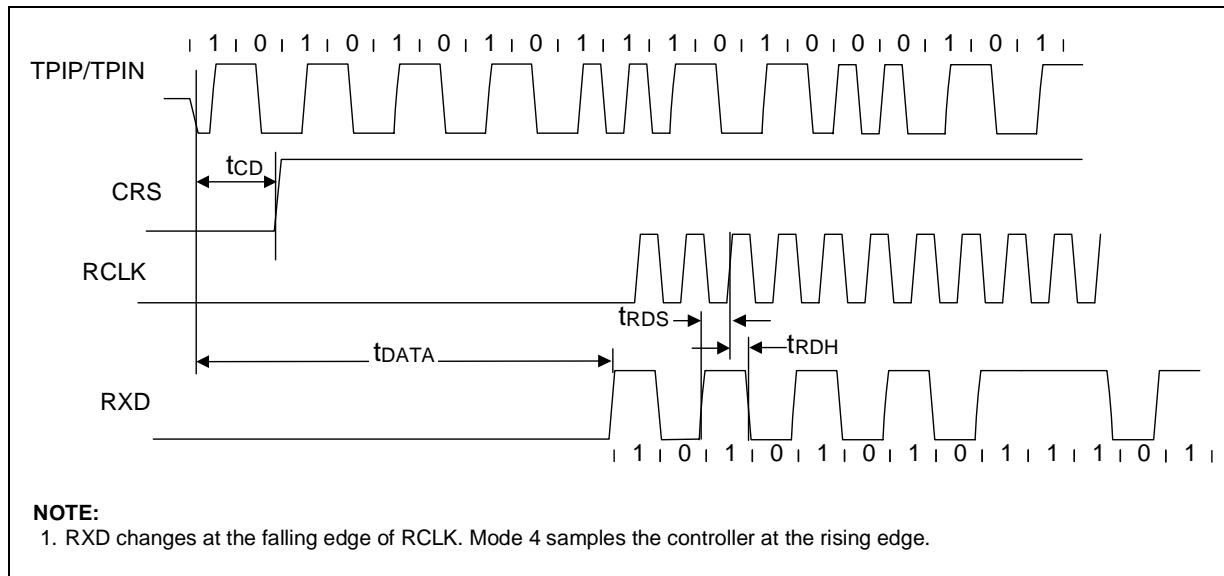
Figure 24. Mode 4 RCLK/End-of-Frame Timing

NOTE:
1. RXD changes at the falling edge of RCLK. Mode 4 samples the controller at the rising edge.
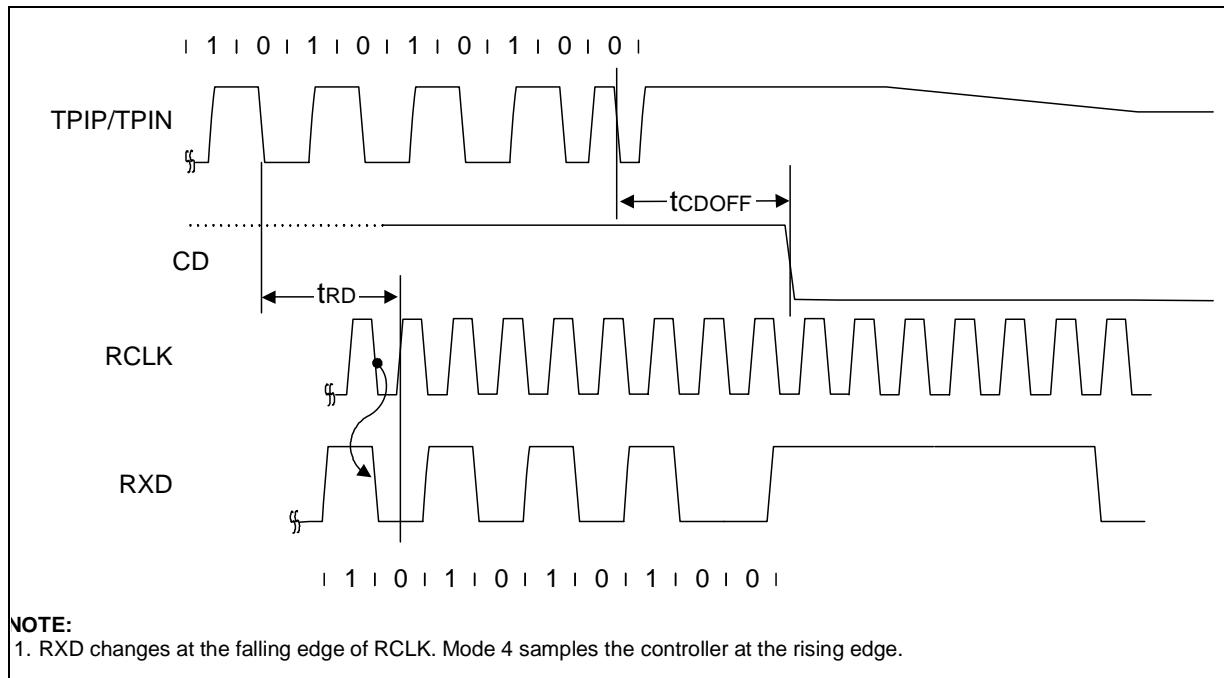
Figure 25. Mode 4 Transmit Timing
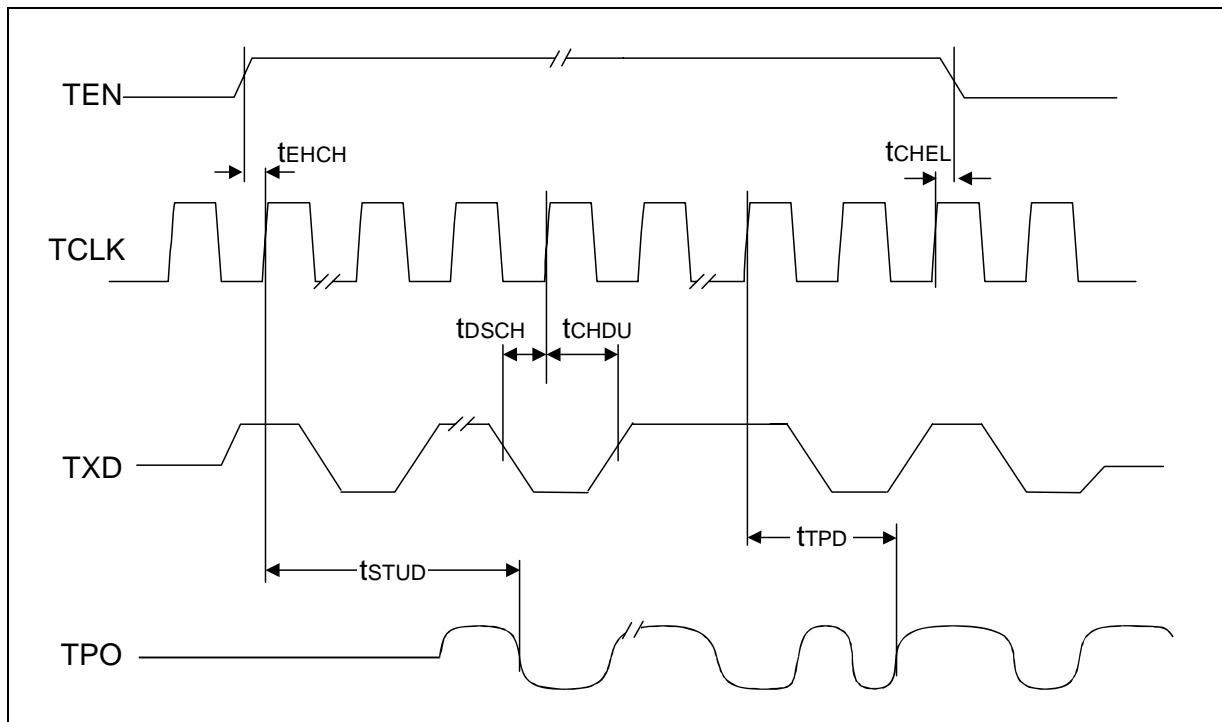
Figure 26. Mode 4 COL Output Timing
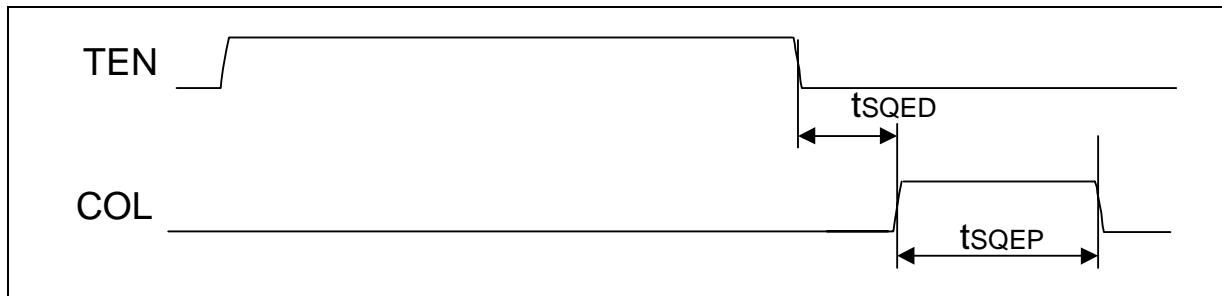
5.0 Mechanical Specifications

Figure 27. Intel® LXT905PC PHY Package Specifications

28-Pin PLCC

- Part Number LXT905PC (Commercial Temperature Range)
- Part Number LXT905PE (Extended Temperature Range)
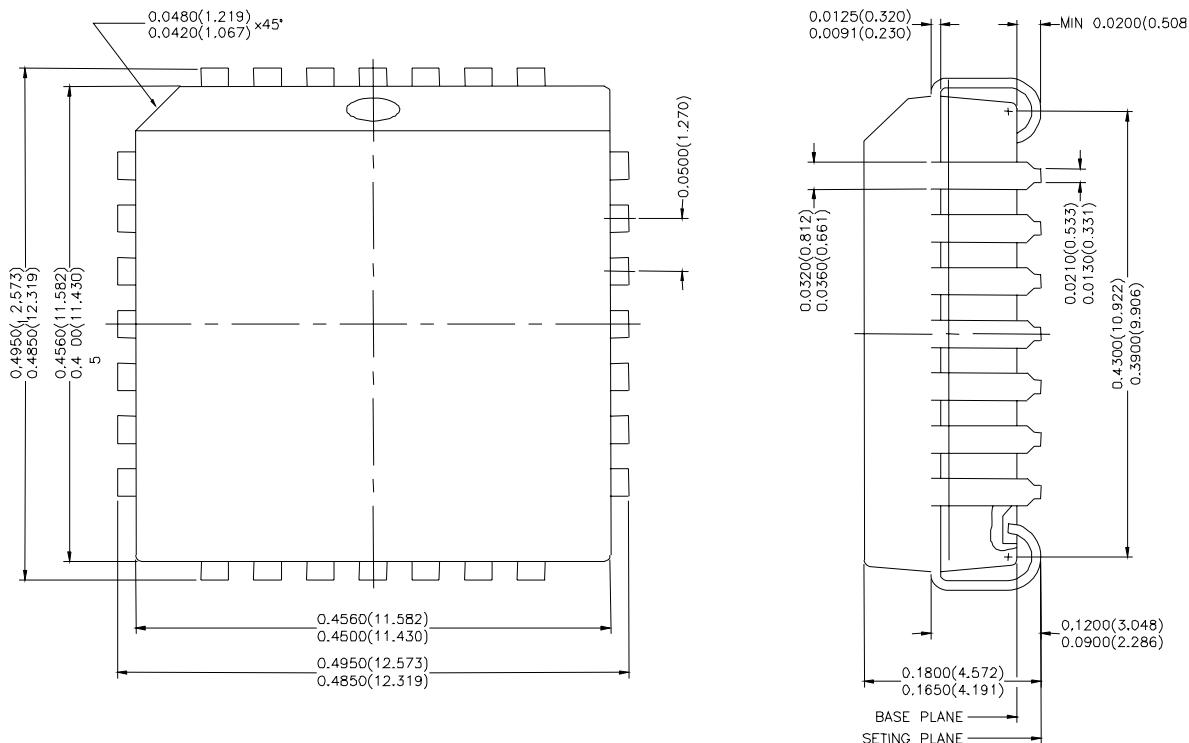
Table 14. Plastic Leaded Chip Carrier

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A_1	0.090	0.120	2.286	3.048
A_2	0.062	0.083	1.575	2.108
B	0.050	–	1.270	–
C	0.026	0.032	0.660	0.813
D	0.485	0.495	12.319	12.573

Figure 28. Intel® LXT905LC PHY Package Specifications

32-Pin LQFP

- Part Number LXT905LC (Commercial Temperature Range)
- Part Number LXT905LE (Extended Temperature Range)

All Dimensions in millimeters
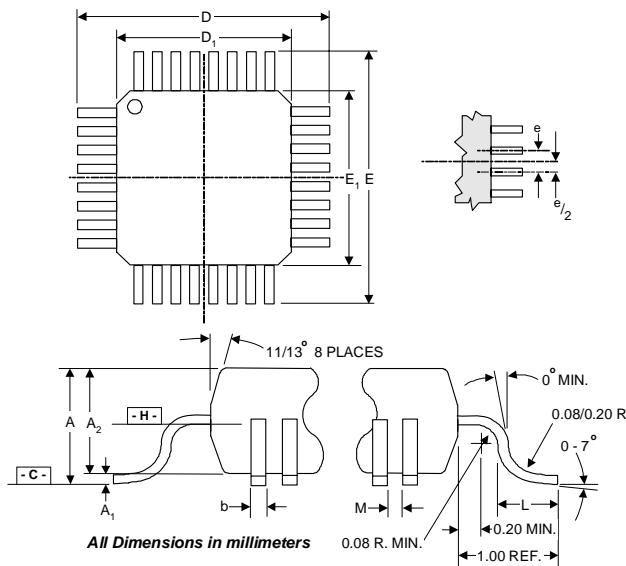
Table 15. Quad Flat Package

Dim.	All Dimensions in millimeters			
	Min.	Typ.	Max.	Notes
A	---	---	1.60	
A$_1$	0.05	0.10	0.15	
A$_2$	1.35	1.40	1.4	
D	9.00 BSC.			5
D$_1$	7.00 BSC.			6, 7, 8
E	9.00 BSC			5
E$_1$	7.00 BSC			6, 7, 8
L	0.45	0.60	0.75	
M	0.15	---	---	
b	0.30	0.37	0.45	9
e	0.80 BSC.			

NOTES:
1. All dimensions are in millimeters.
2. This package conforms to JEDEC publication 95 registration MO-136, variation BC.
3. Datum plane -H- located at mold parting line and is coincident with leads where leads exit plastic body at bottom of parting line.
4. Measured at seating plane -C-.
5. Measured at datum plane -H-.
6. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm.
7. Package top dimensions are smaller than bottom dimensions. Top of package will not overhang bottom of package.
8. Dimension b does not include dambar protrusion. Allowable dambar protrusion is no more than 0.08 mm.

6.0 Top-Label Device Marking

Figure 29 through Figure 32 illustrate the LXT905 Transceiver top label markings. Figure 29 and Figure 31 are the standard top labels; Figure 30 and Figure 32 are the RoHS-compliant top labels.

Note: In contrast to the Pb-Free (RoHS-compliant) package, the non-RoHS-compliant package does not have the "e3" symbol in the last line of the package label.

Figure 29. Top-Label Device Marking – Intel® DJLXT905LC.C2 Transceiver
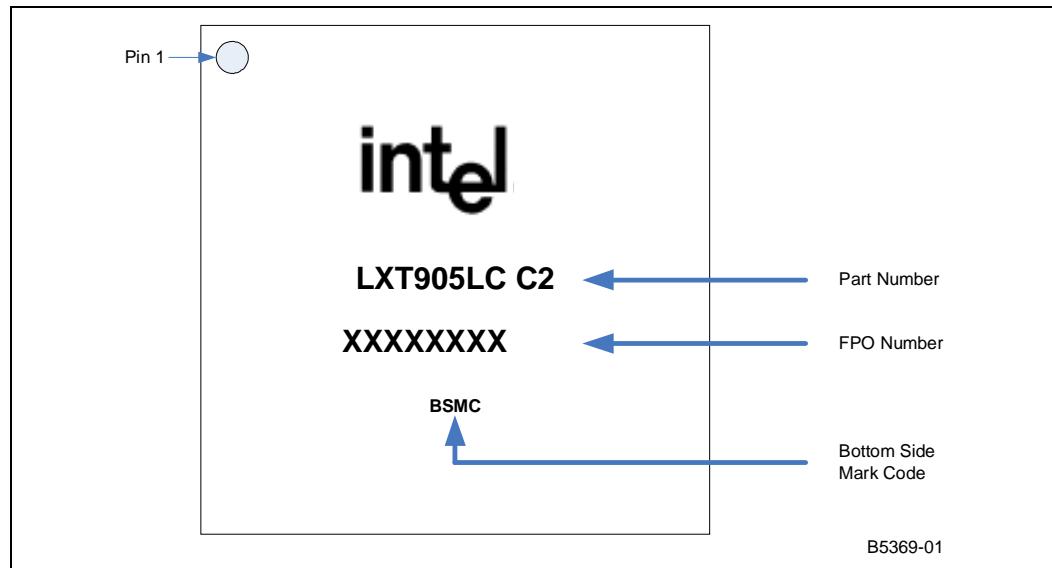
Figure 30. Top-Label Device Marking – Intel® WJLXT905LC.C2 Transceiver
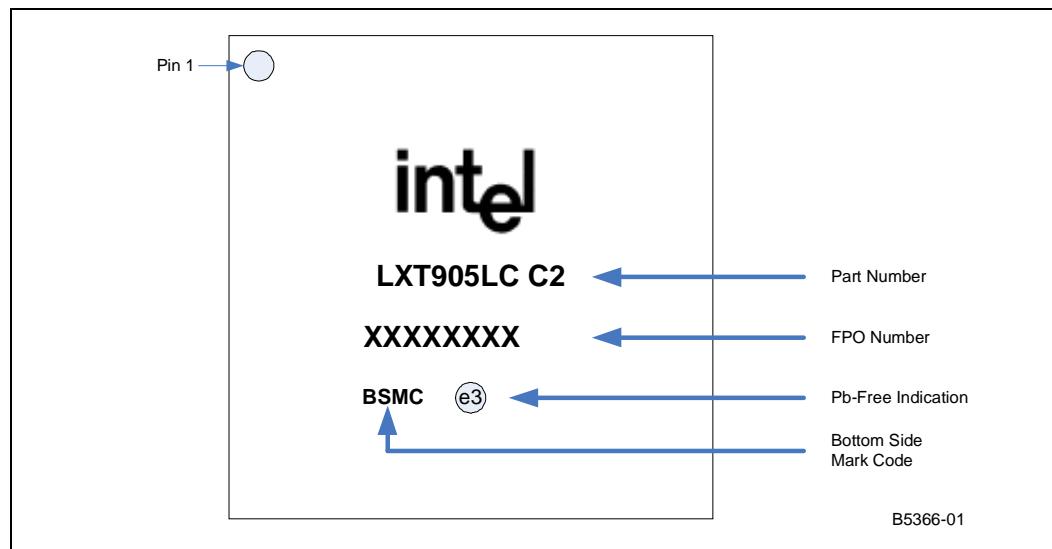
Figure 31. Top-Label Device Marking – Intel® NLXT905PC.C2 Transceiver

Pin 1

intel ®

LXT905PC C2 ← Part Number

XXXXXXXX ← FPO Number

BSMC ← Bottom Side Mark Code

B5370-01
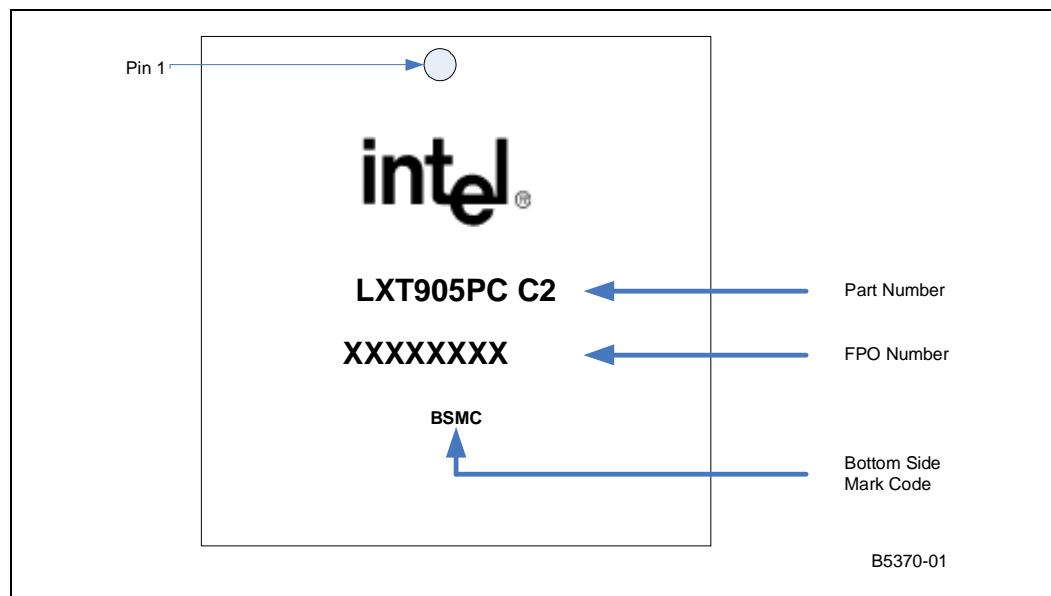
Figure 32. Top-Label Device Marking – Intel® EELXT905E.C2 Transceiver

Pin 1

intel ®

EELXT905E C2 ← Part Number

XXXXXXXX ← FPO Number

BSMC (e3) ← Pb-Free Indication

← Bottom Side Mark Code

B5371-01
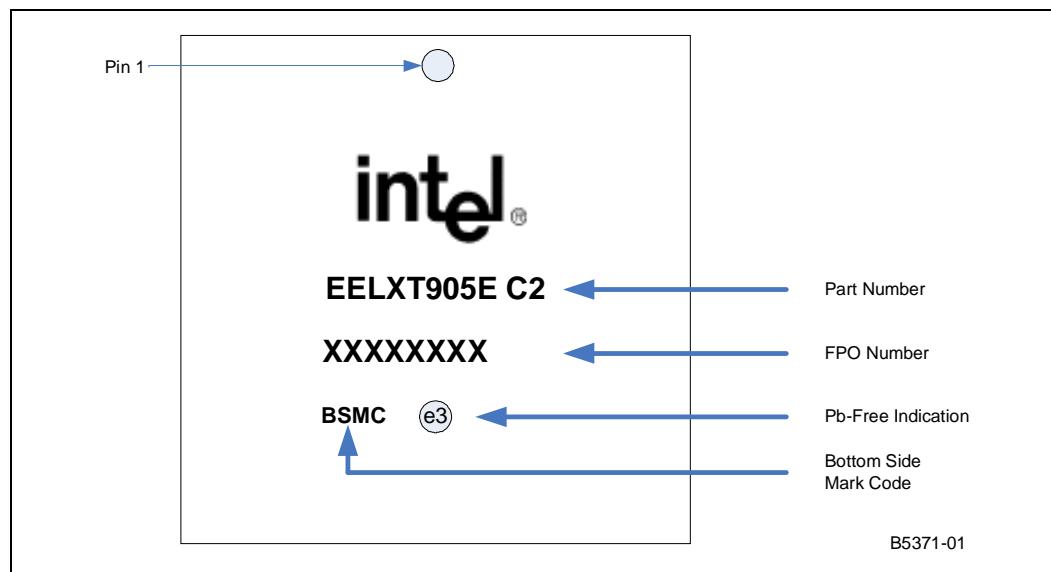
7.0 Ordering Information

Table 16 lists the LXT905 Transceiver product ordering information.

Table 16. Product Information

Number	Revision	Package Type	Pin Count	RoHS Compliant
DJLXT905LC.C2	C2	TQFP	32	No
WJLXT905LC.C2	C2	TQFP	32	Yes
DJLXT905LE.C2	C2	TQFP	32	No
WJLXT905LE.C2	C2	TQFP	32	Yes
NLXT905PC.C2	C2	PLCC	28	No
EELXT905PC.C2	C2	PLCC	28	Yes
NLXT905PE.C2	C2	PLCC	28	No
EELXT905PE.C2	C2	PLCC	28	Yes

Figure 33 shows an order matrix with sample information for the LXT905 Transceiver.

Figure 33. Ordering Information - Sample

DJ	LXT	905	L	C	C2

Product Revision
xn = 2 Alphanumeric characters

Temperature Range
A = Ambient (0 – 55^0 C)
C = Commercial (0 – 70^0 C)
E = Extended (-40 – 85^0 C)

Internal Package Designator
L = LQFP
P = PLCC
N = DIP
Q = PQFP
H = QFP
T = TQFP
B = BGA
C = CBGA
E = TBGA
K = HSBGA (BGA with heat slug

Product Code
xxxxx = 3-5 Digit alphanumeric

IXA Product Prefix
LXT = PHY layer device
IXE = Switching engine
IXF = Formatting device (MAC/Framer)
IXP = Network processor

Intel Package Designator

Pb-Free	Package	Leaded
WJ	LQFP	DJ
BJ	LQFP	FA
JA	TQFP	FA
EL	TPBGA	FL
EL	PBGA	FL
PR	BGA	FW
PR	PBGA	FW
LU	PBGA	GD
EW	BGA	GW
WB	HQFP	HB
WD	PQFP	HD
WF	CBGA	HF
WG	QFN	HG
JP	FCBGA	HL
RU	BGA	HZ
QU	PQFP	KU
UB	QFN	LB
EE	PLCC	NL
EE	PLCC	NS
EP	SSOP	PA
UC	PDIP	PD
PC	MMAP	RC
EG	PQFP	SL
EG	HQFP	SL
EG	PQFP	SL
SC	TPBGA	TL

B5361-01