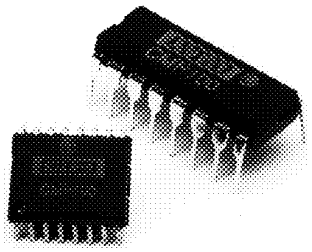
BURR-BROWN®

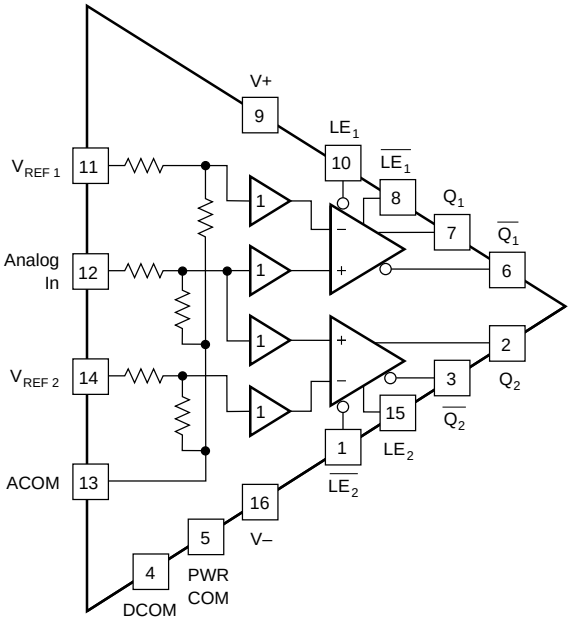


CMP100

HIGH-SPEED WINDOW COMPARATOR ATE PIN RECEIVER

FEATURES

- **PROPAGATION DELAY: 5ns max, 100mV Overdrive**
- **COMMON MODE INPUT RANGE: ±12V**
- **INPUT IMPEDANCE: 120kΩ || 2pF**
- **OUTPUTS: Latchable, 10k ECL Compatible**
- **COMPLETE: No External Parts Required**
- **TEMPERATURE RANGE: –25°C to +85°C**
- **PACKAGES: 16-Pin Plastic DIP, 16-Lead Plastic SOIC**



APPLICATIONS

- **ATE PIN RECEIVER**
- **WINDOW COMPARATOR**
- **THRESHOLD DETECTOR**

DESCRIPTION

CMP100 is a high-speed dual comparator designed for use as an automatic test system pin receiver. It is also useful in a wide variety of analog threshold detector and window comparator applications.

CMP100 has two reference inputs and one analog input which is common to both comparators. All inputs are attenuated by a voltage divider to provide high common mode voltage operation. The analog input attenuator is R-C tuned to optimize operation with high-speed input waveforms. The reference input attenuators are not R-C tuned. Each attenuator network is followed by a buffer amplifier ahead of the comparator circuits.

Complementary ECL output stages are capable of driving 50Ω terminated transmission lines to a –2V pull-down voltage. In addition, latch-enable inputs are provided for each comparator, allowing operation as a sampling comparator.

CMP100 is available as an industrial temperature range device, –25°C to +85°C, and is packaged in a 16-pin plastic DIP and in a 16-lead plastic SOIC.

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PDS-1075A Printed in U.S.A. March, 1992

SPECIFICATIONS

ELECTRICAL

T_A = 25°C and at rated supplies: V+ = +5V, V– = –5.2V unless otherwise noted.

PARAMETER	CMP100AP, AU MIN	CMP100AP, AU TYP	CMP100AP, AU MAX	UNITS
ANALOG INPUTS				
Differential Input Voltage Range		24		V
Common Mode Voltage Range		±12		V
Resistance				
Reference Inputs: $V_{REF\ 1}$, $V_{REF\ 2}$	45	60	75	kΩ
Analog Input	90	120	150	kΩ
Capacitance, All Inputs		2		pF
TRANSFER CHARACTERISTICS				
ACCURACY				
Input Offset Voltage, V_{OS} (1)		10	20	mV
Common Mode Error			10	mV/V
Voltage Offset Drift		100	250	µV/°C
Power Supply Sensitivity of Offset: $\Delta V_{OS}/\Delta V+$			±10	µV/V
$\Delta V_{OS}/\Delta V-$			±10	µV/V
RESPONSE TIME				
Propagation Delay, t_{PD} (2, 3)				
100mV Overdrive, Latch Disabled		3.6	5	ns
DIGITAL SIGNALS (4) (Over Specification Temperature Range)				
Inputs (Latch Controls)				
Logic Levels: V_{IH}	–1.1			V
V_{IL}			–1.5	V
I_{IH} (V_I = –1.1V)			50	µA
I_{IL} (V_I = –1.5V)			5	µA
Outputs (Balanced)				
Logic Levels: V_{OL} (50Ω Load to –2V)			–1.5	V
V_{OH} (50Ω Load to –2V)	–1.1			V
POWER SUPPLY REQUIREMENTS				
Supply Voltage				
V+	+4.75	+5	+5.25	VDC
V–	–5.45	–5.2	–4.95	VDC
Supply Current (5)				
V+		+30	+40	mA
V–		–40	–50	mA
Power Dissipation (6)		360	460	mW
TEMPERATURE RANGE				
Specification	–25		+85	°C
Storage	–65		+150	°C

NOTES: (1) Defined as half the magnitude between low-to-high and high-to-low transition input voltages. (2) See section on "Measuring CMP100 Performance." (3) See "Discussion of Specifications" for exact conditions. (4) 10k ECL compatible. (5) Maximum supply current is specified at typical supply voltages. (6) Maximum Power Dissipation is calculated with typical supply voltages and maximum currents. Note that dissipation in the output transistors from driving 50Ω ECL loads will increase the total power dissipation by about 50mW.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common and Power Common ..... +6V
V– to Digital Common and Power Common ..... –6V
(V+) – (V–) 12V
Digital Inputs to Digital Common
  Differential ..... ±4V
  Common Mode ..... V– to V+
Differential Analog Input Voltage ..... ±25V
Package Power Dissipation 750mW
Storage Temperature ..... –60°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

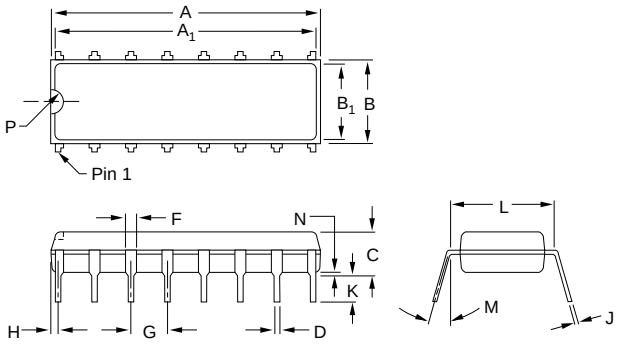
Stresses exceeding those listed above may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN DEFINITIONS

PIN	NAME	DESCRIPTION
1, 15	$\overline{LE2}$, LE2	LATCH or UNLATCH comparator 1 outputs
2, 3	Q2, $\overline{Q2}$	ECL outputs of comparator 2
4	DCOM	Return for comparator circuits
5	PWRCOM	Return for ECL output transistor currents
6, 7	$\overline{Q1}$, Q1	ECL outputs of comparator 1
8, 10	$\overline{LE1}$, LE1	LATCH or UNLATCH comparator 2 outputs
9	V+	Positive Supply Voltage, +5V
11	$V_{REF\ 1}$	Reference Voltage for comparator 1
12	Analog In	Analog Signal input
13	ACOM	Return for Analog In, $V_{REF\ 1}$, $V_{REF\ 2}$
14	$V_{REF\ 2}$	Reference voltage for comparator 2
16	V–	Negative Supply Voltage: (ECL Supply, –5.2V)

MECHANICAL

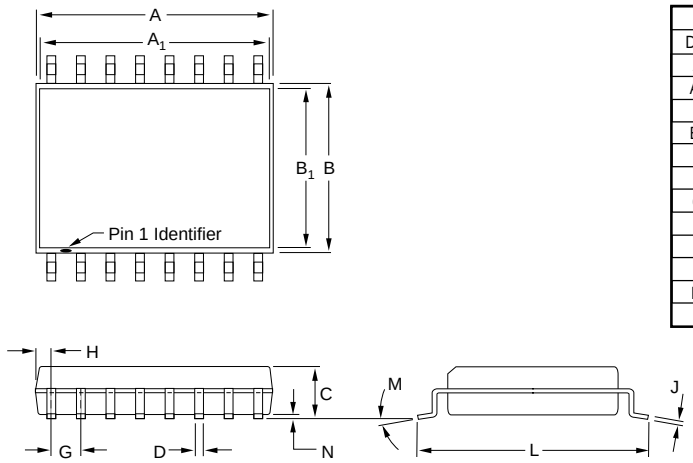
P Package — 16-Pin Plastic DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

U Package — 16-Pin SOIC



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.400	.416	10.16	10.57
A1	.388	.412	9.86	10.46
B	.286	.302	7.26	7.67
B1	.268	.286	6.81	7.26
C	.093	.109	2.36	2.77
D	.015	.020	0.38	0.51
G	.050 BASIC		1.27 BASIC	
H	.022	.038	0.56	0.97
J	.008	.012	0.20	0.30
L	.391	.421	9.93	10.69
M	5° TYP		5° TYP	
N	.000	.012	0.00	0.30

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

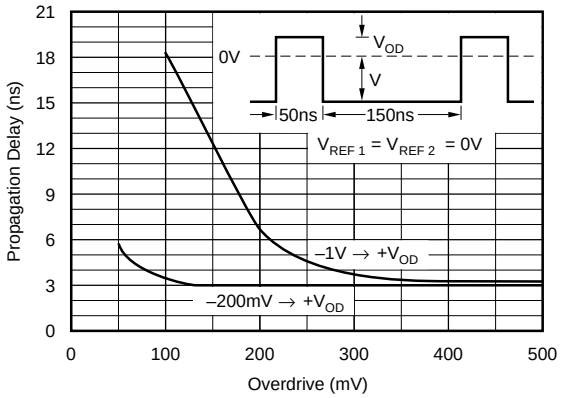
ORDERING INFORMATION

MODEL	PACKAGE
CMP100AP	16-Pin DIP
CMP100AU	16-Lead SOIC

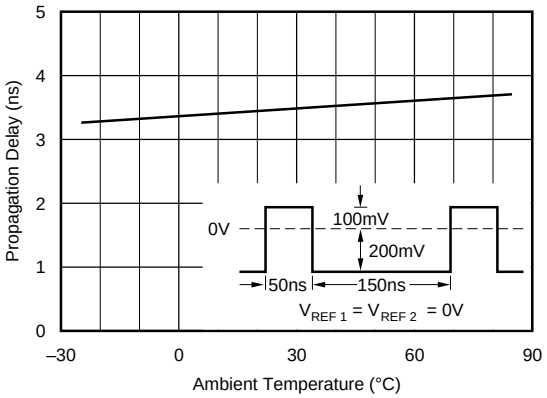
TYPICAL PERFORMANCE CURVES

T_A = 25°C and at rated supplies: V+ = +5V, V– = –5.2V unless otherwise noted.

PROPAGATION DELAY vs OVERDRIVE

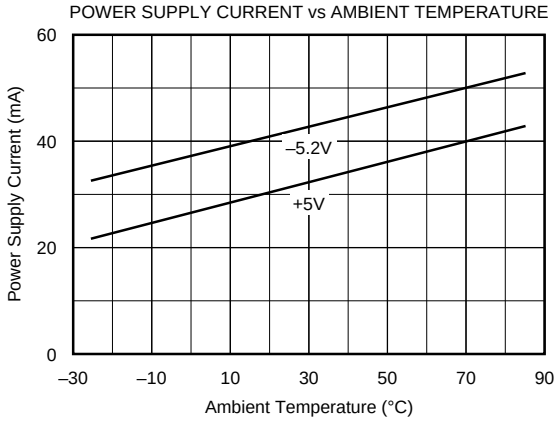


PROPAGATION DELAY vs AMBIENT TEMPERATURE

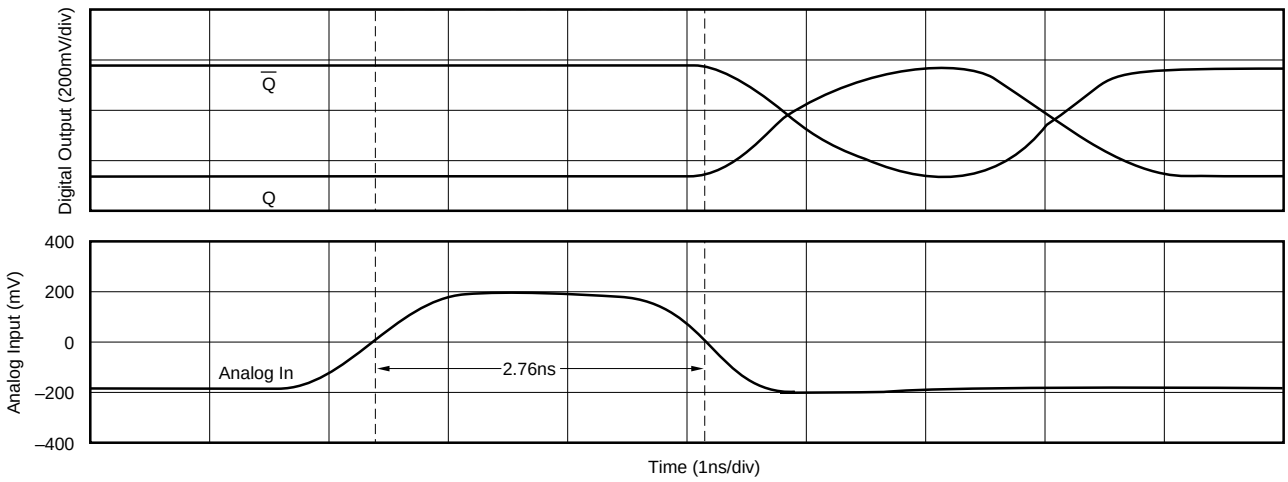


NOTE: Propagation Delay vs Overdrive is shown for two amplitudes of input pulse: from –200mV → $+V_{OD}$ (0.2nV/ns slew rate) and –1V → $+V_{OD}$ (1V/ns slew rate). For an inverse input waveform: from +1V → $–V_{OD}$ and from +200mV → $–V_{OD}$, propagation delays identical to those above are produced.

POWER SUPPLY CURRENT vs AMBIENT TEMPERATURE



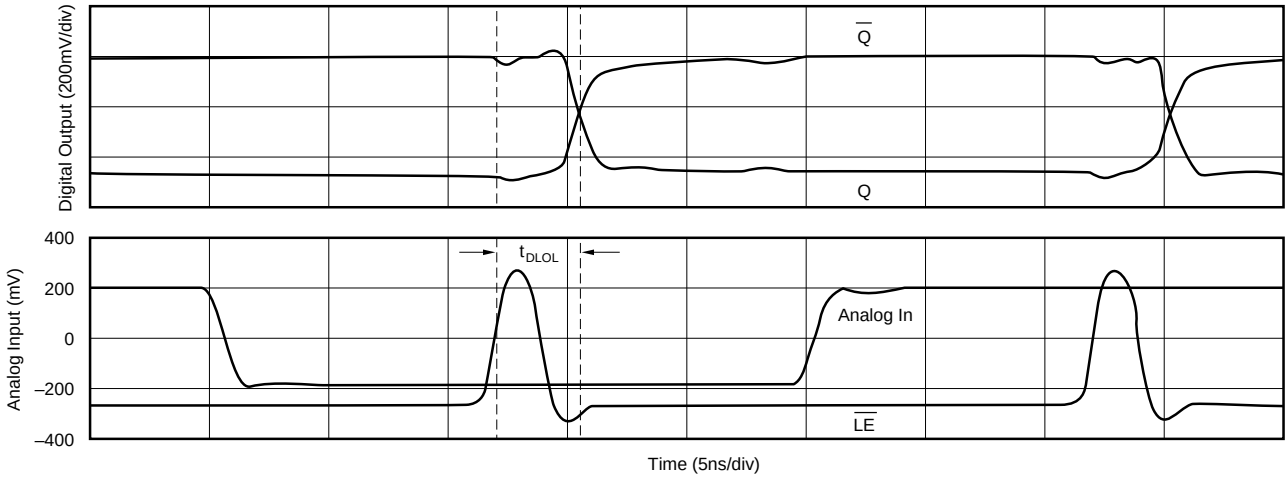
RESPONSE TO A 3ns ANALOG INPUT PULSE



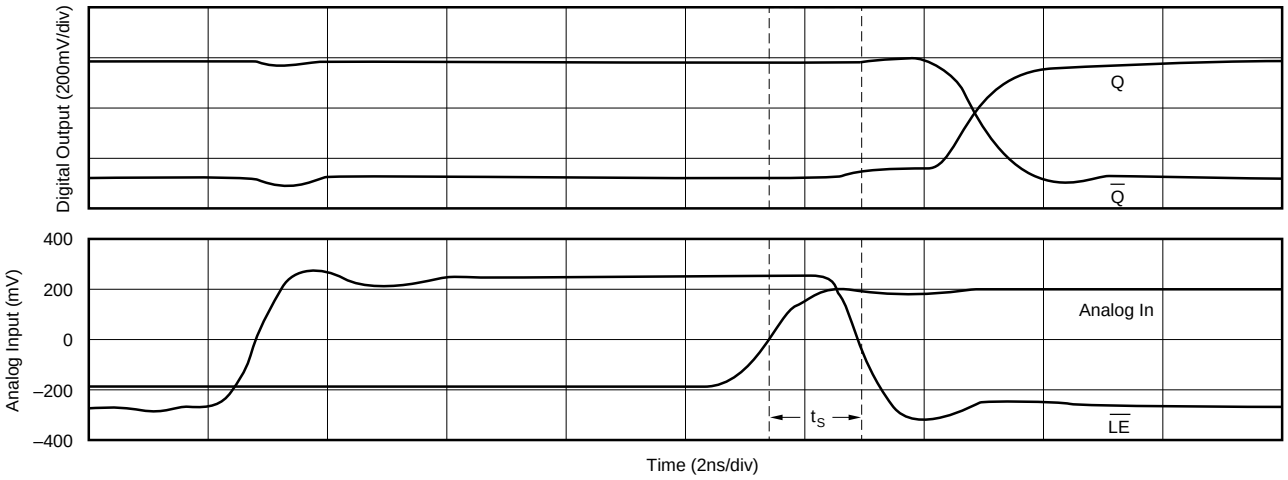
TYPICAL PERFORMANCE CURVES (CONT)

T_A = 25°C and at rated supplies: V+ = +5V, V– = –5.2V unless otherwise noted.

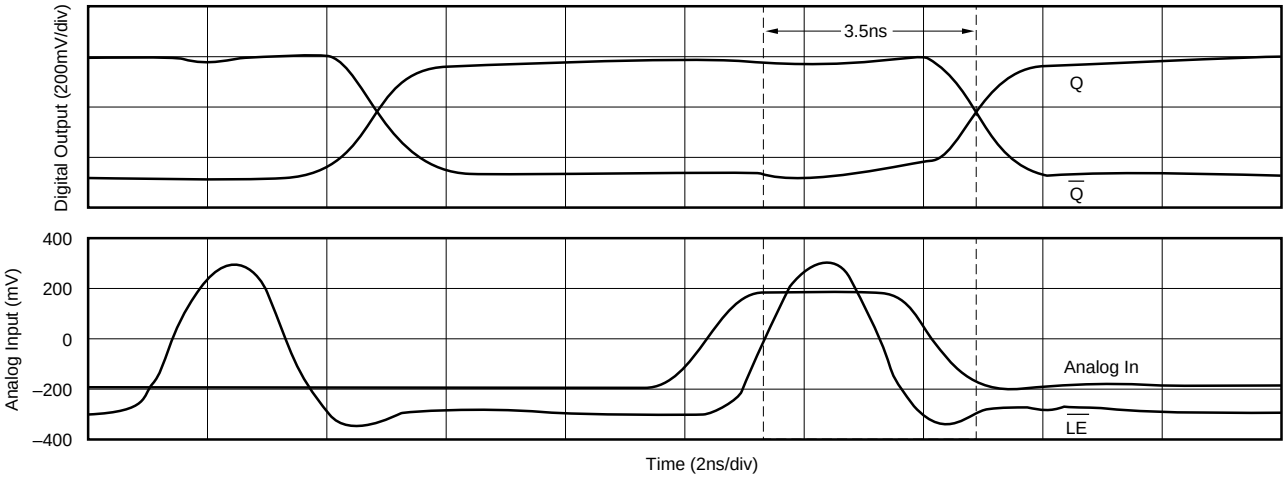
RESPONSE TO A 2ns LATCH ENABLE PULSE



SETUP TIME, t_S



CAPTURING A NARROW ANALOG PULSE



DISCUSSION OF SPECIFICATIONS

ANALOG INPUT

Offset Voltage, V_{OS}

The value of the the comparison threshold for $V_{REF\,1}$ or $V_{REF\,2}$ = 0V. V_{OS} and maximum drift vs temperature of V_{OS} are guaranteed.

Common Mode Error

As V_{REF} varies over its range, there is a small gain error which manifests itself as a change in the comparison level. Common mode error drifts typically –15µV/ºC.

DYNAMIC PERFORMANCE

Figure 1 illustrates the following analog and logic performance definitions.

Input to Output High Propagation Delay, t_{PDH}

t_{PDH} is the propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output (Q output) Low-to-High transition. Output logic is not latched for this definition.

Input to Output Low Propagation Delay, t_{PDL}

t_{PDL} is the propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output (Q output) High-to-Low transition. Output logic is not latched for this definition.

The propagation delay of the CMP100 is virtually identical for negative going and positive going analog input edges.

Differential Propagation Delay (Skew), t_{DIFF}

t_{DIFF} is the difference in propagation delay from one comparator to another. The skew between each half of one CMP100 is no greater than 200ps.

Propagation Delay Dispersion

Propagation Delay Dispersion is the variation in propagation delay versus input overdrive. Note that propagation delay may also be a function of input slew rate and of the previous level.

The input waveform for the propagation delay specification is illustrated in the first typical performance curve, Propagation Delay vs Overdrive. The Propagation Delay listed in the Electrical Specifications table is specified using an input waveform with 100mV overdrive, a previous level of –200mV and a slew rate of 200V/µs. A typical propagation delay curve is also shown for a previous level of –1V. The outputs are not latched for this specification.

Overdrive

Overdrive is the voltage by which the input exceeds $V_{REF} \pm V_{OS}$.

Minimum Set-Up Time, t_S

t_S is the minimum time before the positive transition of the Latch Enable (LE) that an analog input signal change must be present in order to be acquired and held at the outputs.

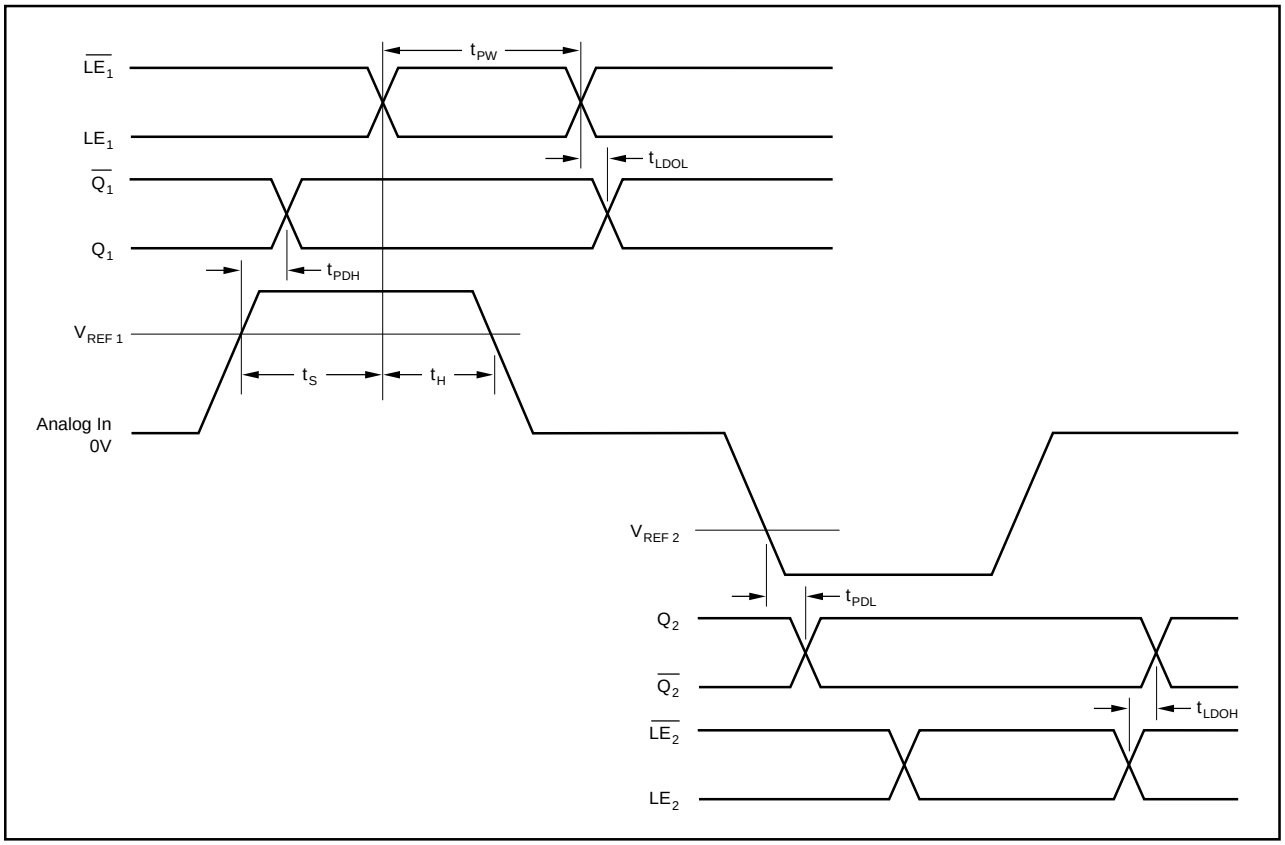


FIGURE 1. Analog and Logic Timing Definitions.

The t_S performance of CMP100 is illustrated in the Typical Performance Curves.

Minimum Hold Time, t_H

t_H is the minimum time after the positive transition of the Latch Enable (LE) that an analog input signal must remain unchanged in order to be acquired and held at the outputs. t_H = 0 for CMP100.

LOGIC PERFORMANCE DEFINITIONS

Latch Enable to Output High Delay, t_{DLOH}

t_{DLOH} is the propagation delay of latch logic circuits measured from the 50% point of the Latch Enable signal (LE) High-to-Low transition to the 50% point of an output (Q) Low-to-High transition.

Latch Enable to Output Low Delay, t_{DLOL}

t_{DLOL} is the propagation delay of latch logic circuits measured from the 50% point of the Latch Enable signal High-to-Low transition to the 50% point of an output (Q) High-to-Low transition.

Minimum Latch Enable Pulse Width, t_{PW}

t_{PW} is the minimum time that the Latch Enable (LE) must be High in order to acquire and hold an input signal change.

The actual timing performance of CMP100 is illustrated in the Typical Performance Curves.

OPERATING CONSIDERATIONS

INPUT VOLTAGE

Input reference voltages $V_{REF\ 1}$ and $V_{REF\ 2}$ may vary from –12V to +12V. The frequency-compensated analog input network can also swing from –12V to +12V.

Care must be taken to be sure that the Maximum Differential Input Voltage is not exceeded. That is, the voltage between Analog In and $V_{REF\ 1}$ or between Analog In and $V_{REF\ 2}$ must not exceed ±25V. If this voltage is exceeded by 1 or 2 volts, even momentarily, emitter-base voltage breakdown of the input transistors will occur and cause a permanent shift of the offset voltage, V_{OS}, to an out-of-spec value. However, the CMP100 will continue to function and will not be destroyed.

Input voltages to the CMP100 of uncontrolled magnitude may occur during system power-up. Take care to assure that the Absolute Maximum Differential Input Voltage is not exceeded during power-up.

DRIVING SOURCE IMPEDANCE

An apparent slow response of the CMP100 may be due a combination of high source impedance and stray capacitance to ground at the analog input. An R-C combination of 1kΩ source resistance and 10pF to ground results in a 10ns time constant—more than double the typical response time of the CMP100.

THE LATCH FUNCTION

The latch function is used for sampling the state of the outputs and holding them until the output can be processed.

Figure 1 shows a timing diagram for differential input latch enable controls, LE and $\overline{LE}$. The latches of the CMP100 are transparent type latches. If LE is Low ($\overline{LE}$ is High), the Q outputs indicate the sign of the input difference voltage. When LE goes High ($\overline{LE}$ Low), the comparator outputs are held at the current state.

When the analog input signal passes through the reference level, the comparator output Q changes, after a time of t_{PDH} or t_{PDL}. However, if the output is to be latched, the input signal must have crossed the threshold for a time t_S (set-up time) before the rising edge of LE occurs in order to capture the correct output state. On the other hand, in order to capture a correct output state just before it changes, it is necessary to maintain that output state for t_H, (hold time) after the rising edge of LE. t_H = 0 for CMP100.

A minimum latch pulse width of t_{PW} is needed to capture the state of narrow pulses. See the Typical Performance Curves for an example of sampling a narrow pulse.

10k ECL LOGIC

If the latching function is not used, the Latch Enable inputs ($\overline{LE_1}$ and $\overline{LE_2}$) should be returned to an ECL High voltage (–0.8V) or to Digital Common (0V). LE_1 and LE_2 should be returned to an ECL Low level (–1.8V), to an ECL bias voltage (–1.3V) or to the –2V 50Ω load pull-down power supply. Connecting an ECL input to –5.2V may create a marginal transistor emitter-base breakdown situation over the ambient temperature range and is not recommended.

If a single (non-differential) ECL logic input is used, connect the complementary input to an ECL bias voltage (–1.3V).

100k ECL LOGIC

The negative power supply, V–, of the CMP100 can be operated at –4.5V. The common mode input range of the analog and reference inputs will be reduced to +12V to –7.5V. Output levels are not affected by changing the V– power supply voltage to –4.5V.

TTL INPUTS

The operating common mode range of a logic input is –2V to +2V. Thus one can bias the logic inputs to use them with TTL inputs if the High input level is maintained below +2V. In this case, the complementary logic input should be biased at the TTL threshold of +1.4V.

LEVEL SHIFTING ECL to TTL

The ECL outputs can be translated to TTL using a Motorola MC10125 Quad ECL-TTL translator. The logic delay t_{DLOH} and t_{DLOL} and the propagation delay t_{PDL} and t_{PDH} will be increased by the delay of the translator.

INSTALLATION

TERMINATING ECL OUTPUTS

The best performance will be achieved with the use of proper ECL terminations. Such a configuration is illustrated in Figure 3. The open-emitter outputs of the CMP100 are designed to be terminated through 50Ω resistors to –2V or any other equivalent termination. If high-speed ECL signals must be routed more than a few centimeters, MicroStrip or StripLine techniques may be required to insure proper transition times and prevent output ringing.

POWER SUPPLY SELECTION

Linear power supplies are preferred. Although switching power supply rms specifications may appear to indicate low noise output, voltage spikes generated by switchers may be hard to filter. Their high-frequency components may be extremely difficult to keep out of the power supply return system. If switchers must be used, their outputs must be carefully filtered and the power supply itself should be shielded and located as far away as possible from precision analog circuits.

PRINTED CIRCUIT LAYOUT CONSIDERATIONS

Power Supply Wiring

Use heavy power supply and power supply common (ground) wiring. A ground plane under the part is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive circuits.

When passing power through a connector, use every available spare pin for making power supply return connections, and use some of the pins as a Faraday shield to separate the Analog and Digital Common lines.

Power Supply Returns (ACOM, DCOM and PWRCOM)

For best performance, connect ACOM (pin 13) and DCOM (pin 4) to the ground plane under the comparator. PWRCOM (pin 5), which is connected to the collectors of the ECL outputs, can be returned by separate printed circuit trace but its inductance should be kept low to avoid ringing. Do not connect ACOM and DCOM together at the end of a long printed circuit trace and then run a single wire to the power supply. To use separate ACOM and DCOM return printed circuit traces, connect a 1µF to 47µF tantalum capacitor between DCOM and ACOM pins as close to the package as possible.

Power Supply Bypassing

Every power supply line leading into the comparator must be bypassed to the Common pins. The bypass capacitor should be located as close to the comparator package as possible and tied to a solid return, preferably to the ground plane under the device. If the capacitors are not close enough to the package, DC resistance and inductance may be above acceptable levels. Use tantalum capacitors with values of from 1µF to 10µF. Parallel them with smaller ceramic

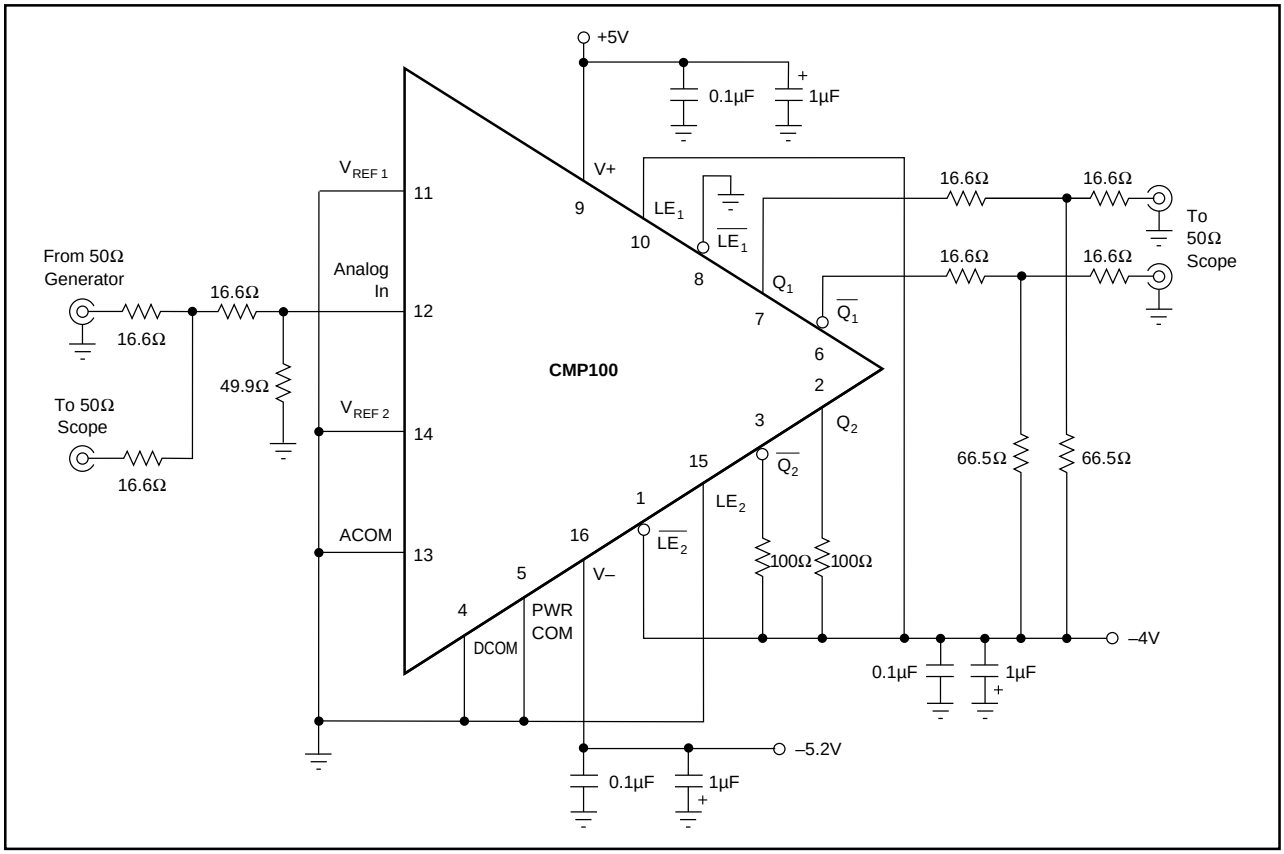


FIGURE 2. Circuit for Evaluating Analog Propagation Delay, t_{PDH}, t_{PDL}.

capacitors for high frequency filtering if necessary. Electrolytic capacitors are not recommended because their high frequency response is poor.

Separate the Analog and Digital Signals

Digital signal paths entering or leaving the layout should have minimum length to minimize crosstalk to analog wiring. Stray capacitive feedback from digital outputs to the analog input may cause the outputs to appear fuzzy well after the outputs have changed. Keep analog signals as far away as possible from digital signals. If they must cross, cross them at right angles. Coaxial cable may be necessary for analog inputs in some situations.

MEASURING CMP100 PERFORMANCE

USING AN OSCILLOSCOPE

Oscilloscope probes should be matched to the oscilloscope. Use an oscilloscope with at least 400MHz bandwidth.

Be sure the probe compensation is adjusted properly. Improper compensation will result in apparent overshoot and/or ringing if undercompensated, and an apparent slow edge if overcompensated. If the probe ground lead is too long, the output may appear distorted and oscillatory. Use probes with short (less than one inch) ground straps or use a coaxial cable connection instead of a probe. Do not use X1 or "straight" probes. Their bandwidth is 20MHz or less and capacitive loading is high. The best method is to use 50Ω matched terminations as shown in Figures 2 and 3.

MEASURING PROPAGATION DELAY

Figure 2 shows a circuit configuration used for evaluating propagation delay. It uses 50Ω matched terminations between the instruments and the CMP100 for best signal integrity. An HP8130A Pulse Generator is used for the analog input and for the latching signals. The oscilloscope is an HP54503A 500MHz Digitizing Oscilloscope. This setup was used to generate the dynamic performance waveforms in the Typical Performance Curves section.

MEASURING LOGIC TIMING

Figure 3 shows the circuit configuration used for evaluating logic propagation delay. The logic input LE1 has been added to the circuit of Figure 2.

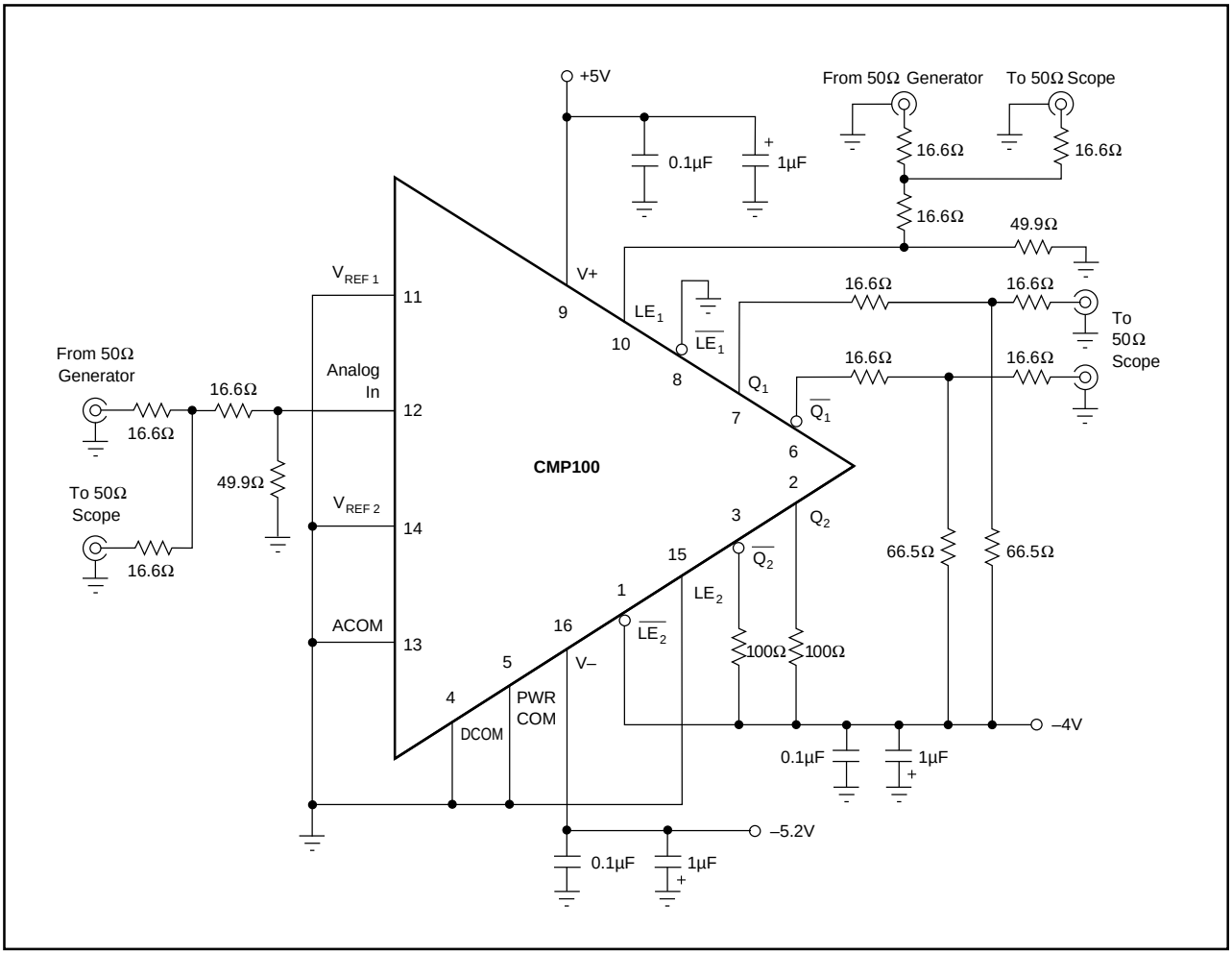


FIGURE 3. Circuit for Evaluating Logic Timing.

CMP100 APPLICATIONS

ATE PIN RECEIVER

A typical ATE pin receiver application using CMP100 is illustrated in Figure 4. The reference inputs, $V_{REF\,1}$ and $V_{REF\,2}$ are driven by D/A converters (Figure 5) while analog input is driven directly from the device under test (DUT).

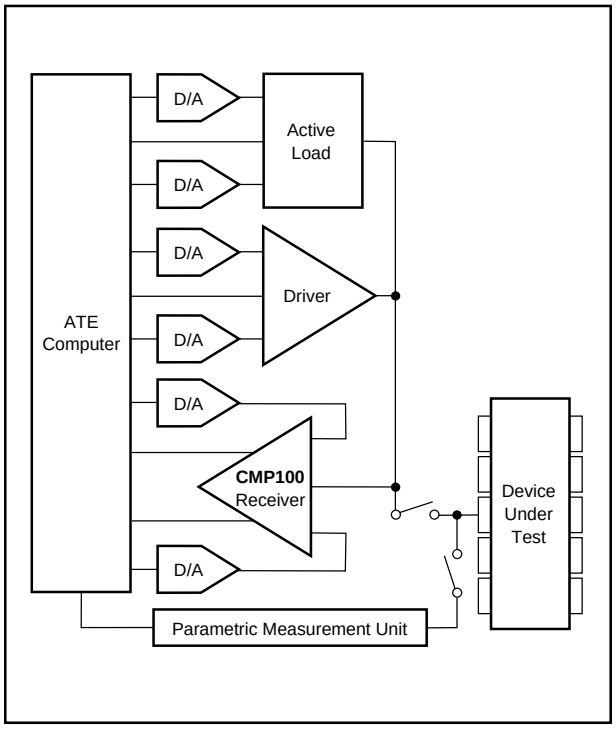


FIGURE 4. Typical ATE Pin Receiver Application.

WINDOW COMPARATOR

Because of its high speed, the CMP100 can be used to make timing measurements on modest-speed digital or high-speed analog waveforms. When the outputs of the CMP100 are combined with a NOR gate, a true window comparator function is implemented. Refer to gate G3 of Figure 6. The output pulse width generated by an input signal passing through the reference levels can be measured. This could be for a rise-time/fall-time measurement (setting the reference levels at 10% and 90% of the signal height) of a modest speed digital waveform, or for the width (and hence the value) of an analog ramp moving between two values from an integrating type signal detector.

PULSE RECOVERY

The window comparator function can also be used to reconstruct pulses that have been degraded. Positive and/or negative reference levels can be set up to detect both High and Low levels of the pulse.

A plot of the response of CMP100 to a narrow pulse with V_{REF1} = 0V is shown in the Typical Performance Curves section.

DETECTING TRANSIENTS

CMP100 can be connected to Detect and Hold transient occurrences above and below threshold voltages set by $V_{REF\,1}$ and $V_{REF\,2}$ as illustrated in Figure 6. The outputs of comparator 1 and comparator 2 are fed back to their LE inputs in order to self-latch their outputs. The Reset control is used to "unlock" the outputs after the transient occurrence has been read. The output NOR gate G3 combines CMP100 outputs into a single-output window comparator function.

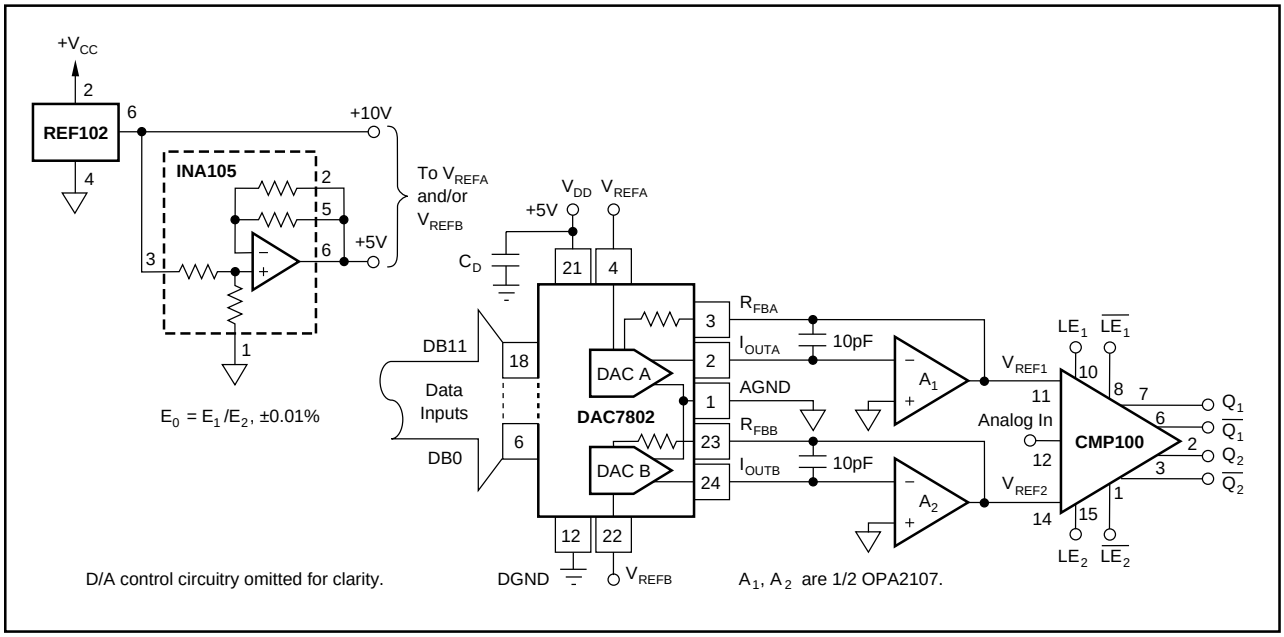


FIGURE 5. Dual DAC7802 (12-bit port), DAC7801 (8-bit port) or DAC7800 (serial port) D/A Converters Supply Reference Inputs to the CMP100. For higher resolution use DAC725, dual 16-bit D/A converter.

Note that the transient being detected must remain above $V_{REF\ 1}$ (or below $V_{REF\ 2}$) longer than the propagation delay of the CMP100 plus the propagation delay of gates G1 and G2.

In an application where only one polarity of transient needs to be captured, comparator 2 (not latched) can be used as the source of the Reset control signal to unlock comparator 1 based on a different threshold condition (defined by $V_{REF\ 2}$) on the analog input signal. This connection will stretch the transient occurrence for the time the $V_{REF\ 2}$ condition is present.

WIDE-BAND AMPLIFIERS FOR ANALOG INPUT SIGNAL CONDITIONING

In a component test application the analog input of the CMP100 is usually driven directly from the DUT output. Other applications may require a high-speed buffer or voltage gain ahead of the CMP100. Recommended wide-bandwidth amplifiers are Burr-Brown OPA603 for up to ±10V signals, or OPA620/OPA621 for very wide-band ±3V signals. A high speed instrumentation amplifier such as the Burr-Brown INA110 can be used for common mode rejection.

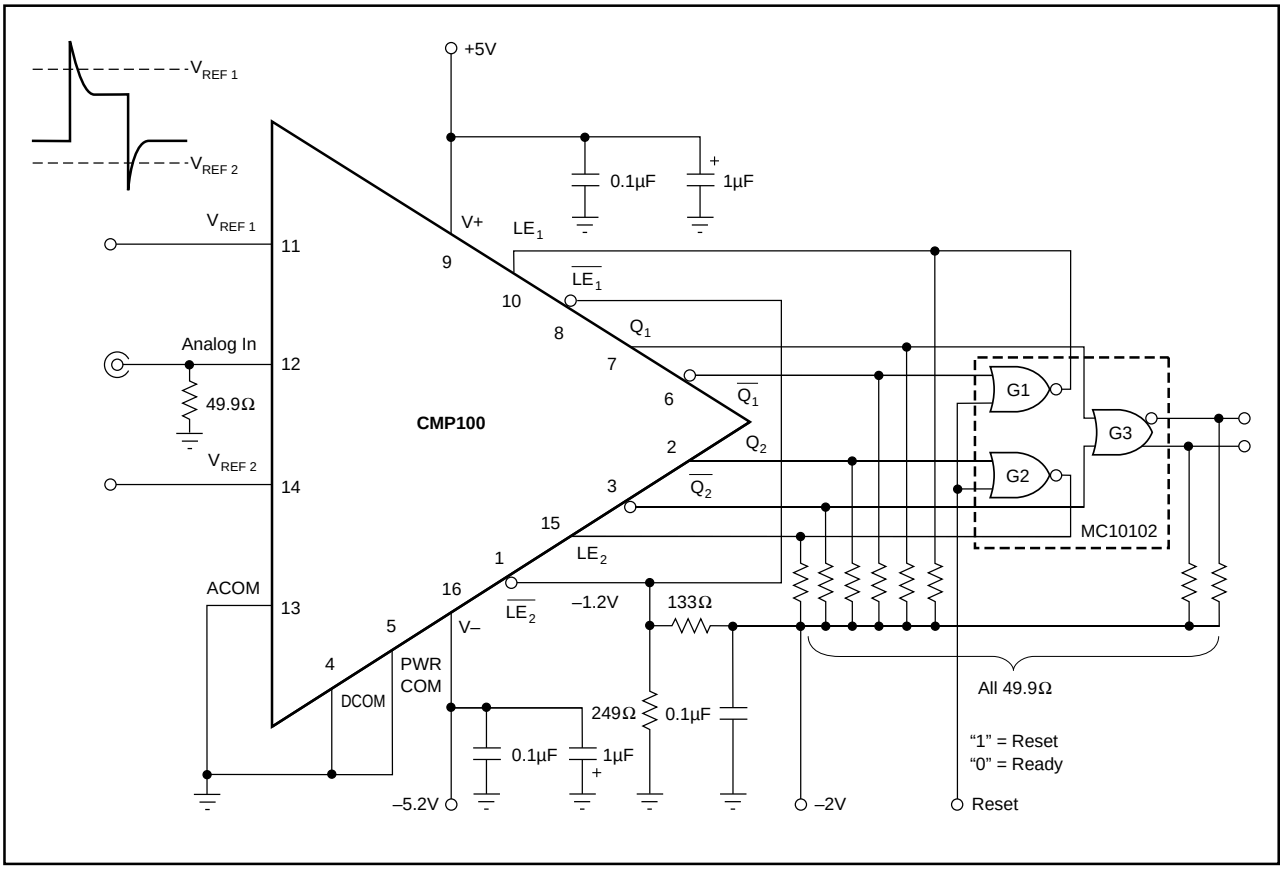


FIGURE 6. CMP100 Used to Detect and Hold Transient Occurrences on the Output Pulse of a Device Under Test, or Out-of-Limits Conditions in a Process-Variable Monitoring Application.