4-Phase Interleaved Boost PWM Controller with Light Load Efficiency Enhancement

ISL78225

The ISL78225 4-phase controller is targeted for applications where high efficiency (>95%) and high power are required. The multiphase boost converter architecture uses interleaved timing to multiply channel ripple frequency and reduce input and output ripple. Lower ripple results in fewer input/output capacitors and therefore lower component cost and smaller implementation area.

The ISL78225 has a dedicated pin to initiate the phase dropping scheme for higher efficiency at light load by dropping phases based on the load current, so the switching and core losses in the converter are reduced significantly. As the load increases, the dropped phase(s) are added back to accommodate heavy load transients and improve efficiency.

Input current is sensed continuously by measuring the voltage across a dedicated current sense resistor or inductor DCR. This current sensing provides precision channel-current balancing, and per-phase overcurrent protection. A separate totalizing current limit function provides overcurrent protection for all the phases combined. This two-stage current protection provides maximum performance and circuit reliability.

ISL78225 can also provide for input voltage tracking via the VREF2 pin. The comparison reference voltage will be the lower of the VREF2 pin or the internal 2V reference. By using a resistor network between VIN and VREF2 pin, the output voltage can track input voltage to limit the output power during automotive cranking conditions.

ISL78225 can output a clock signal for expanding operation to 8 phases, which offers high system flexibility. The threshold-sensitive enable input is available to accurately coordinate the start-up of the ISL78225 with any other voltage rail.

Features

- Peak Current Mode PWM Control with Adjustable Slope Compensation
- Precision Resistor/DCR Current Sensing
- 2, 3 or 4-Phase Operation
- Adjustable Phase Dropping/Diode Emulation/Pulse Skipping for High Efficiency at Light Load
- Adjustable Switching Frequency or External Synchronization from 75kHz up to 1MHz Per Phase
- Over-Temperature/Overvoltage Protection
- 2V ±1.0% Internal Reference
- Pb-Free 44-Lead 10x10 EP-TQFP (RoHS Compliant)
- -40°C to +125°C Operating Temperature Range
- AEC-Q100 Qualified
- TS16949 Compliant

Applications

- Automotive Power Supplies
  - Start/Stop DC/DC Converter
  - Fuel Pumps
  - Injection System
- Audio Amplifier Power Supplies
- Telecom and Industrial Power Supplies

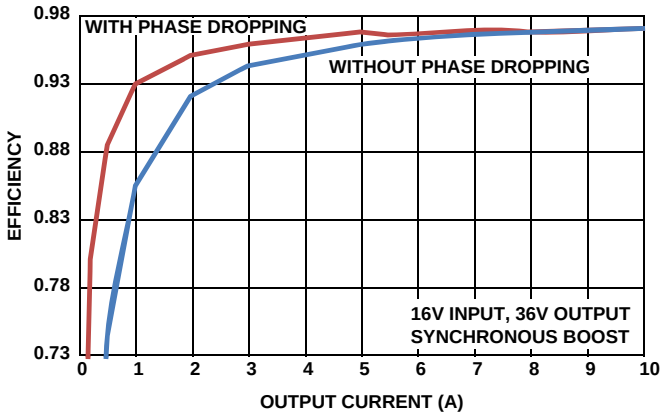
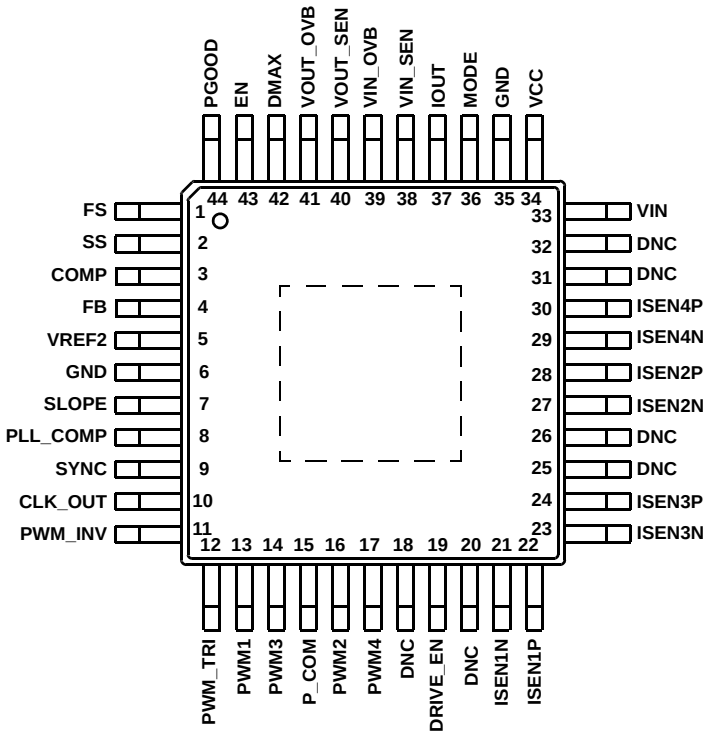


FIGURE 1. EFFICIENCY vs OUTPUT CURRENT vs PHASE DROPPING MODE

Pin Configuration

ISL78225
(44 LD 10x10 EP-TQFP)
TOP VIEW



Functional Pin Descriptions

PIN #	SYMBOL	DESCRIPTION
1	FS	A resistor placed from FS to ground will set the PWM switching frequency.
2	SS	Use this pin to set-up the desired soft-start time. A capacitor placed from SS to ground will set up the soft-start ramp rate and in turn determine the soft-start time.
3	COMP	The output of the transconductance amplifier. Place the compensation network between COMP and GND for compensation loop design.
4	FB	The inverting input of the transconductance amplifier. A resistor network should be placed between the FB pin and output rail to set the output voltage.
5	VREF2	External reference input to the transconductance amplifier. When the VREF2 pin voltage drops below 1.8V, the internal reference will be shifted from 2V to VREF2. The VREF2 voltage can be programmed by connecting a resistor divider network from VCC or VIN.
6	GND	Bias and reference ground for the IC.
7	SLOPE	This pin programs the slope of the internal slope compensation. A resistor should be connected from the SLOPE pin to GND. Please refer to “Adjustable Slope Compensation” on page 19 for how to choose the resistor value.
8	PLL_COMP	This pin serves as the compensation node for the PLL. A second order passive loop filter connected between PLL_COMP pin and GND compensates the PLL feedback loop.
9	SYNC	Frequency synchronization pin. Connecting the SYNC pin to an external square pulse waveform (typically 20% to 80% duty cycle) will synchronize the converter switching frequency to the fundamental frequency of the input waveform. If SYNC function is not used, tie the SYNC pin to GND. A 500nA current source is connected internally to pull-down the SYNC pin if it is left open.
10	CLK_OUT	This pin provides a clock signal to synchronize with another ISL78225. This provides scalability and flexibility. The rising edge signal on the CLKOUT pin is in phase with the leading edge of the PWM1 signal.
11	PWM_INV	This pin determines the polarity of the PWM output signal. Pulling this pin to GND will force normal operation. Pulling this pin to VCC will invert the PWM signal. This function provides the flexibility for the ISL78225 to work with different drivers.

Functional Pin Descriptions (Continued)

PIN #	SYMBOL	DESCRIPTION
12	PWM_TRI	This pin enables the tri-level of the PWM output signal. Pulling this pin to GND forces the PWM output to be traditional two level logic. Pulling the PWM_TRI pin to VCC will enable tri-level PWM signals, then the PWM output can be at the 2.5V tri-level condition.
13, 14, 16, 17	PWM1, PWM3, PWM2, PWM4	Pulse width modulation outputs. Connect these pins to the PWM input pins of the external driver ICs. The number of active channels is determined by the state of PWM3, PWM4. For 2-phase operation, connect PWM3 to VCC; similarly, connect PWM4 to VCC for 3-phase operation.
15	P_COM	PWM Compensation pin; connect this pin through resistor to VCC.
19	DRIVE_EN	Driver enable output pin. This pin is connected to the enable pin of MOSFET drivers.
18,20,25, 26,31,32	DNC	Do Not Connect – These pins must be left floating.
21, 22, 23, 24, 27, 28, 29, 30	ISEN1N, ISEN1P, ISEN3N, ISEN3P, ISEN2N, ISEN2P, ISEN4N, ISEN4P	The ISENxP and ISENxN pins are current sense inputs to individual differential amplifiers. The sensed current is used as a reference for current mode control and overcurrent protection. Inactive channels should have their respective ISENxP pins connected to VIN and ISENxN pins left open. The ISL78225 utilizes external sense resistor current sensing method or Inductor DCR sensing method.
33	VIN	Connect input rail to this pin. This pin is connected to the internal linear regulator, generating the power necessary to operate the chip. It is recommended the DC voltage applied to the VIN pin does not exceed 40V.
34	VCC	This pin is the output of the internal linear regulator that supplies the bias and gate voltage for the IC. A minimum 4.7µF decoupling ceramic capacitor should be connected from VCC to GND. The controller starts to operate when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold. This pin can be connected directly to a +5V supply if VIN falls below 5.6V.
35	GND	Bias and reference ground for the IC.
36	MODE	Mode selection pin. Pull this pin to logic HIGH for forced PWM mode; phase dropping/adding is inactive during forced PWM mode. Connecting a resistor from MODE pin to GND will initialize phase dropping mode (PDM). In PDM, a 5µA fixed reference current will flow out of the MODE pin, and the phase dropping threshold can be programmed by adjusting the resistor value.
37	IOUT	IOUT is the current monitor pin with an additional OCP adjustment function. An RC network needs to be placed between IOUT and GND to ensure the proper operation. The voltage at the IOUT pin will be proportional to the input current. If the voltage on the IOUT pin is higher than 2V, ISL78225 will go into overcurrent protection mode and the chip will latch off until the EN pin is toggled.
38	VIN_SEN	The VIN_SEN pin is used for sensing the VIN voltage. A resistor divider network is connected between this pin and boost power stage input voltage rail. When the voltage on VIN_SEN is greater than 2.4V, the VIN_OVB pin will be pulled low to indicate an input overvoltage condition. The threshold voltage can be programmed by changing the divider ratios.
39	VIN_OVB	The VIN_OVB pin is an open drain indicator of an overvoltage condition at the input. When the voltage on the VIN_SEN pin is greater than the 2.4V threshold, the VIN_OVB pin will be pulled low.
40	VOUT_SEN	The VOUT_SEN pin is used for sensing the output voltage; a resistor divider network is connected between this pin and output voltage rail. When the voltage on VOUT_SEN pin is greater than 2.4V, VOUT_OVB pin will be pulled low, indicating an output overvoltage condition.
41	VOUT_OVB	The VOUT_OVB pin is an open drain indicator of an overvoltage condition at the output. When the voltage on the VOUT_SEN pin is greater than the 2.4V threshold, the VOUT_OVB pin will be pulled low and latched, toggling VIN or EN will reset the latch.
42	DMAX	DMAX pin sets the maximum duty cycle of the PWM modulator. If the DMAX pin is connected to GND, the maximum duty cycle will be set to 91.7%. Floating this pin will limit the duty cycle to 75% and connecting the DMAX pin to VCC will limit the duty cycle to 83.3%.
43	EN	This pin is a threshold-sensitive enable input for the controller. Connecting the power supply input to EN pin through an appropriate resistor divider provides a means to synchronize power-up of the controller and the MOSFET driver ICs. When EN pin is driven above 1.2V, the ISL78225 is active depending on status of the internal POR, and pending fault states. Driving the EN pin below 1.1V will clear all fault states and the ISL78225 will soft-start when re-enabled.
44	PGOOD	This pin is used as an indication of the end of soft-start and output regulation. It is an open-drain logic output that is low impedance until the soft-start is completed. It will be pulled low again once the UV/OV/OC/OT conditions are detected.
	Exposed Pad	It is recommended to solder the Exposed Pad to the ground plane.

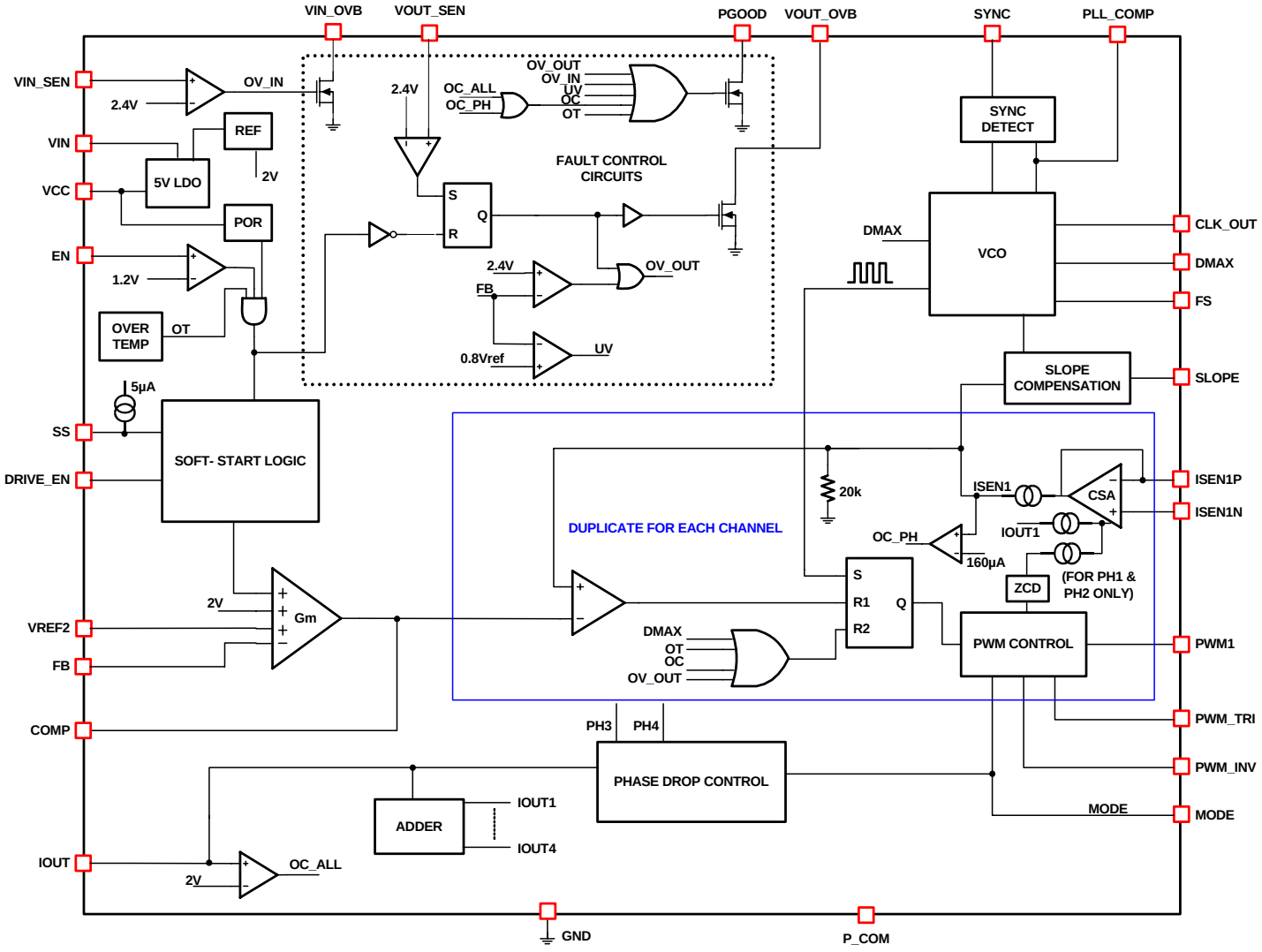
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE TAPE & REEL (Pb-free)	PKG. DWG. #
ISL78225ANEZ-T	ISL78225 ANEZ	-40 to +125	44 Ld EP-TQFP	Q44.10x10A

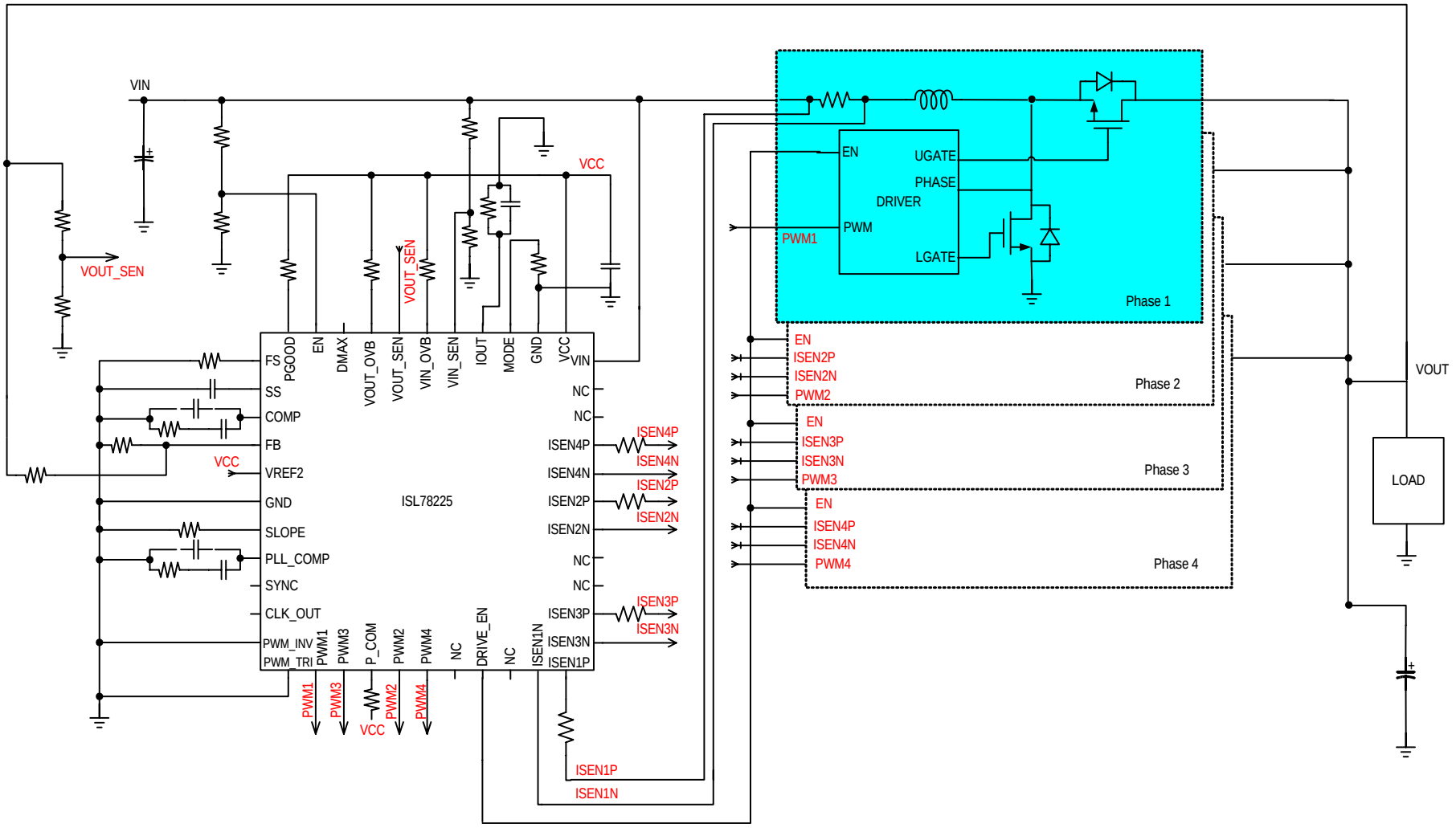
NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78225. For more information on MSL please see techbrief TB363.

ISL78225 Block Diagram

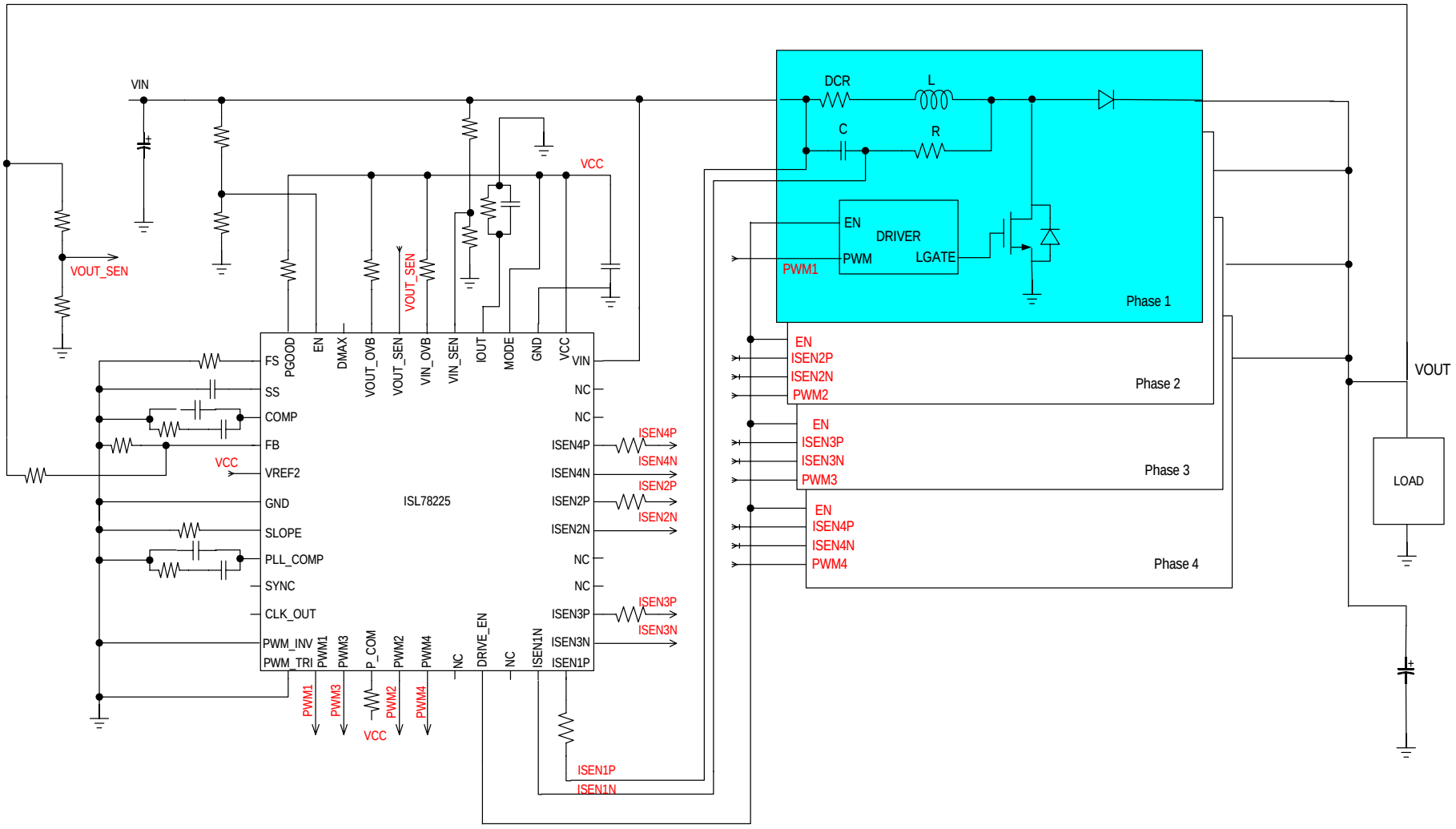


Typical Application 1: 4-Phase Synchronous Boost Converter with Sense Resistor Current Sensing



Note: Please see ISL78420 for an Automotive Qualified 100V synchronous boost driver.

Typical Application 2: 4-Phase Standard Boost Converter with DCR Current Sensing



Absolute Maximum Ratings

Supply Voltage, VIN . . . . . GND-0.3V to +45V
All ISEN_ Pins . . . . . V_{IN}-5V to V_{IN}+0.3V
VCC . . . . . GND-0.3V to +6V
All Other Pins . . . . . GND-0.3V to V_{CC}+0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114E) 2.5kV
Machine Model (Tested per JESD-A115-A) 200V
Charge Device Model (Tested per JESD22-C101C) 1.5kV
Latch Up (Tested per JESD78B, Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
44 Ld EP-TQFP Package (Notes 4, 5)	28	2.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Voltage at VIN . . . . . +5.6V to +40V
All ISEN_ Pins . . . . . VIN-5V to VIN+0.3V
Voltage at VCC . . . . . +5V ±5%
Ambient Temperature (Auto) . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: V_{IN} = 12V, T_A = -40°C to +125°C, unless otherwise specified. Typical specifications are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
SUPPLY INPUT					
Input Voltage Range		**5.6**	12	**40**	V
Input Supply Current (Normal Mode)	V_{IN} = 12V, R_{FS} = 158kΩ (For f_S = 250kHz), EN = 5V		8	**12**	mA
Input Supply Current (Shutdown Mode)	V_{IN} = 12V, R_{FS} = 158kΩ (For f_S = 250kHz), EN = 0V			**10**	µA
INTERNAL LINEAR REGULATOR					
LDO Output Voltage (VCC Pin)	V_{IN} > 5.6V, C_L = 4.7µF from VCC to GND, I_{VCC} < 50mA	**4.75**	5	**5.25**	V
LDO Current Limit (VCC pin)	VCC = 3V, C_L = 4.7µF from VCC to GND		200 (Note 7)		mA
POWER-ON RESET (POR) AND ENABLE					
POR Threshold	VCC Rising	**4.4**	4.5	**4.6**	V
	VCC Falling	**4.1**	4.2	**4.3**	V
EN Threshold	Rising	**1.1**	1.2	**1.3**	V
	Hysteresis		70		mV
OSCILLATOR					
Accuracy of Switching Frequency Setting	R_{FS} = 158kΩ from FS to GND	**225**	250	**275**	kHz
Adjustment Range of Switching Frequency		**75**		**1000**	kHz
FS pin voltage			1		V
SOFT-START					
Soft-Start Current	C_{SS} = 2.2nF from SS to GND	**4**	5	**6**	µA
Soft-Start Pre-Bias Voltage Range		**0**		**2**	V
Soft-Start Pre-Bias Voltage Accuracy	V_{FB} = 500mV	**-25**		**25**	mV
Soft-Start Clamp Voltage			3.4		V
REFERENCE VOLTAGE					
System Accuracy	-40°C to +125°C, measure at FB pin, V_{REF2} > 2.5V	**1.98**	2	**2.02**	V
FB Pin Input Bias Current	V_{FB} = 2V, V_{REF2} > 2.5V	**-1**		**1**	µA
V_{REF2} Pin Input Bias Current	V_{REF2} = 1.6V	**-1**		**1**	µA

Electrical Specifications Operating Conditions: V_{IN} = 12V, T_A = -40°C to +125°C, unless otherwise specified. Typical specifications are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
V_{REF2} External Reference Voltage Range		**0.7**		**1.8**	V
V_{REF2} External Reference Voltage Accuracy	-40°C to +125°C, measure at FB pin, V_{REF2} = 1.8V	**-1**		**1**	%
	-40°C to +125°C, measure at FB pin, V_{REF2} = 0.7V	**-1.5**		**1.5**	
ERROR AMPLIFIER					
Transconductance Gain			2		mS
Output Impedance			5		MΩ
Unity Gain Bandwidth	C_{COMP} = 100pF from COMP pin to GND		11		MHz
Slew Rate	C_{COMP} = 100pF from COMP pin to GND		2.5		V/µs
Output Current Capability			±300		µA
Maximum Output Voltage		**3.5**			V
Minimum Output Voltage				**0.5**	V
PWM CORE					
Duty Cycle Matching	I_{ISENxP} = 60µA, R_{SLOPE} = 30.1k, f_S = 250kHz, V_{COMP} = 2V, 4-phase, T_A = +25°C	-6		6	%
Zero Crossing Detection (ZCD) Threshold for PWM1/PWM2	$R_{SEN1, 2}$ = 750Ω		3		mV
Leading Edge Blanking (Audio Mode)	V_{MODE} = VCC, V_{PWM_TRI} = VCC, V_{COMP} = 0.5V		Ts/12 (Note 8)		ns
Leading Edge Blanking (Other Mode)	V_{MODE} <4V or V_{PWM_TRI} = GND, V_{COMP} = 0.5V		130		ns
SLOPE pin Voltage		**385**	515	**650**	mV
ISENxN Bias Current	V_{ISENxN} = V_{ISENxP}, from V_{IN} - 1V to V_{IN}		0.3		µA
ISENxN, ISENxP Common Mode Voltage Range	V_{IN} > 12V	**V_{IN}-5**		**V_{IN}**	V
PWMx OUTPUT					
PWMx Output Voltage LOW	I_{PWMx} = -500µA			**0.5**	V
PWMx Output Voltage HIGH	I_{PWMx} = +500µA	**4.5**			V
PWMx Tri-State Output Voltage	I_{PWMx} = ±100µA	**2.3**	2.5	**2.7**	V
PWMx Pull-Down Current	During Phase Detection Time (t_3 on Figure 14), V_{PWM} = 1V		50		µA
PWM3, PWM4 Disable Threshold	During Phase Detection Time (t_3 on Figure 14)	**3.5**			V
PHASE ADDING/DROPPING					
MODE Pull-up Current	V_{MODE} = 2.4V	**4.2**	5.1	**5.6**	µA
V_{IOUT} Threshold, 4-phase, Drop Phase 4	V_{MODE} = 1.6V	**1.175**	1.2	**1.225**	V
V_{IOUT} Threshold, 4-phase, Drop Phase 3	V_{MODE} = 1.6V	**0.775**	0.8	**0.825**	V
V_{IOUT} Threshold, 3-phase, Drop Phase 3	V_{MODE} = 1.8V	**1.175**	1.2	**1.225**	V
V_{IOUT} Threshold Hysteresis			40		mV
Phase Drop Disable Threshold at MODE pin		**3.5**	4		V
CURRENT SENSE AND OVERCURRENT PROTECTION					
Peak Current Limit for Individual Channel			160		µA
IOUT Current Tolerance	I_{ISENxP} = 60µA, 4-phase	**173**	187	**200**	µA
Maximum Voltage Limit at IOUT Pin			2.0		V
DMAX PIN					
DMAX Threshold, High		**3**			V
DMAX Threshold, Low				**2**	V
DMAX Floating Voltage	During Phase Detection Time (t_3 on Figure 14)		2.5		V

Electrical Specifications Operating Conditions: V_{IN} = 12V, T_A = -40°C to +125°C, unless otherwise specified. Typical specifications are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Max Duty Cycle, DMAX = GND	V_{COMP} = 3.5V		91.7		%
Max Duty Cycle, DMAX = FLOAT	V_{COMP} = 3.5V		75		%
Max Duty Cycle, DMAX = VCC	V_{COMP} = 3.5V		83.3		%
DMAX Source/Sink Current	During t_3 on Figure 14		50		µA
DMAX Source/Sink Current	After t_3 on Figure 14	**-1**		**1**	µA
PWM_TRI, PWM_INV, SYNC PIN DIGITAL LOGIC					
Input Leakage Current	EN < 1V	**-1**		**1**	µA
Input Pull-Down Current	EN > 2V, Pin Voltage = 2.1V		0.4	**1.5**	µA
Logic Input Low				**0.8**	V
Logic Input High		**2**			V
DRIVE_EN, CLK_OUT PIN					
Output High Voltage	I_{DRIVE_EN} = 500µA	**4.5**			V
Output Low Voltage	I_{DRIVE_EN} = -500µA			**0.5**	V
VOUT SENSE PIN					
Input Leakage Current		**-1**		**1**	µA
Threshold Voltage		**2.325**	2.4	**2.475**	V
VIN SENSE PIN					
Input Leakage Current		**-1**		**1**	µA
Threshold Voltage		**2.325**	2.4	**2.475**	V
Hysteresis			110		mV
VOUT_OVB, VIN_OVB PIN					
Leakage Current	V_{PIN} = HIGH			**1**	µA
Low Voltage	I_{PIN} = 0.5mA			**0.2**	V
POWER GOOD MONITOR PIN					
PGOOD Leakage Current	PGOOD = HIGH			**1**	µA
PGOOD Low Voltage	I_{PGOOD} = 0.5mA			**0.2**	V
Overvoltage Rising Trip Point	V_{FB}/V_{REF}, V_{REF2} > 2.5V	**117**	120	**123**	%
Overvoltage Rising Hysteresis	V_{FB}/V_{REF}, V_{REF2} > 2.5V		5		%
Undervoltage Rising Trip Point	V_{FB}/V_{REF}, V_{REF2} > 2.5V	**77**	80	**83**	%
Undervoltage Rising Hysteresis	V_{FB}/V_{REF}, V_{REF2} > 2.5V		5		%
OVER-TEMPERATURE PROTECTION					
Over-Temperature Trip Point			160		°C
Over-Temperature Recovery Threshold			145		°C

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise noted. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. Please refer to LDO current derating curve in “Internal 5V LDO Output Current Limit Derating Curves” on page 19 for I_{MAX} vs V_{IN}.
8. Ts = Switching Period = 1/(switching frequency).

Typical Performance Curves

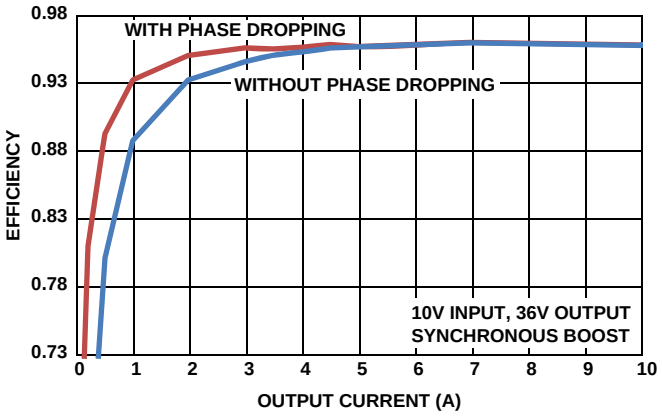


FIGURE 2. 10V INPUT EFFICIENCY vs OUTPUT CURRENT vs PHASE DROPPING MODE

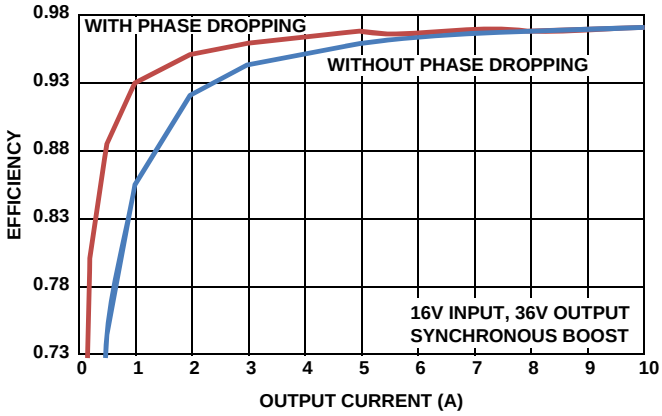


FIGURE 3. 16V INPUT EFFICIENCY vs OUTPUT CURRENT vs PHASE DROPPING MODE

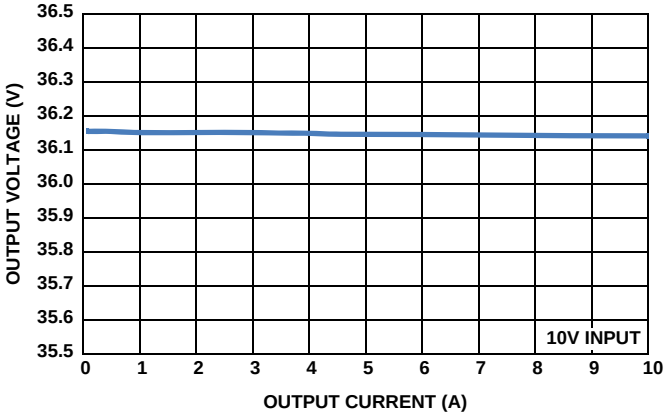


FIGURE 4. OUTPUT VOLTAGE vs OUTPUT CURRENT

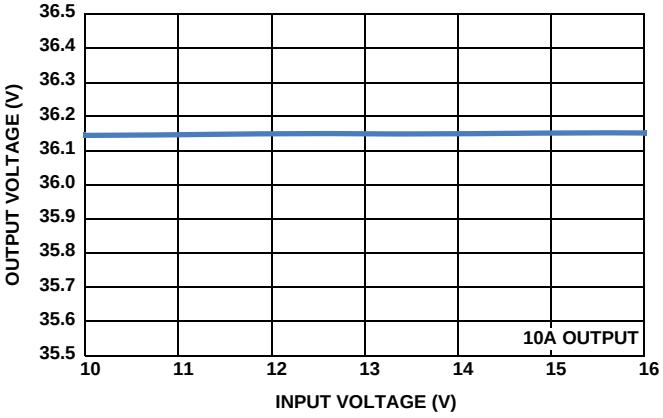


FIGURE 5. OUTPUT VOLTAGE vs INPUT VOLTAGE

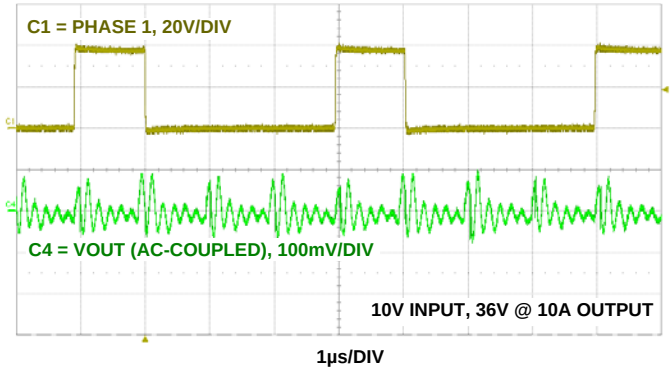


FIGURE 6. FULL LOAD OUTPUT RIPPLE

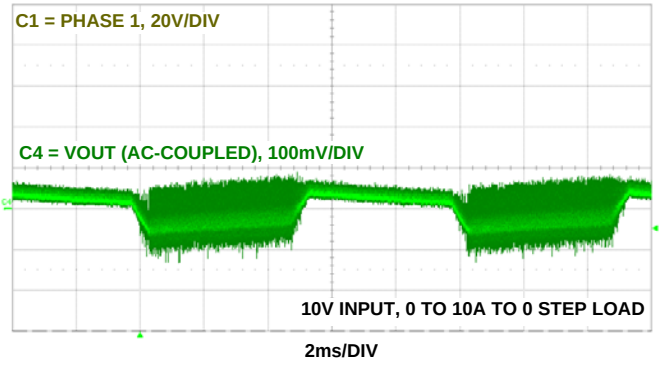


FIGURE 7. FULL STEP LOAD TRANSIENT

Typical Performance Curves (Continued)

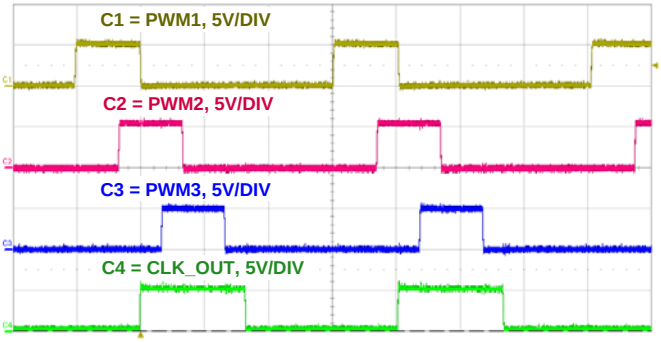


FIGURE 8. WAVEFORMS WITH PWM_INV = GND

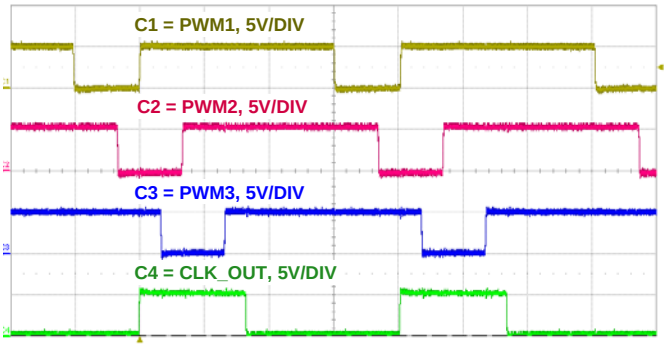


FIGURE 9. WAVEFORMS WITH PWM_INV = V_{CC}

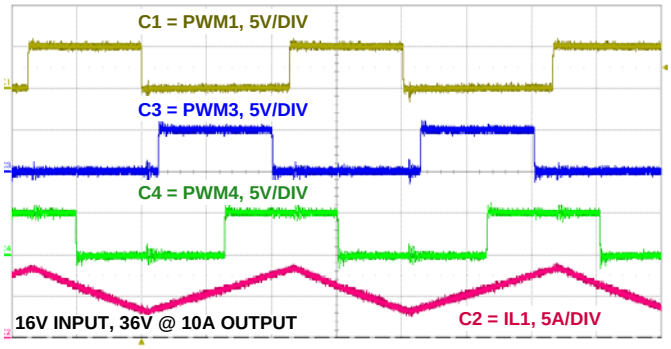


FIGURE 10. FULL LOAD WAVEFORMS

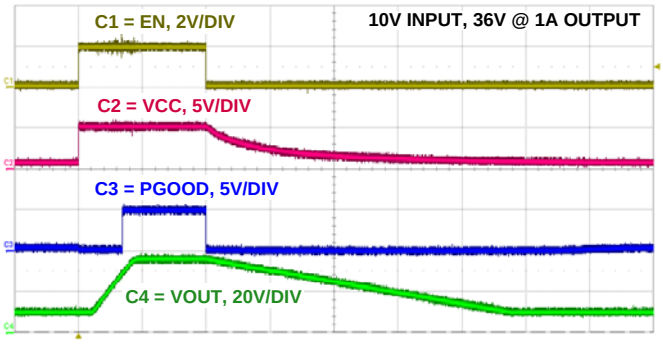


FIGURE 11. ENABLE/DISABLE WAVEFORMS

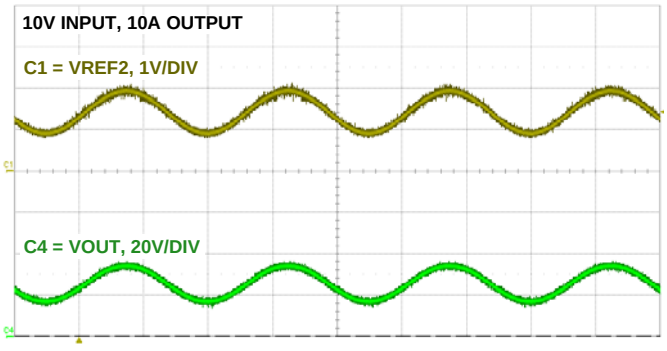


FIGURE 12. MODULATING VREF2 INPUT

Operation Description

Multiphase Power Conversion

The technical challenges associated with producing a single-phase converter that is both cost-effective and thermally viable for high power applications have forced a change to the cost-saving approach of multiphase solution. The ISL78225 controller helps reduce the complexity of implementation by integrating vital functions and requiring minimal output components.

Interleaving

The switching of each channel in a multiphase converter is timed to be symmetrically out-of-phase with each of the other channels. Take a 3-phase converter for example; each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the three-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor current is reduced in proportion to the number of phases (Equations 1 and 2). The increased ripple frequency and the lower ripple amplitude mean that the designer can use less per-channel inductance and lower total input and output capacitance for any performance specification.

Figure 13 illustrates the multiplicative effect on input ripple current. The three channel currents (I_{L1}, I_{L2}, and I_{L3}) combine to form the AC ripple current and the DC input current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is triggered 1/3 of a cycle after the start of the PWM pulse of the previous phase.

To understand the reduction of the ripple current amplitude in the multiphase circuit, examine the equation representing an individual channel's peak-to-peak inductor current.

In Equation 1, V_{IN} and V_{OUT} are the input and the output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

$$I_{PP} = \frac{(V_{OUT} - V_{IN})V_{IN}}{L f_S V_{OUT}} \quad \text{(EQ. 1)}$$

The input capacitors conduct the ripple component of the inductor current. In the case of multiphase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Reducing the inductor ripple current allows the designer to use fewer or less costly input capacitors.

$$I_{C(P-P)} = \frac{(V_{OUT} - N V_{IN})V_{IN}}{L f_S V_{OUT}} \quad \text{(EQ. 2)}$$

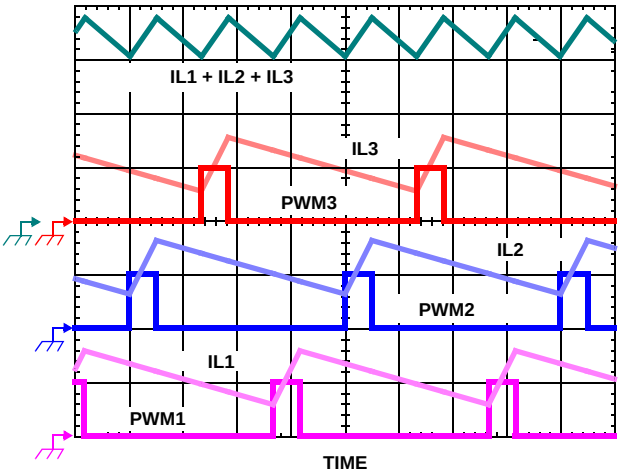


FIGURE 13. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

PWM Operations

The timing of each channel is set by the total number of active channels. The default channel setting for the ISL78225 is 4, and the switching cycle is defined as the time between PWM pulse initiation signals of each channel. The cycle time of the pulse initiation signal is the inversion of the switching frequency set by the resistor between the FS pin and ground. The PWM signals command the MOSFET drivers to turn on/off the channel MOSFETs.

In the default 4-phase operation, the PWM2 pulse starts 1/4 of a cycle after PWM1, the PWM3 pulse starts 1/4 of a cycle after PWM2, and the PWM4 pulse starts 1/4 of a cycle after PWM3.

Phase Selection

The ISL78225 can work in 2, 3, or 4-phase configuration. Connecting the PWM4 to VCC selects 3-phase operation and the pulse times are spaced in 1/3 cycle increments. Connecting the PWM3 to VCC selects 2-phase operation and the pulse times are spaced in 1/2 cycle increments. Unused current sense inputs must be left floating.

Modes of Operation

The different modes of operation will be determined by the voltage combinations of the MODE pin and the PWM_TRI pin.

If automatic phase adding/dropping function is not needed, the MODE pin should be tied to VCC (Logic HIGH). If higher light load efficiency is preferred, phase adding/dropping function could be implemented by connecting the MODE pin through a resistor to GND. A 5µA reference current will flow out of the MODE pin to generate corresponding V_{MODE}. V_{MODE} is used to compare with V_{IOUT} to determine the phase adding/dropping level.

When PWM_TRI is tied to GND (Logic LOW), the PWM outputs will be 2-levels (i.e., 0V and 5V). When PWM_TRI is pulled to VCC (Logic HIGH), apart from generating the 0V and 5V PWM signals, the PWM outputs can also generate 2.5V tri-level signal. The external driver can identify this tri-level signal and turn off both low side and high side output signals accordingly.

The truth table regarding V_{MODE} and V_{PWM_TRI} for different modes of applications is summarized as in Table 1.

TABLE 1. OPERATION MODE FOR DIFFERENT APPLICATIONS

CASE	MODE	PWM _TRI	EXTERNAL DRIVER IDENTIFY 2.5V TRI-LEVEL SIGNAL?	APPLICATIONS
A	1	1	Yes	Synchronous boost for audio amplifier power supply. No phase dropping.
B	Analog	1	Yes	Applications that need improving light load efficiency (automatic phase dropping + cycle-by-cycle diode emulation + pulse skipping).
C	1	0	No	Applications that the external driver cannot identify tri-level signal; no phase dropping.
D	Analog	0	No	Applications that the external driver cannot identify tri-level signal, with improved light load efficiency (e.g., 6-phase non synchronous boost with phase dropping).

Considerations for Audio Amplifier Power Supply Application

For multiphase boost converters used in audio amplifier applications, it is preferred to have the following features:

1. Automatic phase dropping function is NOT needed because the load is fast changing.
2. In car audio amplifier applications, the switching frequency is preferred to be fixed, such that it will not interfere with FM/AM band.
3. For synchronous boost, diode emulation is needed during start-up in order to prevent negative current dumping to the input side.
4. For synchronous boost, a maximum duty cycle limitation on the synchronous FET is preferred.

Based on the above mentioned “preferred features”, for audio amplifier applications, it does not need phase dropping/adding, but it needs a tri-state PWM signal if synchronous boost structure is used. Also, in order to limit the maximum duty cycle of the synchronous FET, the minimal turn on time of the active FET (Low side FET for boost structure) will be changed from fixed 130ns to variable time, which is 1/12 of the switching periods.

Operation Initialization Before Soft-Start

Prior to converter initialization, proper conditions must exist on the enable inputs (EN pin) and VCC pin. When both conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, V_{PGOOD} is asserted logic high.

Figure 14 shows the ISL78225 internal circuit functions before the soft-start begins.

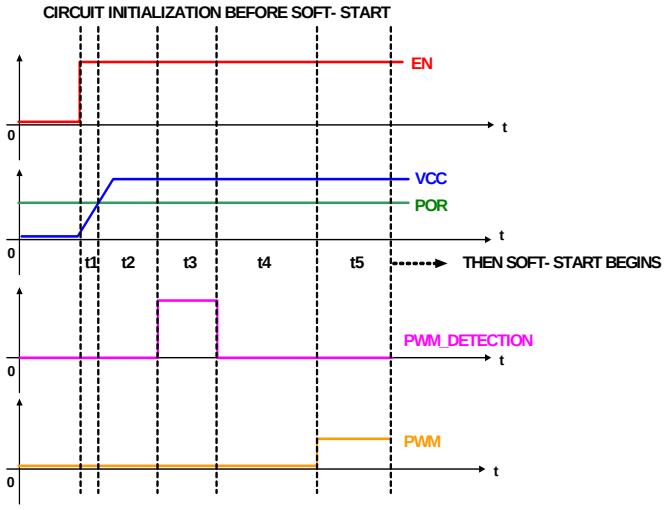


FIGURE 14. CIRCUIT INITIALIZATION BEFORE SOFT-START

As shown on Figure 14, there are 5 time intervals before the soft-start is initialized. They are specified as t_1, t_2, t_3, t_4 and t_5, respectively. The descriptions for each time interval are as follows:

Time t_1: The enable comparator holds the ISL78225 in shutdown until the V_{EN} rises above 1.2V at the beginning of t_1 time period. During t_1, V_{VCC} will gradually increase until it reaches the internal power-on reset (POR) rising threshold. Then the system enters t_2.

Time t_2: During t_2 time, the device initialization occurs. The time duration for t_2 is typically from 60µs to 100µs.

Time t_3: After the self-calibration finishes, the internal PWM detection signal will be asserted and the system enters the t_3 period. During t_3, the ISL78225 will detect the voltage on each PWM pin to determine the active phase number. If PWM1 or PWM2 is accidentally pulled to VCC, the chip will be latched off and wait for power recycling. The time duration for t_3 is fixed to around 30µs.

Time t_4: When the internal PWM detection signal is released, the system enters t_4 period. During t_4 period, the ISL78225 will wait until the internal PLL circuits are locked to the pre-set oscillator frequency. When PLL locking is achieved, the oscillator will generate output at the CLK_OUT pin. The time duration for t_4 is typically around 0.5ms, depending on the PLL_COMP pin configuration.

Time t_5: After the PLL locks the frequency, the system enters the t_5 period. During t_5, the PWM outputs are held in a high-impedance state (If V_{PWM_TRI} = 1) or logic low (if V_{PWM_TRI} = 0), and the V_{DRIVE_EN} is logic LOW to assure the external drivers remain off. The ISL78225 has one unique feature to pre-bias the V_{SS} based on V_{FB} information during this time. The duration time for t_5 is around 50µs.

After t_5, the soft-start process will begin. The following section will discuss the soft-start process in detail for different applications.

Soft-Start Process for Different Modes (Refer to Table 1)

Case A (V_{MODE} = VCC, V_{PWM_TRI} = VCC)

Figure 15 shows the pre-bias start-up PWM waveform for Case A in Table 1. The V_{PWM_TRI} = VCC so the PWM can output a tri-level signal, which the external drivers need to identify, and V_{MODE} = VCC to ban the automatic phase dropping function.

Time t_4, t_5: Same as the t_4, t_5 in Figure 14, soft-start has not started yet. See "Operation Initialization Before Soft-Start" on page 13 for a detailed description.

Time t_6: At the beginning of t_6, the SS pin has already been pre-biased to a value very close to the V_{FB}, so that the internal reference signal will start from the voltage close to the FB pin. This scheme will eliminate the internal delay for a non pre-biased application.

The DRIVE_EN pin, which is connected to the enable pins of the external drivers, will be pulled high when first PWM toggles at the beginning of t_6; as a result external drivers will start working. The PWM signals will switch between tri-level and low. The driver will only turn on the lower MOSFET accordingly, and the duty cycle will increase gradually from 0 to steady state. The synchronous MOSFET (Upper FET for Boost converter) will never turn on during this time, so diode emulation can be achieved during the start-up and in turn prevent negative current flowing from output to input.

Time t_7: Soft-start finishes at the beginning of t_7. The PWMs will change to a 2-level 0V to 5V switching signal and the synchronous MOSFET will be turned on.

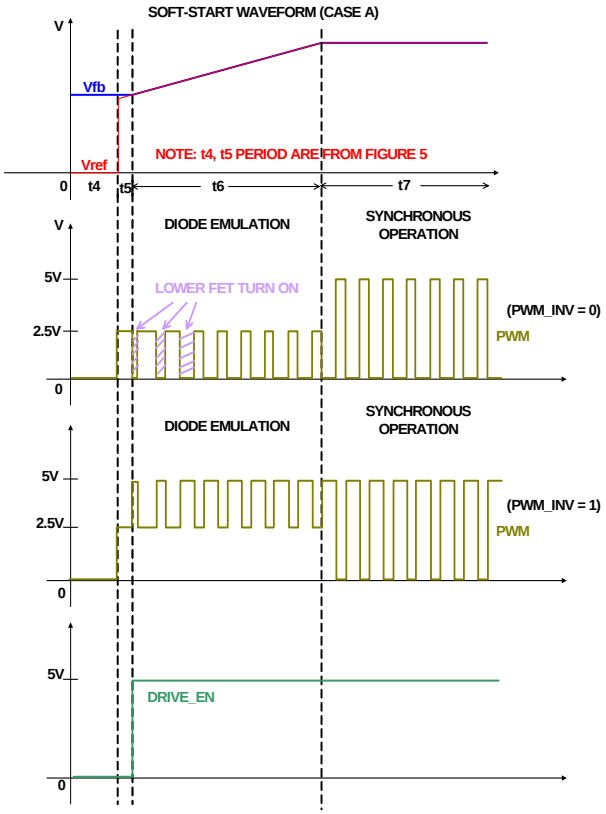


FIGURE 15. SOFT-START WAVEFORM (CASE A)

Case B (V_{MODE} < 4V, V_{PWM_TRI} = VCC, Light Load Condition)

The only difference between Case A and Case B start-up waveforms is that at light load, Case B can drop phases and have cycle-by-cycle diode emulation at PWM1 and PWM2.

For Case B applications, where good light load efficiency is always preferred, the ISL78225 provides three light load efficiency enhancement methods. When the load current reduces, the ISL78225 will first assert the automatic phase dropping function to reduce the active phase number according to the load level. The minimum active phase number is two. If the load current further reduces even when running at two-phase operation, the ISL78225 will assert a second method by utilizing cycle-by-cycle diode emulation. During this time the IC will sense the inductor current, and when the current is approximately zero, it will turn off the synchronous MOSFET. If the load current is further reduced to deep light load operation, pulse skipping function will kick in to optimize the overall efficiency.

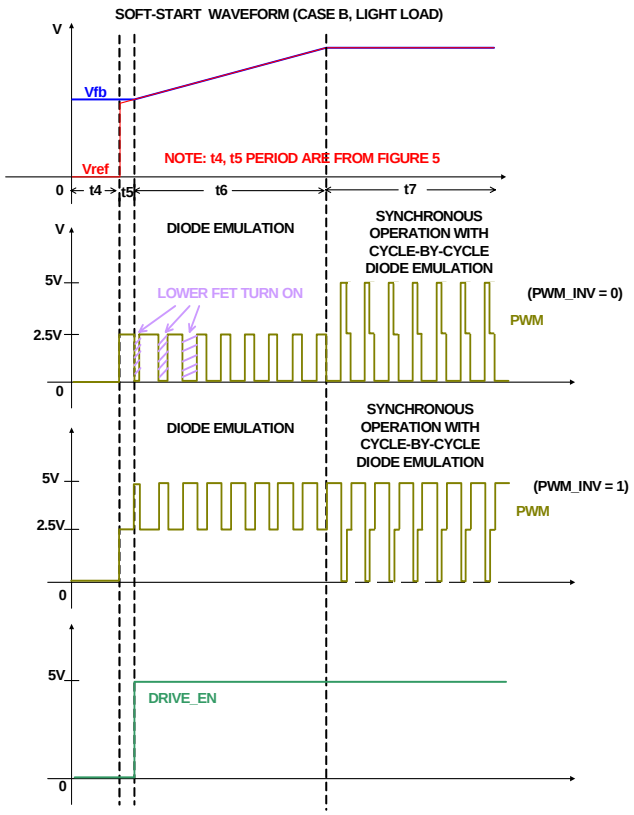


FIGURE 16. SOFT-START WAVEFORM (CASE B, LIGHT LOAD)

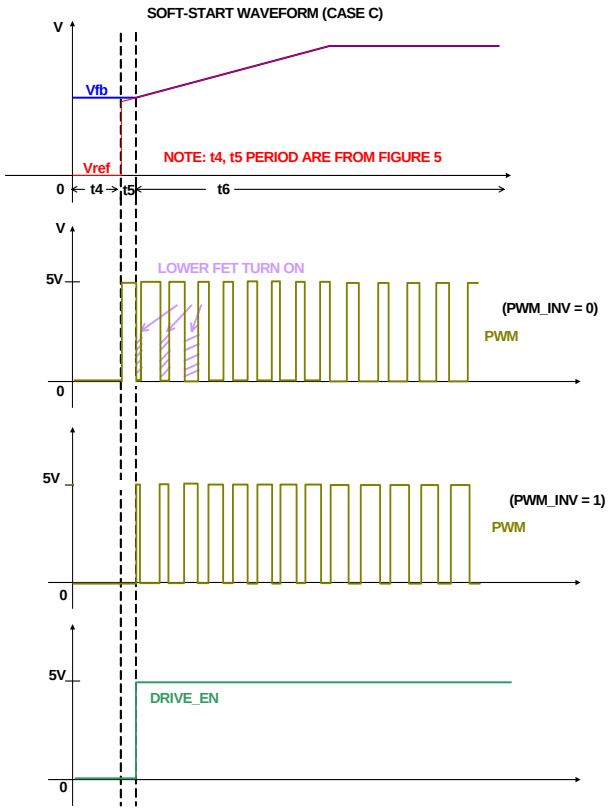


FIGURE 17. SOFT-START WAVEFORM (CASE C, LIGHT LOAD)

Case C (V_{PWM_TRI} = 0)

For applications that the driver cannot identify a tri-state PWM signal, the V_{PWM_TRI} should be connected to GND (Logic LOW), such that the PWM signal will only be 2 levels between 0V and 5V. Then the DRIVE_EN pin can be connected to the EN pin of the external drivers. DRIVE_EN will be asserted when the PWM first toggles such that the pre-bias start-up capability can be achieved. Detailed soft-start for Case C is shown in Figure 17.

Time t_4, t_5: Same as the t_4, t_5 in Figure 14, soft-start has not started yet; see "Operation Initialization Before Soft-Start" on page 13 for detailed description.

Time t_6: At the beginning of t_6, the PWM signal will start to switch between 0V and 5V. The driver will turn on the lower and upper MOSFETs accordingly, and the duty cycle for lower MOSFET will increase gradually from 0 to steady state. DRIVE_EN will be pulled high when the first PWM toggles at the beginning of t_6 to enable the external drivers.

Soft-Start Ramp Slew Rate Calculation

The soft-start ramp slew rate SR_{SS} is determined by the capacitor value C_{SS} from SS pin to GND. C_{SS} can be calculated based on Equation 3:

$$SR_{SS} = \frac{5 \times 10^{-12}}{C_{SS}} \left(\frac{V}{\mu s}\right) \quad \text{(EQ. 3)}$$

Figure 18 shows the relationship between C_{SS} and SR_{SS}.

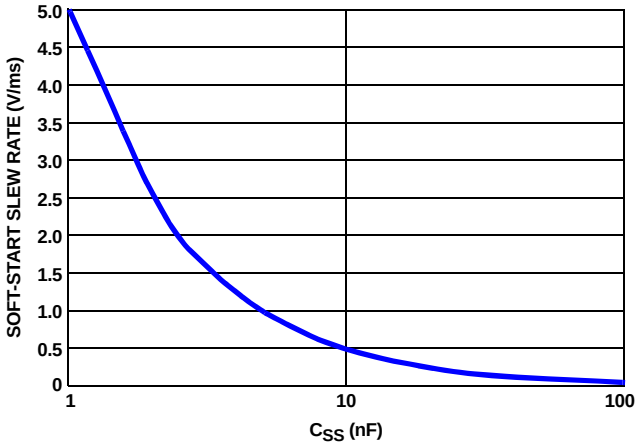


FIGURE 18. SOFT-START CAPACITOR vs SLEW RATE

Oscillator and Synchronization

The switching frequency is determined by the selection of the frequency-setting resistor, R_{FS}, connected from the FS pin to GND. Equation 4 is provided to assist in selecting the correct resistor value.

$$R_{FS} = 4X10^{10}\left(\frac{1}{f_{SW}} - 5X10^{-8}\right) \quad \text{(EQ. 4)}$$

Where f_{SW} is the switching frequency of each phase. Figure 19 shows the relationship between R_{FS} and switching frequency.

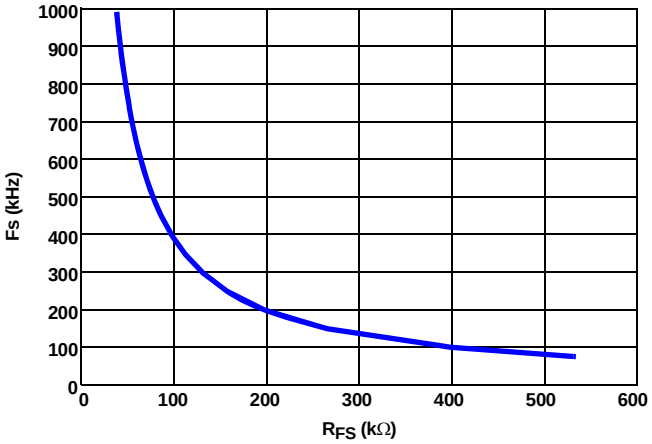


FIGURE 19. R_{FS} vs SWITCHING FREQUENCY

The maximum frequency at each PWM output is 1MHz. If the FS pin is accidentally shorted to GND or connected to a low impedance node, the internal circuits will detect this fault condition and fold back the switching frequency to the 75kHz minimal value.

The ISL78225 contains a phase lock loop (PLL) circuit and has frequency synchronization capability by simply connecting the SYNC pin to an external square pulse waveform (typically 20% to 80% duty cycle). In normal operation, the external SYNC frequency needs to be at least 20% faster than the internal oscillator frequency setting. The ISL78225 will synchronize its switching frequency to the fundamental frequency of the input waveform. The frequency synchronization feature will synchronize the rising edge of the PWM1 clock signal with the rising edge of the external clock signal at the SYNC pin.

The PLL is compensated with a series resistor-capacitor (Rc and Cc) from the PLL_COMP pin to GND and a capacitor (Cp) from PLL_COMP to GND. Typical values are Rc = 6.8kΩ, Cc = 6.8nF, Cp = 1nF. The typical lock time is around 0.5ms.

The CLK_OUT pin provides a square pulse waveform at the switching frequency. The amplitude is 5V with approximately 40% positive duty cycle, and the rising edge is synchronized with the leading edge of PWM1.

Current Sensing

The ISL78225 senses the current continuously for fast response. It supports both sense resistor and inductor DCR current sensing methods. The sensed current for each active channel will be used for loop control, phase current balance, individual channel overcurrent protection and total average current protection. The internal circuitry, (shown in Figures 20 and 21), represents a single channel. This circuitry is repeated for each channel, but may not be active depending on the status of the PWM3 and PWM4 pin voltage.

Peak current mode control is implemented by feeding back the current output of the current sense amplifier (CSA) to the regulator control loop. Individual channel peak current limit is implemented by comparing the CSA output current with 160µA. When the peak current limit comparator is tripped, the PWM ON-pulse is terminated and the IC is latched off.

Sense Resistor Current Sensing

A sense resistor can be placed in series with the power inductor. As shown in Figure 20, The ISL78225 acquires the channel current information by sensing the voltage signal across the sense resistor. Because the voltage on both the positive input and the negative input of the current sense amplifier (CSA) are forced to be equal, the voltage across R_{SET} is equivalent to the voltage drop across the R_{SEN} resistor. The resulting current into the ISENxP pin is proportional to the channel current, I_L. Equation 5 for I_{SEN} is derived where I_L is the channel current:

$$I_{SEN} = I_L \cdot \frac{R_{SEN}}{R_{ISET}} \quad \text{(EQ. 5)}$$

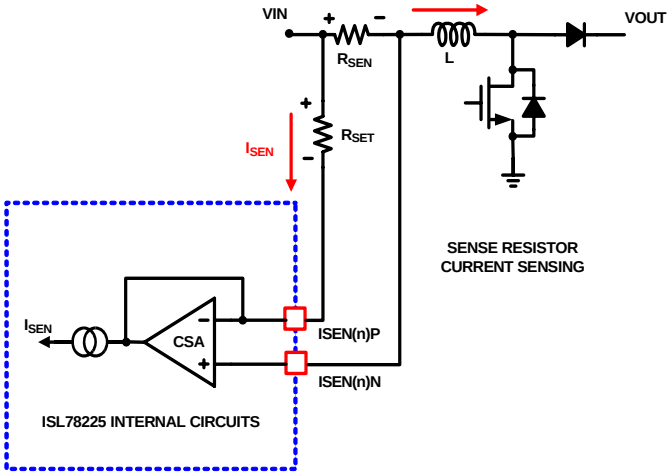


FIGURE 20. SENSE RESISTOR CURRENT SENSING

Inductor DCR Sensing

An inductor's winding is characteristic of a distributed resistance as measured by the DCR (Direct Current Resistance) parameter.

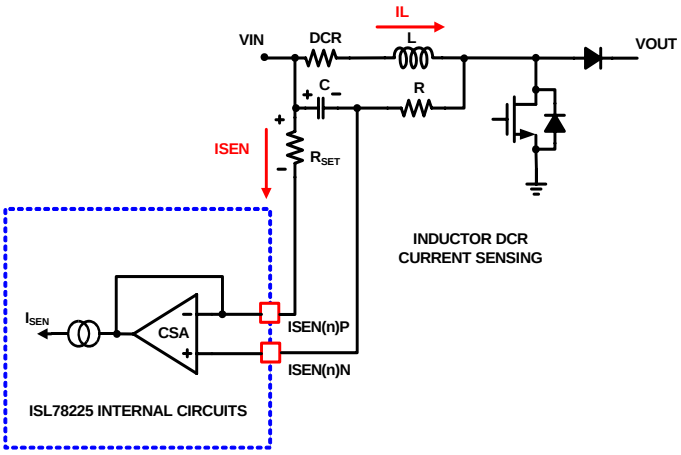


FIGURE 21. INDUCTOR DCR CURRENT SENSING

Consider the inductor DCR as a separate lumped quantity, as shown in Figure 21. The channel current I_L, flowing through the inductor, will also pass through the DCR. Equation 6 shows the s-domain equivalent voltage across the inductor V_L.

$$V_L = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 6)}$$

A simple R-C network across the inductor extracts the DCR voltage, as shown in Figure 21.

The voltage on the capacitor V_C, can be shown to be proportional to the channel current I_L, see Equation 7.

$$V_C = \frac{\left(s \cdot \frac{L}{DCR} + 1\right) \cdot (DCR \cdot I_L)}{(s \cdot RC + 1)} \quad \text{(EQ. 7)}$$

If the R-C network components are selected such that the RC time constant (= R*C) matches the inductor time constant (= L/DCR), the voltage across the capacitor V_C is equal to the voltage drop across the DCR, i.e., proportional to the channel current.

With the internal low-offset differential current sense amplifier, the capacitor voltage V_C is replicated across the sense resistor R_{SET}. Therefore, the current flow into the ISENxP pin is proportional to the inductor current. Equation 8 shows that the ratio of the channel current to the sensed current I_{SEN} is driven by the value of the sense resistor and the DCR of the inductor.

$$I_{SEN} = I_L \cdot \frac{DCR}{R_{SET}} \quad \text{(EQ. 8)}$$

Light Load Efficiency Enhancement Schemes

For switching mode power supplies, the total loss is related to both the conduction loss and the switching loss. At heavy load, the conduction loss is dominant while the switching loss will take charge at light load condition. So, if a multiphase converter is running at a fixed phase number for the entire load range, we will observe that below a certain load point, the total efficiency starts to drop heavily. The ISL78225 has automatic phase dropping, cycle-by-cycle diode emulation and pulse skipping features to enhance the light load efficiency. By observing the total input current on-the-fly and dropping the active phase numbers accordingly, the overall system can achieve optimized efficiency over the entire load range. All the previously mentioned light load enhancement features can be disabled by simply pulling the MODE pin to VCC.

Adjustable Automatic Phase Dropping/Adding at Light Load Condition

If the MODE pin is connected to a resistor to GND, and the voltage on the MODE pin is lower than its disable threshold 4V, the adjustable automatic phase dropping/adding mode will be enabled. When the ISL78225 controller works in this mode, it will automatically adjust the active phase number by comparing the V_{MODE} and V_{IOUT}, which represents sensed total current information. The V_{MODE} sets the overall phase dropping threshold, and the V_{IOUT} is proportional to the input current, which is in turn proportional to the load current. The smaller the load current, the lower the voltage observed on the IOUT pin, and the ISL78225 will drop phases in operation. Once the MODE pin voltage is fixed, the threshold to determine how many phases are in operation is dependent on two factors:

1. The maximum configured phase number.
2. The voltage on the IOUT pin (V_{IOUT}).

For example, if the converter is working in 4-phase operation and the MODE pin is set to 1.2V, the converter will monitor the V_{IOUT} and compared to 1.2V; if less than 900mV (75% of 1.2V), it will drop to 3-phase; if less than 600mV (50% of 1.2V), it will drop to 2-phase. The detailed threshold setting is shown in the "Electrical Specifications" table on page 7.

If PWM_TRI is tied to VCC, the dropped phase will provide a 2.5V tri-level signal at its PWM output. The external driver has to identify this tri-state signal and turn off both the lower and upper switches accordingly. For better transient response during phase dropping, the ISL78225 will gradually reduce the duty cycle of the phase from steady state to zero, typically within 15 switching cycles. This gradual dropping scheme will help smooth the change of the PWM signal and, in turn, will help to stabilize the system when phase dropping happens.

The ISL78225 also has an automatic phase adding feature similar to phase dropping, but when doing phase adding there will not be 15 switching cycles gradually adding. It will add phases instantly to take care of the increased load condition. The phase adding scheme is controlled by three factors.

1. The maximum configured phase number
2. The voltage on the IOUT pin (V_{IOUT}).
3. Individual phase current

Factors 1 and 2 are similar to the phase dropping scheme. If the V_{IOUT} is higher than the phase dropping threshold plus the hysteresis voltage, the dropped phase will be added back one by one instantly.

The previously mentioned phase-adding method can take care of the condition that the load current increases slowly. However, if the load is increasing quickly, the IC will use a different phase adding scheme. The ISL78225 monitors the individual channel current for all active phases. During phase adding, the system

will bring down the pre-set channel current limit to 2/3 of its original value (160µA). If any of the phase's sensed current hit the 2/3 of pre-set channel current limit threshold (i.e., 106.7µA), all the phases will be added back instantly. After a fixed 1.5ms delay, the phase dropping circuit will be activated and the system will react to drop the phase number to the correct value.

During phase adding, when either phase hits the pre-set channel current limit, there will be 200µs blanking time such that per-channel OCP will not be triggered during this blanking time.

Diode Emulation at Very Light Load Condition

When phase dropping is asserted and the minimum phase operation is 2 phases, if the load is still reducing and synchronous boost structure is used, the ISL78225 controller will enter into forced cycle-by-cycle diode emulation mode. The PWM output will be tri-stated when the inductor current falls to zero, such that the synchronous MOSFET can be turned off accordingly cycle-by-cycle for forced diode emulation. This cycle-by-cycle diode emulation scheme will only be asserted when two conditions are met:

1. The PWM_TRI pin voltage is logic HIGH.
2. Only two phases are running either by phase dropping or initial configuration.

By utilizing the cycle-by-cycle diode emulation scheme in this way, negative current is prevented and the system can still optimize the efficiency even at very light load conditions.

Pulse Skipping at Deep Light Load Condition

If the converter enters diode emulation mode and the load is still reducing, eventually pulse skipping will occur to increase the deep light load efficiency.

Adjustable Slope Compensation

For a boost converter working in current mode control, slope compensation is needed when steady state duty cycle is larger than 50%. When slope compensation is too low, the converter can suffer from jitter or oscillation. On the other hand, over compensation of the slope will cause the reduction of the phase margin. Therefore, proper design of the slope compensation is needed.

The ISL78225 features adjustable slope compensation by setting the resistor value R_{SLOPE} from the SLOPE pin to GND. This function will ease the compensation design and provide more flexibility in choosing the external components.

For current mode control, typically we need the compensation slope m_A to be 50% of the inductor current down ramp slope m_B when the lower MOSFET is off. Equation 9 shows how to choose the suitable resistor value.

$$R_{SLOPE} = \frac{1.136 \times 10^6 \times L \times R_{SET}}{(V_{OUT} - V_{IN})(R_{SEN})}(\Omega) \quad \text{(EQ. 9)}$$

Fault Monitoring and Protection

The ISL78225 actively monitors input/output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to the load. Common power-good indicator pin (PGOOD pin) and VIN_OVB, VOUT_OVB pins are provided for linking to external system monitors.

PGOOD Signal

The PGOOD pin is an open-drain logic output to indicate that the soft-start period is completed and the output voltage is within the specified range. This pin is pulled low during soft-start and releases high after a successful soft-start. PGOOD will be pulled low when a UV/OV/OC/OT fault occurs.

Input Overvoltage Detection

The ISL78225 utilizes VIN_SEN and VIN_OVB pins to deal with a high input voltage. The VIN_SEN pin is used for sensing the input voltage. A resistor divider network is connected between this pin and the boost power stage input voltage rail. When the voltage on VIN_SEN is higher than 2.4V, the open drain output VIN_OVB pin will be pulled low to indicate an input overvoltage condition, The V_{IN} overvoltage sensing threshold can be programmed by changing the resistor values, and hysteresis voltage of the internal comparator is fixed to be 100mV.

Output Undervoltage Detection

The undervoltage threshold is set at 80% of the internal voltage reference. When the output voltage at the FB pin is below the undervoltage threshold minus the hysteresis, PGOOD is pulled low. When the output voltage comes back to 80% of the reference voltage, PGOOD will return back to high.

Output Overvoltage Detection/Protection

The ISL78225 overvoltage detection circuit is active after time t_2 in Figure 14 on page 13. The OV trip point is set to 120% of the internal reference level. Once an overvoltage condition is detected, the PGOOD will be pulled low but the controller will continue to operate.

The ISL78225 also provides the flexibility for output overvoltage protection by utilizing the VOUT_SEN and VOUT_OVB pins. The VOUT_SEN pin is used for sensing the output voltage. A resistor divider network is connected between this pin and the boost power stage output voltage rail. When the voltage on VOUT_SEN is higher than 2.4V, the open drain output VOUT_OVB will be pulled low, and the ISL78225 IC will be latched off to indicate an output overvoltage condition. The V_{OUT} overvoltage sensing threshold can be programmed by changing the resistor values.

Overcurrent Protection

ISL78225 has two levels of overcurrent protection. Each phase is protected from an overcurrent condition by limiting its peak current, and the combined total current is protected on an average basis.

For the individual channel overcurrent protection, the ISL78225 continuously compares the CSA output current of each channel with a 160µA reference current. If any channel's current trips the current limit comparator, the ISL78225 will be shut down.

However, during the phase adding period, the individual channel current protection function will be blanked for 200µs, in order to give other phases the chance to take care of the current.

The IOUT pin serves for both input current monitoring and total average current OCP functions. The CSA output current for each

channel is scaled and summed together at this pin. An RC network should be connected between the IOUT pin and GND, such that the ripple current signal can be filtered out and converted to a voltage signal to represent the averaged total input current. The relationship between total input current I_{IN} and V_{IOUT} can be calculated as Equation 10 (see Figure 20 on page 16 for R_{SEN} and R_{SET} positions):

$$V_{IOUT} = 0.75 I_{IN} \frac{R_{SEN}}{R_{SET}} R_{IOUT} \quad \text{(EQ. 10)}$$

When the V_{IOUT} is higher than 2V for a consecutive 100µs, the ISL78225 IC will be triggered to shut down. This provides additional safety for the voltage regulator.

Equation 11 can be used to calculate the value of the resistor R_{IOUT} based on the desired OCP level $I_{AVG, OCP2}$.

$$R_{IOUT} = \frac{2}{I_{AVG, OCP2}} \quad \text{(EQ. 11)}$$

The total average overcurrent protection scheme will not be asserted until the soft-start pin voltage V_{SS} reaches its clamped value (approximately 3.5V). During the soft-start time, the system does not latch-off if per-channel or overall OC limit is reached. Instead, the individual channel current will run at its pre-set peak current limit level.

Thermal Protection

The ISL78225 will be disabled if the die junction temperature reaches a nominal of +160°C. It will recover when the junction temperature falls below a +15°C hysteresis. The +15°C hysteresis insures that the device will not be re-enabled until the junction temperature has dropped to below about +145°C.

Internal 5V LDO Output Current Limit Derating Curves

ISL78225 contains an internal 5V/200mA LDO, and the input of LDO (VIN pin) can go as high as 40V. Based on the junction to ambient thermal resistance R_{JA} of the package, we need to guarantee that the maximum junction temperature should be below +125°C T_{MAX}. Figure 22 shows the relationship between maximum allowed LDO output current and input voltage. The curve is based on +35°C/W thermal resistance R_{JA} for the package. Each curve represents different ambient temperature, T_A.

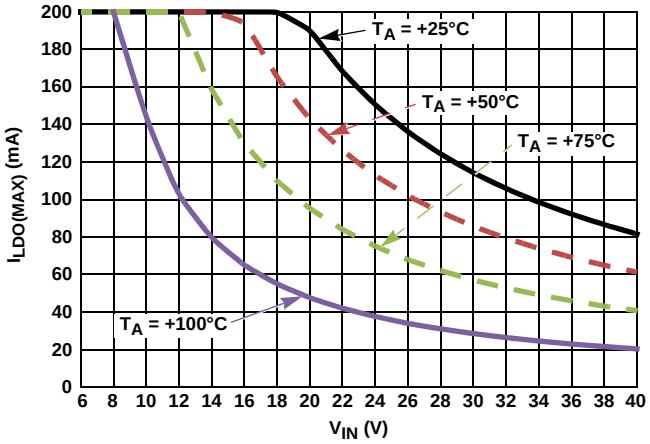


FIGURE 22. $I_{LDO(MAX)}$ vs V_{IN}

Dedicated VREF2 Pin for Input Voltage Tracking

A second reference input pin, VREF2, is added to the input of the transconductance amplifier. The ISL78225 internal reference will automatically change to VREF2 when it is pulled below 1.8V. The VREF2 pin can be connected to VIN through resistor network to implement the automatic input voltage tracking function. This function is very useful under car battery voltage cranking conditions (such as when the car is parked and the driver is listening to the stereo), where the full load power is typically not needed. In this case, the ISL78225 can limit the output power by allowing the output voltage to track the input voltage. If VREF2 is not used, the pin should be connected to VCC.

Configurations for Dual IC Operations

For high power applications, two ISL78225 ICs can be easily configured to support 8-phase operation. The IC that provides the CLK_OUT signal is called master IC, and the IC that received the CLK_OUT signal is called slave IC. Note that the two PWM1 signals are synchronized and the net effect is 4-phase operation with double the output current.

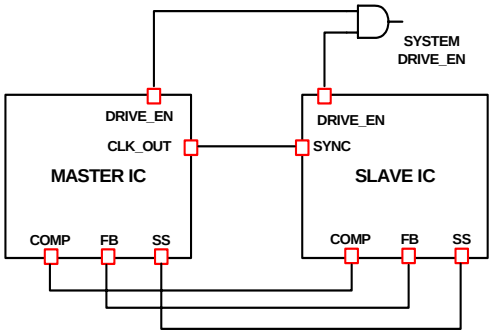


FIGURE 1. CONFIGURATIONS FOR DUAL IC OPERATION

Figure 1 shows the step-by-step setup as follows:

1. Connect the CLK_OUT pin of the master IC to the SYNC pin of the slave IC.
2. Set the master IC's switching frequency as desired frequency; set the slave IC's switching frequency 20% below the master IC's.
3. Connect both IC's COMP, SS and FB pins together.
4. Both IC's DRIVE_EN pin should be ANDed together to provide the system's driver enable signal.
5. Since PGOOD, VOUT_OVB and VIN_OVB pins are open drain structure, both IC's PGOOD, VOUT_OVB and VIN_OVB pins can be tied together and use one pull-up resistor to connect to VCC.
6. If Phase dropping function is needed, tie both IC's IOUT and MODE pins together.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
December 15, 2011	FN7909.0	Initial release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL78225

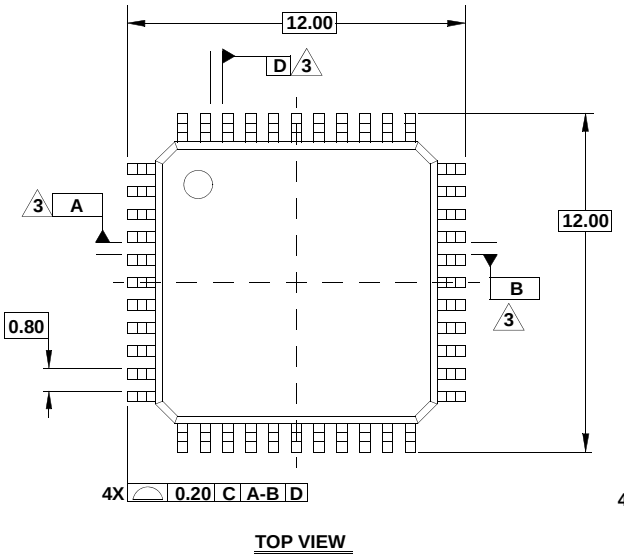
To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/search.php

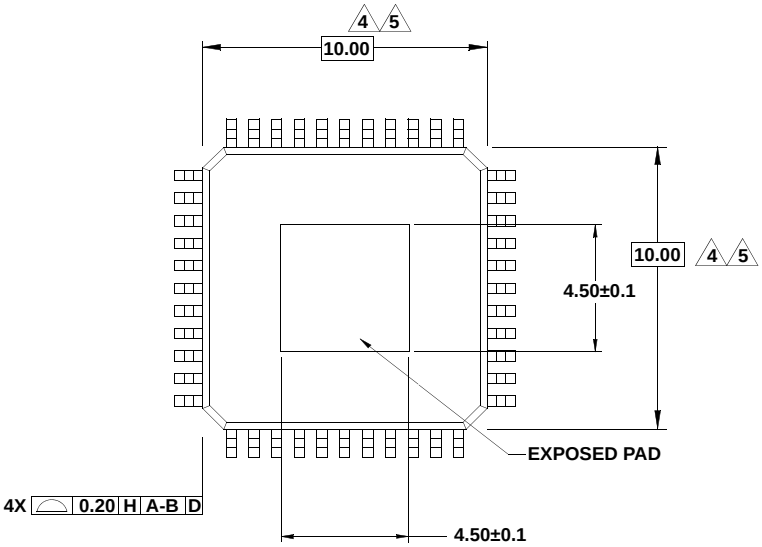
Package Outline Drawing

Q44.10x10A

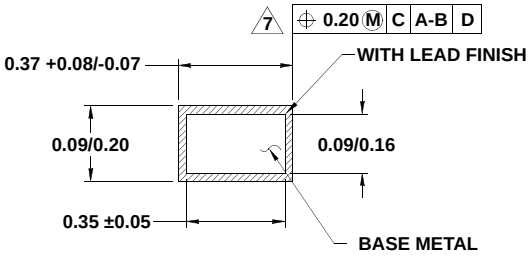
44 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE WITH EXPOSED PAD (EP-TQFP)
Rev 2, 12/10

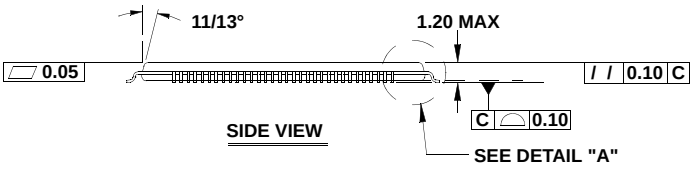


TOP VIEW

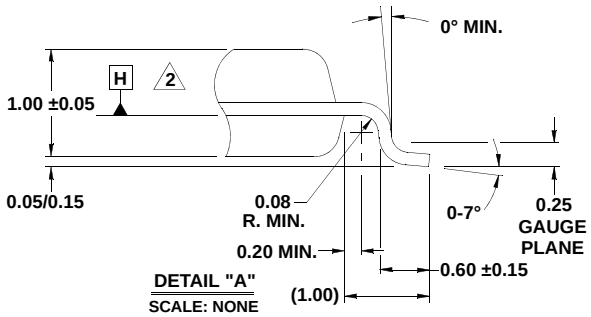


BOTTOM VIEW

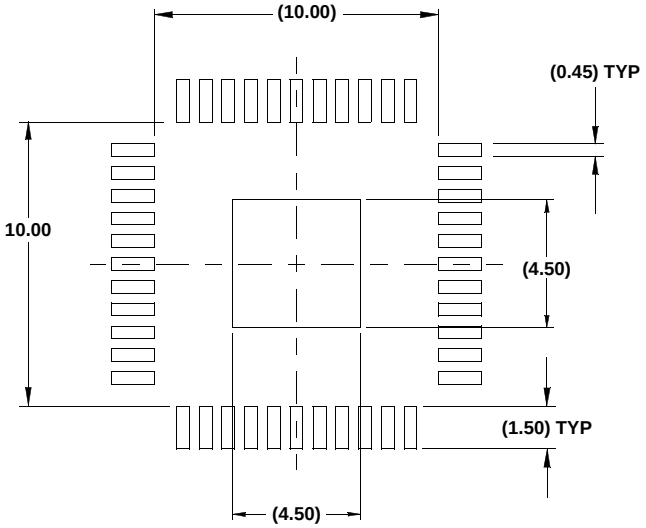




SIDE VIEW



DETAIL "A"
SCALE: NONE



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at centerline between leads where leads exit plastic body at datum plane H.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254mm on D1 and E1 dimensions.
5. These dimensions to be determined at datum plane H.
6. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
7. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
8. Controlling dimension: millimeter.
9. This outline conforms to JEDEC publication 95 registration MS-026, variation ACB.
10. Dimensions in ( ) are for reference only.
11. The corners of the exposed heatspreader may appear different due to the presence of the tiebars.