FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 10480-15
MBM 10480-25

September 1984
Edition 3.0

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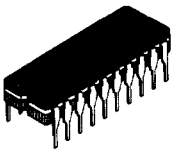
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10480 is fully decoded 16384-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by one bit, and it features on-chip voltage compensation for improved noise margin.

The MBM 10480 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 10480 is specified over a temperature range of from 0°C to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 20-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10K-series ECL families.

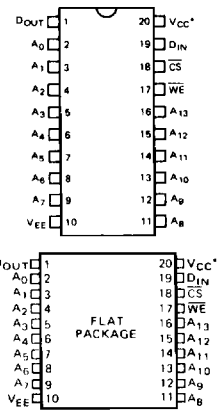
- 16384 words x 1 bit organization
- On-chip voltage compensation for improved noise margin.
- Fully compatible with industry-standard 10K-series ECL families
- Address access time : 15 ns max. (MBM 10480-15)
  : 25 ns max. (MBM 10480-25)
- Chip select access time : 8 ns max. (MBM 10480-15)
  : 10 ns max. (MBM 10480-25)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.05 mW/bit
- DOPOS and IOP-II
- Pin compatible with the F10480



CERAMIC PACKAGE
DIP-20C-C03

CERAMIC PACKAGE
FPT-20C-C01
LCC-20C-F01: See Page 11

PIN ASSIGNMENT



*V_{CC} grounded

LCC PAD CONFIGURATION: See Page 11

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

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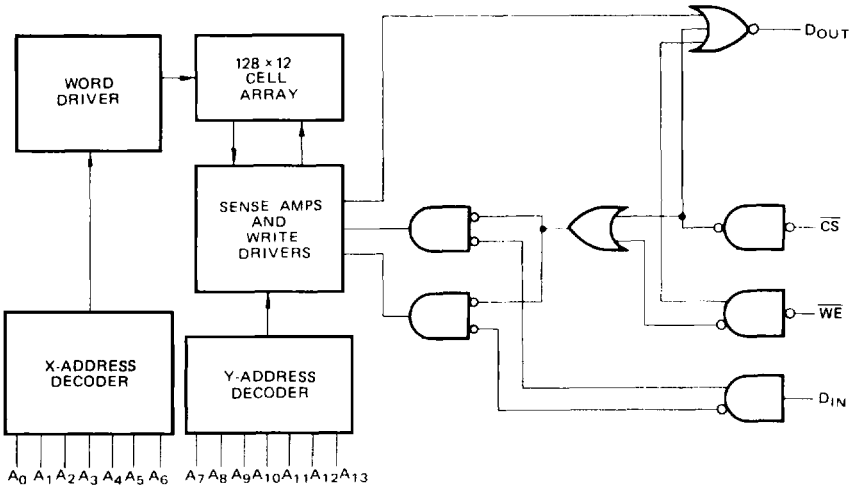
Fig. 1 – MBM 10480 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10480 is fully decoded 16384 bit read/write random access memory organized as 16384 words by one bit. Memory cell selection is achieved by means of a 14-bit address designated A_0 through A_{13}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data in D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-or connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V, Output Load = 50Ω and 30pF to -2.0V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Output Open) MBM 10480-15	I_{EE}	-220			mA	0°C to 75°C
Power Supply Current (All Inputs and Output Open) MBM 10480-25	I_{EE}	-200			mA	0°C to 75°C

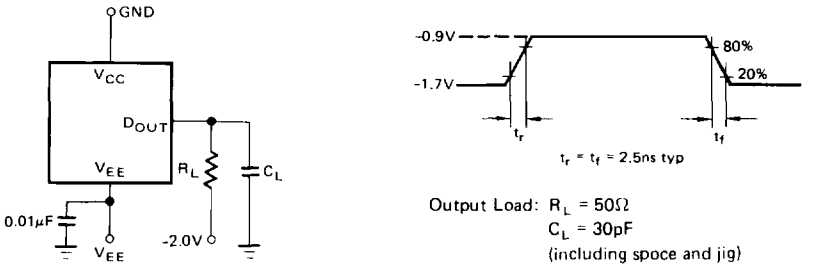
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		5		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC}=0V, V_{EE}=-5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, T_A=0°C to 75°C for DIP, Airflow ≧ 2.5m/s, T_C=0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS



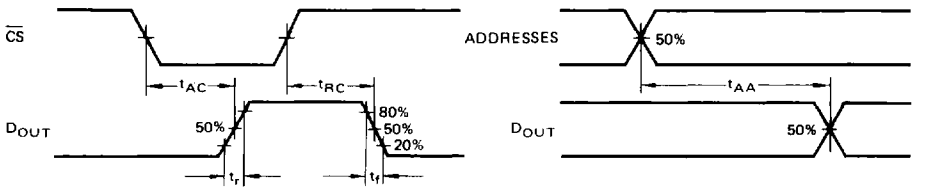
Output Load: R_L = 50Ω
C_L = 30pF
(including spoce and jig)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 10480-15			MBM 10480-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			15			25	ns
Chip Select Access Time	t_{AC}			8			10	ns
Chip Select Recovery Time	t_{RC}			8			10	ns

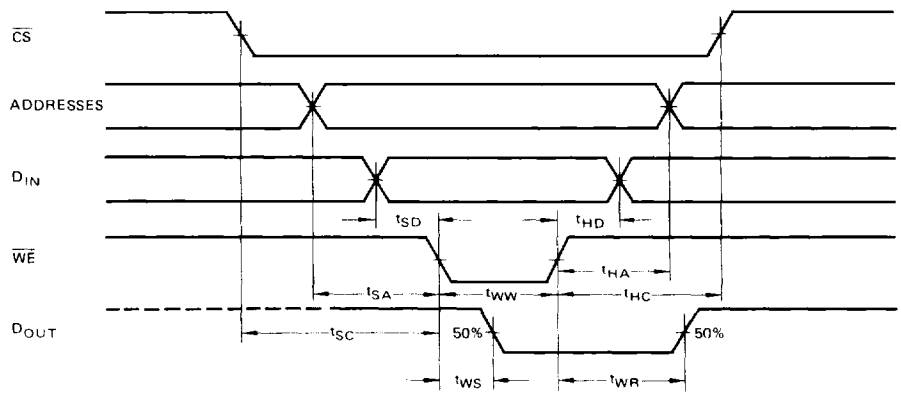
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	MBM 10480-15			MBM 10480-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	15			25			ns
Write Disable Time	t_{WS}			8			10	ns
Write Recovery Time	t_{WR}			18			20	ns
Address Set Up Time	t_{SA}	2			5			ns
Chip Select Set Up Time	t_{SC}	2			5			ns
Data Set Up Time	t_{SD}	2			5			ns
Address Hold Time	t_{HA}	3			5			ns
Chip Select Hold Time	t_{HC}	3			5			ns
Data Hold Time	t_{HD}	3			5			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		3		ns
Output Fall Time	t_f		3		ns

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

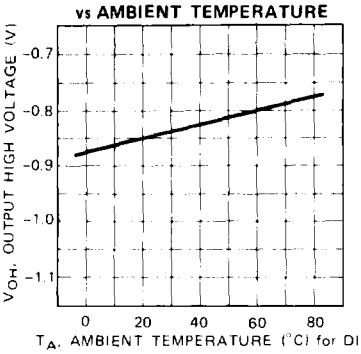


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

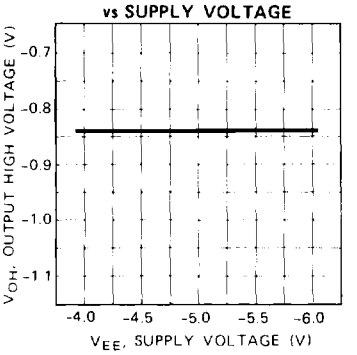


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

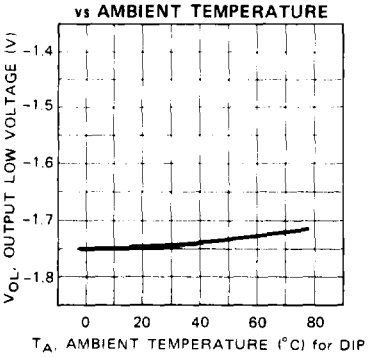


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

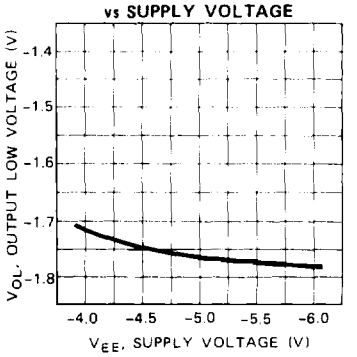


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

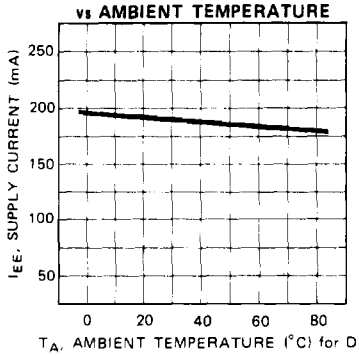


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

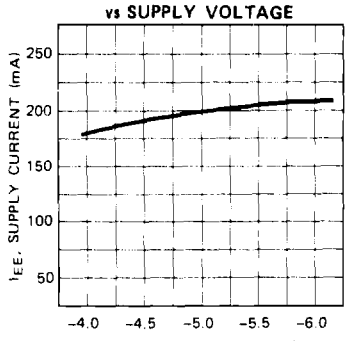


Fig.9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

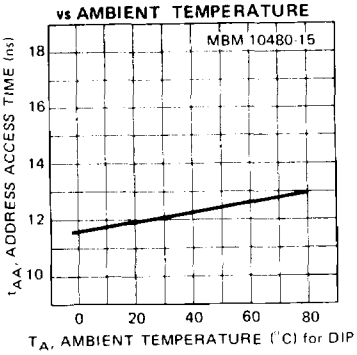


Fig. 10 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

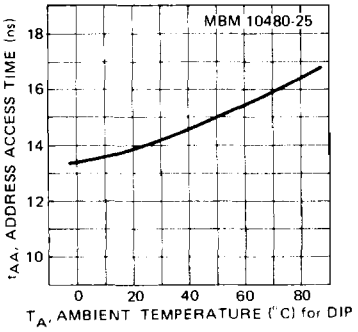


Fig.11 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

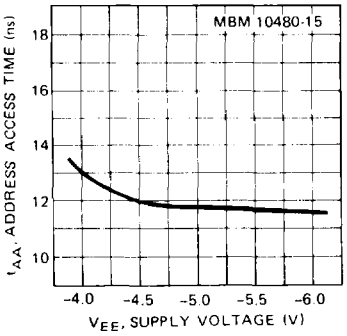


Fig. 12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

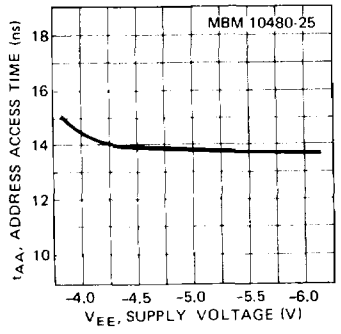


Fig.13 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

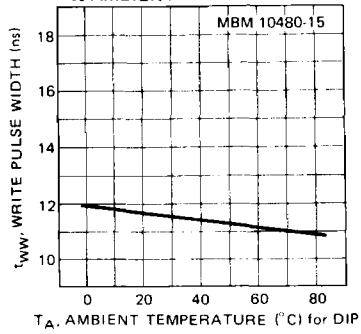


Fig. 14 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

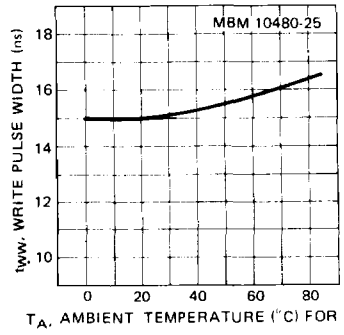


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Fig.15 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

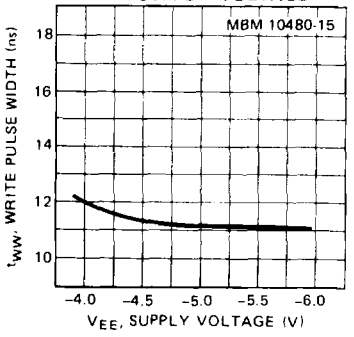
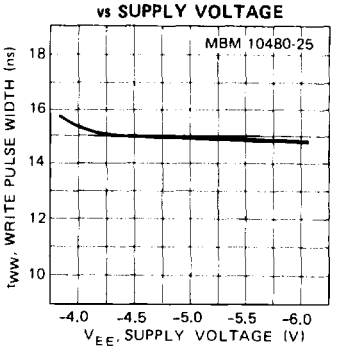
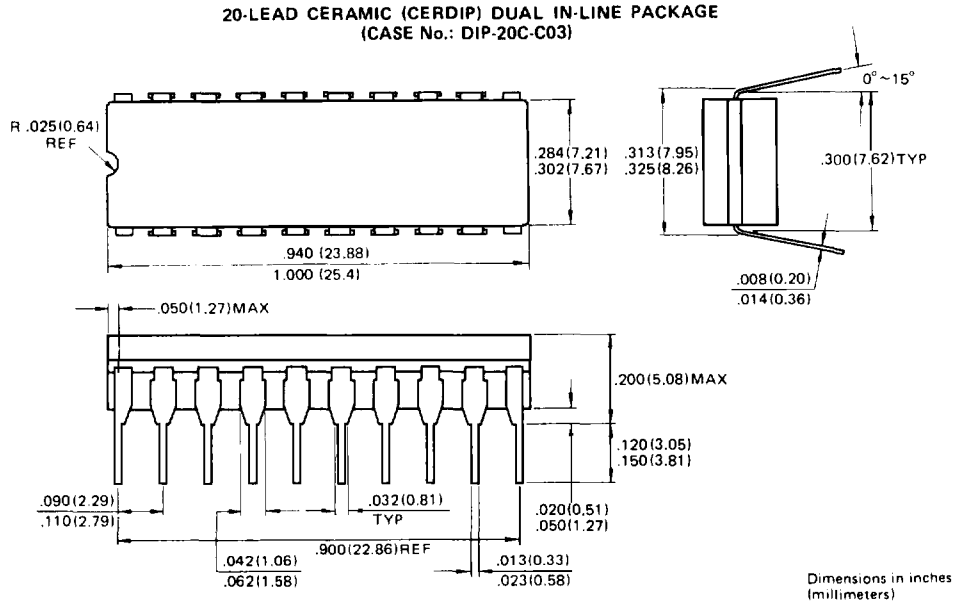


Fig. 16 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



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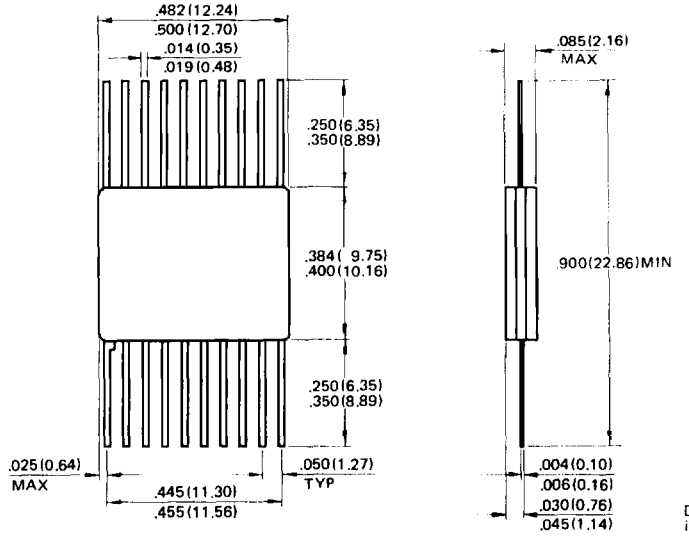
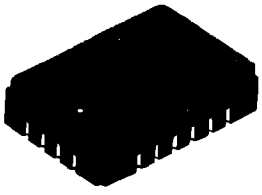
PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-20C-C01)



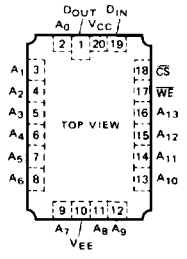
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

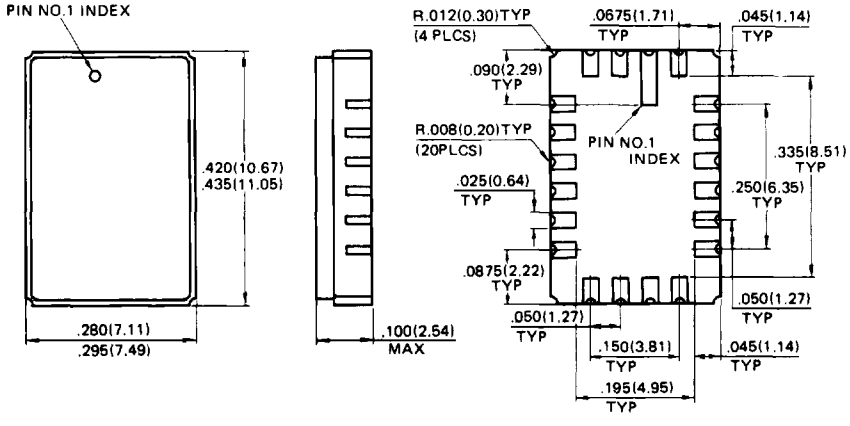


LCC-20C-F01

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



Dimension in
inches (millimeters)