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AP1601

LED light control IC, dimmer compatible

DESCRIPTION

The AP1601 is a control IC which is suitable for LED lighting applications to supply a current to LEDs from an AC power source. The AP1601 can be configured as a DCM isolated flyback circuit or as a CCM non-isolated step down chopper circuit (Buck converter). Also, LED lighting applications for a phase control dimmer (hereinafter called TRIAC dimmer) can be constructed with fewer external components on the application board.
Many functions for LED lighting applications are integrated into the AP1610 such as: 30V pre-driver, TRIAC dimmer control circuit, constant current circuit using the auxiliary winding of the transformer, noise reduction circuit during DCM operation and various protection functions.
The AP1601A also has an independent analog dimming pin and a PWM dimming pin for non-TRIAC dimming systems, providing a low cost LED application with a wide range of dimming configurations.

FEATURES

- LED driver with reduced external component count.
  - Constant current control using auxiliary winding of transformer. (no photo-coupler is required)
- Rectified AC voltage up to 275V can be applied for start-up / Start up by rectified AC voltage up to 275V.
- Current control functions
  - DCM flyback: Control with switching frequency changed by peak current on primary side and forward voltage of LEDs.
  - CCM chopper (Buck): Control with off-time changed by peak current on primary side and forward voltage of LEDs.
  - Analog dimming by external DC input. (Current peak control)
  - PWM dimming by external pulse input.
- TRIAC dimmer compatible, Built in current supply circuit
- Protection circuits
  - LED open protection.
  - Over current protection when transformer is shorted.
  - Under voltage lockout. (UVLO)
  - Thermal protection.
- Package
  - 14pin SOP.

APPLICATION

- Indoor LED lights up to 40W maximum
  - LED down light.
  - LED bracket.
  - LED ceiling light.

BLOCK DIAGRAM

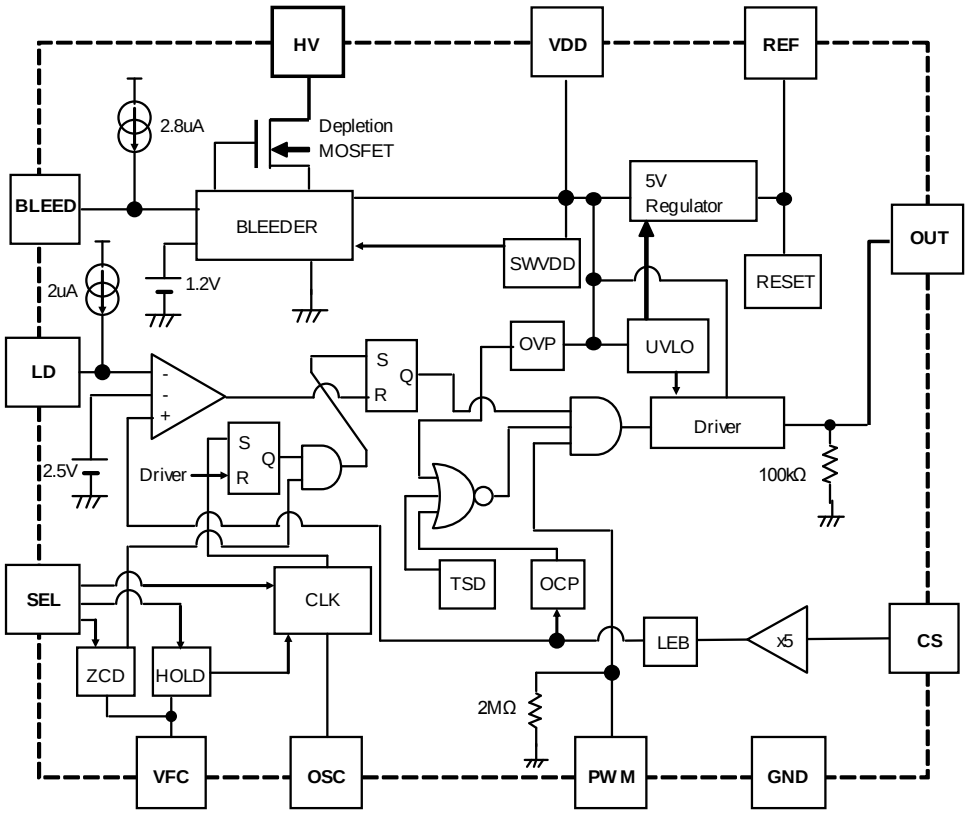


Figure 1. AP1601 Block diagram

Block	Description
BLEEDER	By monitoring the BLEED pin voltage and SWVDD condition, a bleed from HV pin or VDD charge ON/OFF is controlled.
5V Regulator	5V for internal circuits is generated from VDD pin.
SWVDD	By monitoring VDD pin voltage and if VDD voltage is deficient, a signal to BLEEDER is output.
RESET	By monitoring 5V regulator startup condition, malfunction of internal circuits using 5V is prevented.
UVLO	By monitoring VDD pin voltage, Driver output is held to GND level and 5V regulator is inactivated so that malfunction at low voltage is prevented.
OVP	Over voltage detection circuit on VDD pin.
Driver	Driver for external N type MOSFET.
TSD	Overheat detection circuit.
OCP	Over current detection circuit for external MOSFET.
CLK	Internal clock / Off-time generation circuit.
ZCD	Bottom voltage detection circuit.
HOLD	By sampling the auxiliary winding voltage, which is proportional to the Vf of the LEDs, a internal voltage is generated, which compensates for the CLK frequency on DCM or the off-time on CCM.
LEB	Leading edge blank circuit

PIN CONFIGURATION/DESCRIPTION

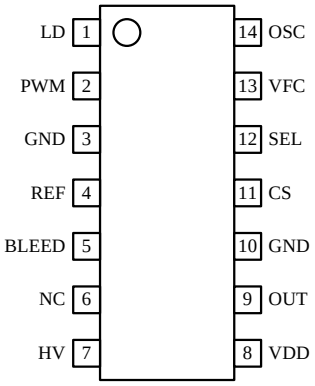


Figure 2. Pin Configuration of AP1601

No.	Pin	I/O	Description
1	LD	I	Analog dimming signal input pin Built in pull-up circuit (pulled by 2uA(typ) current source)
2	PWM	I	PWM dimming signal input pin Built in pull-down resistor (2MΩ(typ))
3,10	GND	PWR	IC ground pin This pin is connected to the frame for heat transfer.
4	REF	O	Internal regulator output pin For stability, please connect a capacitor of 0.1uF.
5	BLEED	I	Threshold set pin of the current source for TRIAC dimmer. While VBLEED pin voltage is less than (1.2V(typ)), a signal is sent to the internal control circuit. Built in pull-up circuit. (pulled by 2.8uA(typ) current source)
6	NC	-	NC pin Please do not connect to any pins. This pin is open.
7	HV	I	Current source pin for TRIAC dimmer. Provide a current to GND to prevent malfunction of TRIAC dimmer operation. During start up and when the external power supplied to VDD is deficient, the power supplied to the VDD pin has priority over the BLEED control signal.
8	VDD	PWR	IC power input pin. For voltage stability, please connect a capacitor from 1uF to 10uF.
9	OUT	O	Gate drive pin for external MOSFET. 1nF capacitor can be charged in 50ns(typ). Built in pull down resistor (100kΩ(typ)).
11	CS	I	External MOSFET current detection pin. Peak current is set connecting resistor between the source pin and GND. This pin also detects over current.
12	SEL	I	Fixed frequency mode / Fixed off-time mode switch pin.
13	VFC	I	Switching frequency/ Off-time compensation input pin. This pin also detects bottom voltage (when SEL=REF)
14	OSC	O	Switching frequency / Off-time set pin Resistor should be connected to GND (details are described later)

* (I/O) I: Input pin, O: Output pin, PWR: Power pin, -: N/A

ABSOLUTE MAXIMUM RATINGS

Ta=25°C unless otherwise specified.

Parameter	Symbol	Min.	Max.	Unit
HV (*1)	V_{HV_max}	-0.3	450	V
VDD (*1)	V_{DD_max}	-0.3	30	V
BLEED, OUT (*1,*2)	V_{MV_max}	-0.3	V_{DD_max}+0.3	V
REF (*1)	V_{REF_max}	-0.3	6.0	V
CS, PWM, LD, OSC, VFC, SEL (*1,*3)	V_{LV_max}	-0.3	V_{REF_max}+0.3	V
Junction Temperature	Tj	-40	125	°C
Storage Temperature	Tstg	-55	150	°C
Power Dissipation (*4)	P_D		1.5	W

Note:

*1 All voltages refer to GND pin (GND) as zero (reference) voltage.

*2 If VDD_max exceeds 29.7V, the maximum value is limited to 30V.

*3 If VREF_max exceeds 5.7V, the maximum value is limited to 6V.

*4 25.4mm×25.4mm×1.6 mm FR4 board, 50% GND copper area, Ta=25°C. PD must be decreased at the rate of 15mW/°C for operation above 25°C

The maximum ratings are the absolute limitation values with the possibility of damaging the IC.
When the operation exceeds these standards the specifications cannot be guaranteed.

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage Range (*5,*6)	V_{DD}	10		20	V
HV Voltage (*5)	V_{HV}			400	V
BLEED, CS, PWM, LD, OSC, VFC, SEL(*5)		GND		V_{REF}	V
Operating Temperature Range (*7)	Ta	-40		105	°C

*5 All voltages refer to GND pin (GND) as zero (reference) voltage.

*6 VDD is applied after UVLO is released. (UVLOH ： 17.6V(typ))

*7 In high power applications or low thermal conductivity of the application board or if both are true, the maximum ambient temperature value needs to be lowered not to exceed maximum Tj value.

ELECTRICAL CHARACTERISTICS

Ta=25°C, HV=open, VDD=15V, REF=0.1uF, PWM=VREF, SEL=GND, R15=200kΩ, VFC=VREF unless otherwise specified.
VDD is applied after UVLO is released, which is after the HV voltage (18V typical) is applied.

1. Supply Current

Parameter	Symbol	Specification			Unit	Note
		MIN	TYP	MAX		
Supply Current	I_{DD1}		2.0	3.0	mA	PWM=VREF CS=0.6V OUT=No Load (*8)
	I_{DD2}		1.4	2.1	mA	PWM=0V (*8)

2. Control circuits

Parameter	Symbol	Specification			Unit	Note
		MIN	TYP	MAX		
Operating mode						
SEL voltage H	VSELH	4.5			V	Fixed frequency mode, Bottom voltage detection (DCM)
SEL voltage L	VSELL			0.5	V	Fixed off-time mode(CCM)
Current control						
CS pin control voltage	V_{PEAK}	475	500	525	mV	LD=VREF
Leading edge blank	T_{LEB}	200	300	450	ns	PWM=VREF, CS=0.6V
LD pin input voltage	V_{LD}	0.3		2.65	V	LD pin input voltage range while analog dimming
	V_{LD2}	3.0			V	Analog dimming unused
PWM voltage H	VPWMH	1.5			V	Switching operation
PWM voltage L	VPWML			0.5	V	Cease switching
Switching frequency 1	F_{OP1}	95	100	105	kHz	R15=100kΩ, VVFC=1V, SEL=VREF (DCM)
Switching frequency 2	F_{OP2}	135	150	165	kHz	R15=100kΩ, VVFC=1.5V, SEL=VREF (DCM)
Switching frequency 3	F_{OP3}	40	50	60	kHz	R15=100kΩ, VVFC=0.5V, SEL=VREF (DCM)
Off-time	T_{OSC}	9	10	11	us	R15=100kΩ, VVFC=1V, SEL=GND (CCM)
VFC zero cross detection voltage	V_{THZC}	0.05	0.1	0.15	V	SEL=VREF (DCM)
Gate drive						
OUT pin output voltage H	V_{OUTH}	VDD-0.3	VDD-0.18	VDD-0.05	V	IOUT= -10mA (*8)
OUT pin output voltage L	V_{OUTL}	0.05	0.12	0.2	V	IOUT= 10mA (*8)
Rising time	T_r		50	100	ns	OUT load:1000pF
Falling time	T_f		50	100	ns	OUT load:1000pF
TRIAC dimmer current source						
Current source threshold voltage	V_{BLEED}	1.0	1.2	1.4	V	BLEED pin
Resistor 1 (HV-GND)	R_{ONH1}		450	710	Ω	IHV=20mA (*8)
Resistor 2 (HV-GND)	R_{ONH2}		900	1350	Ω	IHV=10mA, Tj=125 (*8)

ELECTRICAL CHARACTERISTICS (the rest)

Ta=25°C, HV=open, VDD=15V, REF=0.1uF, PWM=VREF, SEL=GND, R15=200kΩ, VFC=VREF unless otherwise specified.

VDD is applied after UVLO is released, which is after the HV voltage (18V typical) is applied.

Parameter	Symbol	Specification			Unit	Note
		MIN	TYP	MAX		
Startup circuit						
Operating startup voltage	UVLOH	15.5	17.6	19.8	V	VDD voltage rising
Operating shutoff voltage	UVLOL	5.6	6.4	7.2	V	VDD voltage falling
Startup current source threshold voltage 1	VDDH	9.1	10.3	11.6	V	VDD voltage rising
Startup current source threshold voltage 2	VDDL	7.8	8.8	9.9	V	VDD voltage falling
Startup current	IDDCH	-12	-8.5	-5.0	mA	VHV=100V, VDD=6.5V(*8)
Internal regulator						
REF voltage	V_{REF}	4.9	5.0	5.1	V	REF current: 0mA(*8)
REF dropout voltage	VDROP		20	100	mV	REF current: -7mA(*8)
Protection circuits						
Thermal protection	TSD	130	150	170	°C	Design Assurance Value
Thermal protection release temperature	ΔTSD	29	65	101	°C	Design Assurance Value
CS over current detection	OCP	720	800	880	mV	LATCH off
VDD over voltage detection	OVP	23	26	29	V	LATCH off

Note:

*8 Current definition: Flow to the pin is plus, flow out from the pin is minus.

OPERATION

1) Operation outline

The AP1601 operates directly from a rectified AC voltage supply (100~240V). It has 2 selectable operating modes, a DCM flyback type and a CCM chopper type (buck) constant current driver. Switching frequency, set by an external resistor, can be automatically adjusted depending upon the LED Vf value. The LED current variation related to the LED Vf variation will be minimized.
Furthermore, the LED current is controlled constant on chopper type (buck) even when the input voltage varies. Dimming can be done using a peak current control method, a PWM pulse current control method, or switching frequency adjustment independently or in combination.
(In the following description, the symbols and numbers on the external parts refer to Figure 22. A typical isolated flyback application circuit for TRIAC dimming is shown later)

2) Operation

2-1) Operation mode

The AP1601 can select from 2 different operation modes. The mode is determined by the voltage of the SEL pin.

Operation mode	SEL pin voltage	External MOSFET control	
		OUT pin H→L	OUT pin L→H
Fixed frequency mode	V_{REF}	The OUT pin is switched from H to L by detecting peak voltage on the CS pin	After rising of the internal CLK signal determined by the OSC pin voltage: if the VFC pin voltage becomes lower than the bottom voltage detection level (<V_{THZC}), the OUT pin is switched from L to H.
Fixed off-time mode	GND	The OUT pin is switched from H to L by detecting peak voltage on the CS pin	After passage of the off-time determined by OSC pin voltage, the OUT pin is switched from L to H.

The fixed frequency mode is suitable for the discontinuous current conduction mode in the flyback circuit shown in Figure 3. On the other hand, the fixed off-time mode is suitable for the continuous current conduction mode in the chopper circuit (buck) shown in Figure 4. Please refer to the application examples of Figure 22 and Figure 23 for the complete circuits.

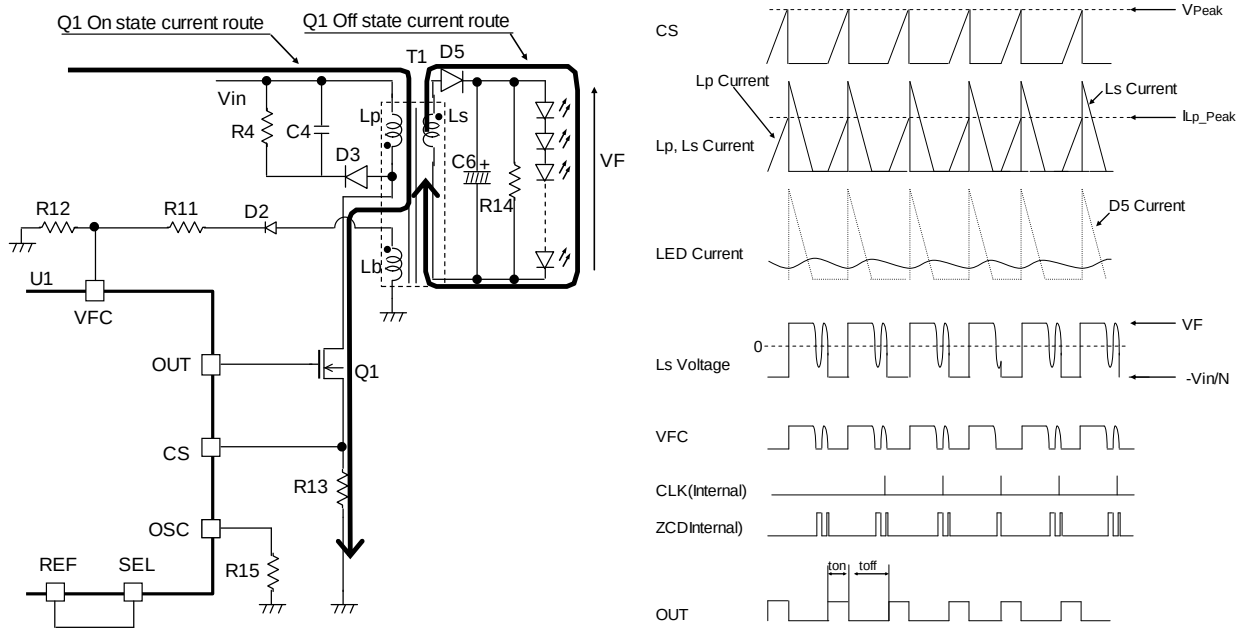


Figure 3 Operation of flyback circuit on fixed frequency mode

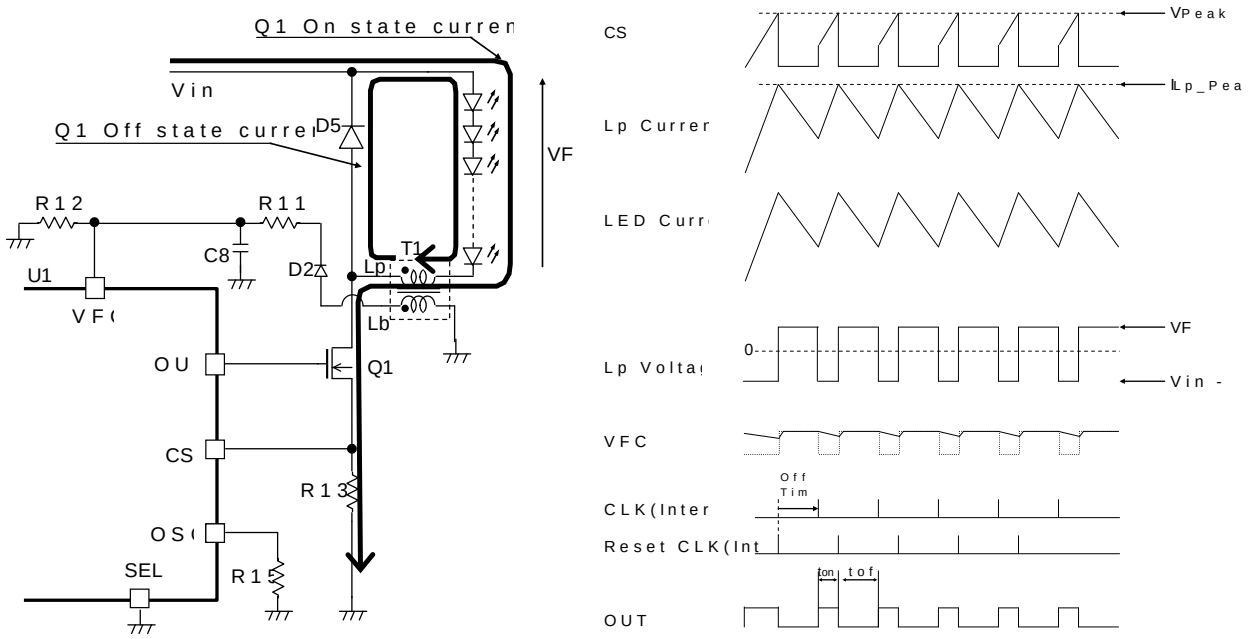


Figure 4 Operation of chopper circuit (buck) on fixed off-time mode

2-2) Current control

The external N channel MOSFET of the AP1601 moves into off-state by detecting the peak current and by using the internal clock (CLK) determined by the VFC voltage (*1) and resistor R15 between the OSC and GND, the MOSFET migrates into on-state (*2). By repeating this PWM switching behavior, the LED current is controlled. The LED current, which is affected by LED forward voltage variation or fluctuation of an external cause, will be compensated to keep it constant by the VFC pin monitoring the auxiliary winding voltage on the transformer and automatically adjusting the internal clock (CLK) cycle.

Note:
*1 It indicates the sampling voltage (V_{VFC}) of the VFC voltage after 700ns (design value) after the OUT pin is turned to V_{OUTL} level.
*2 In the fixed frequency mode, it migrates into an on-state waiting for the VFC voltage to become lower than V_{THZC} (0.1V(typ)) after the rising CLK.

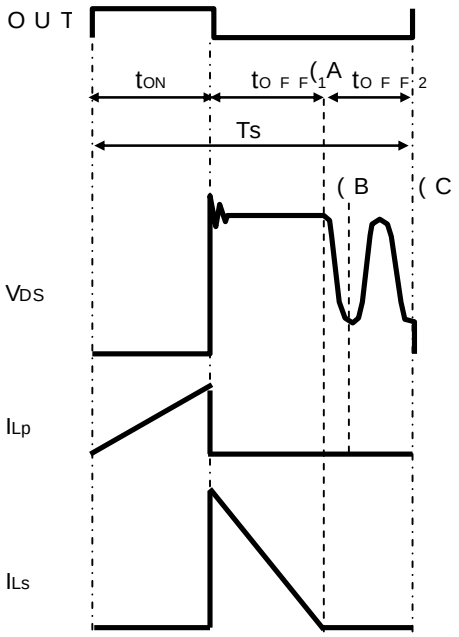
2-2-1) Fixed frequency mode

The AP1601 LED current on the flyback circuit is set by the self-inductance of the transformer's (T_1) primary winding peak current and switching frequency (F_{SW}). The ratio between the primary winding and the secondary winding (0.2 N_{ps} 1) of the transformer is obtained from the switching frequency requirement.

Approximation of LED average current I_{LED_ave} is;

$$I_{LED\_ave} = \eta \times \frac{1}{2} \times \frac{L_p \times I_{Lp\_peak}{}^2 \times F_{sw}}{V_F + V_{FD5}}$$

Here, η is the energy transmission efficiency of the transformer T1 from the primary winding to the secondary winding (η=0.85～0.95), V_F is the total of the LED forward voltage connected in series, V_{FD5} is the diode forward voltage.
Peak current is set by resistor R_{13} connected between the Q_1 source and GND, switching frequency is set by resistor R_{15} described before and the V_{VFC} voltage. However, there is an upper limit of the switching frequency on DCM flyback operation.
Even if the Internal CLK signal is set higher, it is limited to the switching frequency upper limit.
Figure 5 is showing a wave form image on DCM flyback operation of OUT pin voltage, Q1 drain-source voltage (V_{DS}), transformer primary side current (I_{LP}) and transformer secondary side current (I_{LS}).



	tON	tOFF1	tOFF2
OUT	ON	OFF	OFF
D5	OFF	ON	OFF
ILp	$\frac{V_{in}}{L_p} \times t$	0	0
ILs	0	$\frac{I_{Lp\_Peak}}{N} - \frac{V_F + V_{FD5}}{L_S} \times t$	0

Figure 5. DCM flyback mode wave form

The AP1601 fixed frequency mode is using the T1 auxiliary winding, waiting until the Q1 drain voltage falls off after the secondary current becomes zero, then moves to the next cycle. Approximations of "tON, tOFF1" time requirement in Figure 5 are;

$$t_{ON} = \frac{L_p}{V_{in}} \times I_{LP\_Peak}$$

$$t_{OFF1} = \frac{I_{LP\_Peak}}{N} \times \frac{L_S}{V_F + V_{FD5}} = \frac{L_P}{V_F + V_{FD5}} \times I_{LP\_Peak} \times N$$

Next, the tOFF2 period is the time for compensation to the LED VF variation. By detecting the bottom voltage using the VTHZC threshold, tOFF2 (for example) is defined by (B) or (C) if each switching is observed. However, the internal CLK operates at a constant cycle while VVF is maintained constant, and tOFF2 will be an ideal period if averaged for a sufficiently long time (e.g., 10ms for 100kHz switching frequency).

The shortest amount of the tOFF2 time is between (A) and (B) shown in Figure 5. This is the reason why the drain voltage doesn't fall off immediately due to resonance caused by the primary side inductance (Lp) of the transformer and a parasitic capacitor (Clump) between Q1 drain and GND.
Approximation of tOFF2's minimum time is as follows.

$$t_{OFF2\_min} = \pi \cdot \sqrt{L_p \times C_{lump}}$$

If the compensation for LED VF variation is Corr%, the approximation of the set value is as follows.

$$t_{OFF2} = (t_{ON} + t_{OFF1} + t_{OFF2\_min}) \times Corr\%$$

e.g. When Vin=100V, Lp=680uH, ILp=0.7A, VF=30V, VFD5=0.7V, N=0.4, Clump=100pF and ±Corr%=±30%, tON=4.76us, tOFF1=6.2us, tOFF2_min=0.82us, and tOFF2 is calculated to be 3.53us.
From this, when the set frequency is approximately 69kHz and energy transmission efficiency of the transformer η is 0.9, the LED average current will be approximately 337mA.

When the frequency needs to be higher without affecting to the other parameters, tOFF1 should be shorter by changing the winding ratio (N) lower.
However, when the winding ratio (N) decreases, transformer transmission efficiency tends to be less, and the AP1601 shortest tOFF1 time is designed at 2us, therefore, please do not be shorter than that in steady state.
In actual AC power source input, Vin is the absolute value of the sine wave, peak current is proportional to Vin until a certain voltage level, please calculate using the time of the half cycle of the AC power frequency (50Hz/60Hz).

The AP1601 switching frequency on fixed frequency mode is roughly determined by R15 connected between the OSC and GND and the sampling voltage on the VFC pin in normal state as follows.

$$F_{SW} = \frac{V_{VFC}[V]}{R_{15}[\Omega]} \times 10^{7}[kHz]$$

$$0.5V \le V_{VFC} \le 1.5V、\ 20k\Omega \le R_{15} \le 400k\Omega$$

Figure 6 shows the relationship between the VFC pin voltage wave form and the voltage sampling point, as well as between the V_{VFC} voltage and the internal CLK frequency when using R_{15}=100kΩ

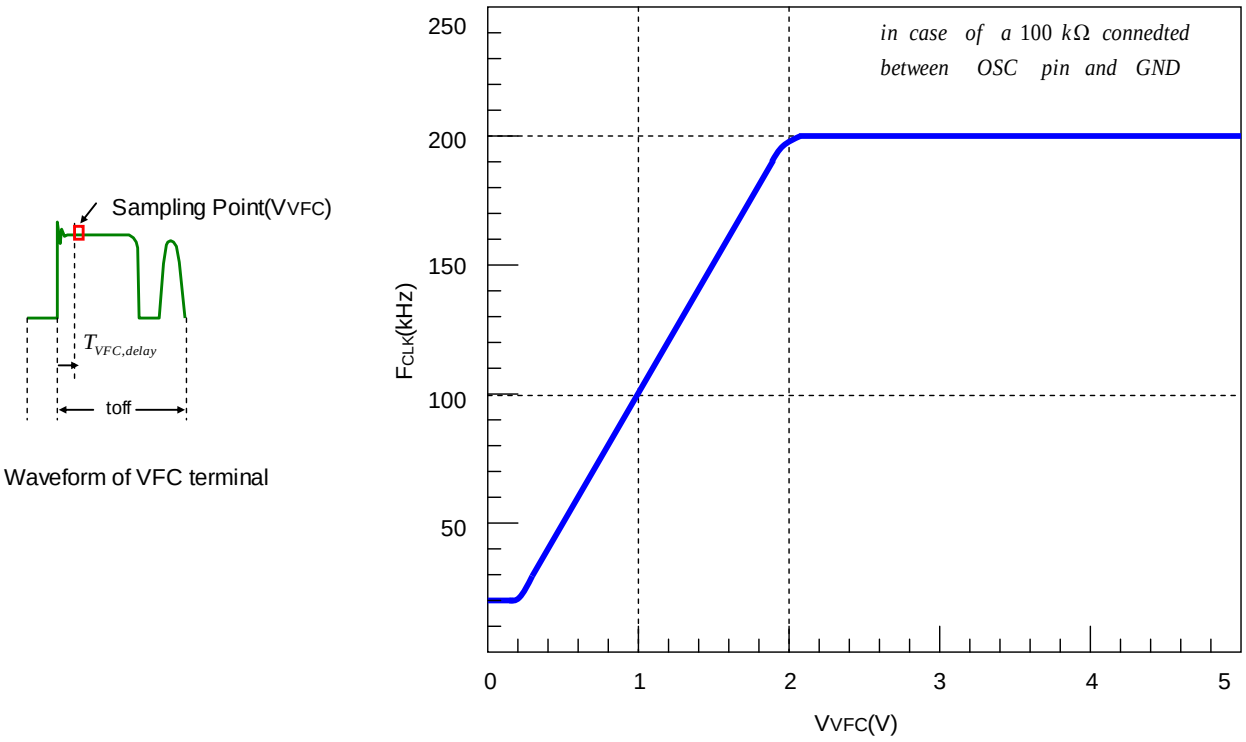


Figure 6. V_{VFC} sampling point and relationship between voltage and internal CLK frequency at R_{15}=100kΩ

Figure 7 shows an image of the compensation for the LED current changed by the VFC pin waveform that is proportional to the variation of the LED V_F. The left side waveforms are for high V_F, the right side are for low V_F.

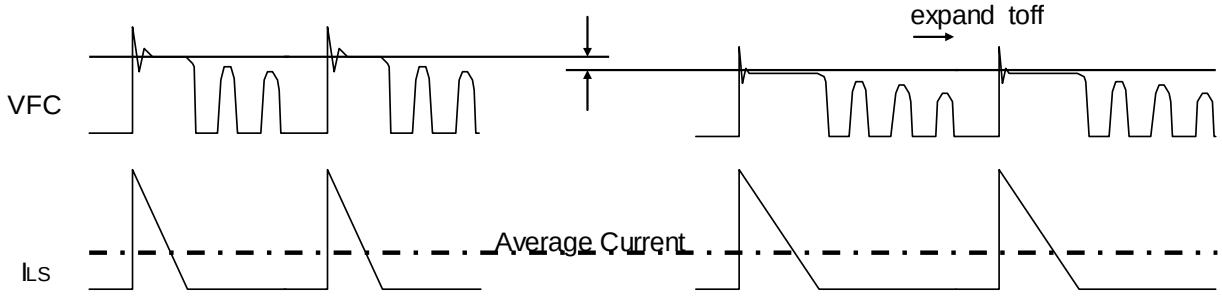


Figure 7. Average current compensation on switching frequency changed by V_{VFC} voltage change.

When the LED V_F increases, a voltage that is proportional to the secondly winding and the auxiliary winding is output as the auxiliary winding voltage immediately after the MOSFET turns off.
The switching frequency is changed due to the OSC pin voltage changes that are according to the sampling voltage divided by a resistor divider from the auxiliary winding. This changes the power. Approximation of V_{VFC} is given by the following equation.

$$V_{VFC} = \frac{R_{12}}{R_{11}+R_{12}} \cdot \left\{ \frac{N_B}{N_S} \cdot (V_{D5} + V_{C6}) - V_{D2} \right\}$$

N_S、N_B are respectively the number of the secondary winding and the auxiliary winding of transformer T1 .
The V_{VFC} voltage is reflected in the OSC pin voltage and is in the range from 0.2V(typ) to 2V(typ); if it is less than 0.2V , the OSC voltage will be 0.2V, and if it is more than 2V(typ), the OSC pin voltage will be 2V(typ). (refer to Figure 6.)
As the graph in Figure 6 shows, V_{VFC} which is the center of V_F variation should be 1V to compensate LED V_F variation. When the voltage is 1V, the ratio of R11 and R12 is approximately given by the following formula.

$$\frac{R_{11}}{R_{12}} = \frac{N_B}{N_S} \cdot \left(V_{D5} + V_{C6}\right) - V_{D2} - 1$$

R11's selectable range is from 5kΩ to 100kΩ. The number of transformer auxiliary winding is determined by the V_{DD} voltage.
The VDD pin voltage, V_{DD} in stable operation, is approximately given by the following formula,

$$V_{DD} = \frac{N_B}{N_S} \cdot \left(V_{D5} + V_{C6}\right) - V_{D4} - I_{DD} \times R_3$$

When the LED V_F variation is expected to be ±30%, the V_{DD} voltage, which is the center of the variation, should be set approximately to 15V to be operating within the V_{DD} operating voltage range.

Bottom voltage detection (V_{THZC})
Figure 8 shows the schematic of bottom voltage detection on the VFC pin.
As the figure is shown, the rising edge of the internal CKL is the regular interval (=Ts)
However, by the bottom voltage detection function, CLK is kept on high level until VFC becomes less than V_{THZC} as shown in the dashed line box A in the figure.
If the VFC pin is already less than V_{THZC} at the internal CLK rising edge, the OUT pin should be V_{OUTH} level.
However, there are the following exceptions in order to prevent malfunction.
① If internal CLK rises while the OUT pin is V_{OUTH} level, the CLK will not be maintained.
② T_{BLANK} period (700ns, design value) immediately after the OUT pin becomes V_{OUTL} level, ZCD(Internal) shown in Figure 8 is held as low level and V_{THZC} detection on the VFC pin is disabled.

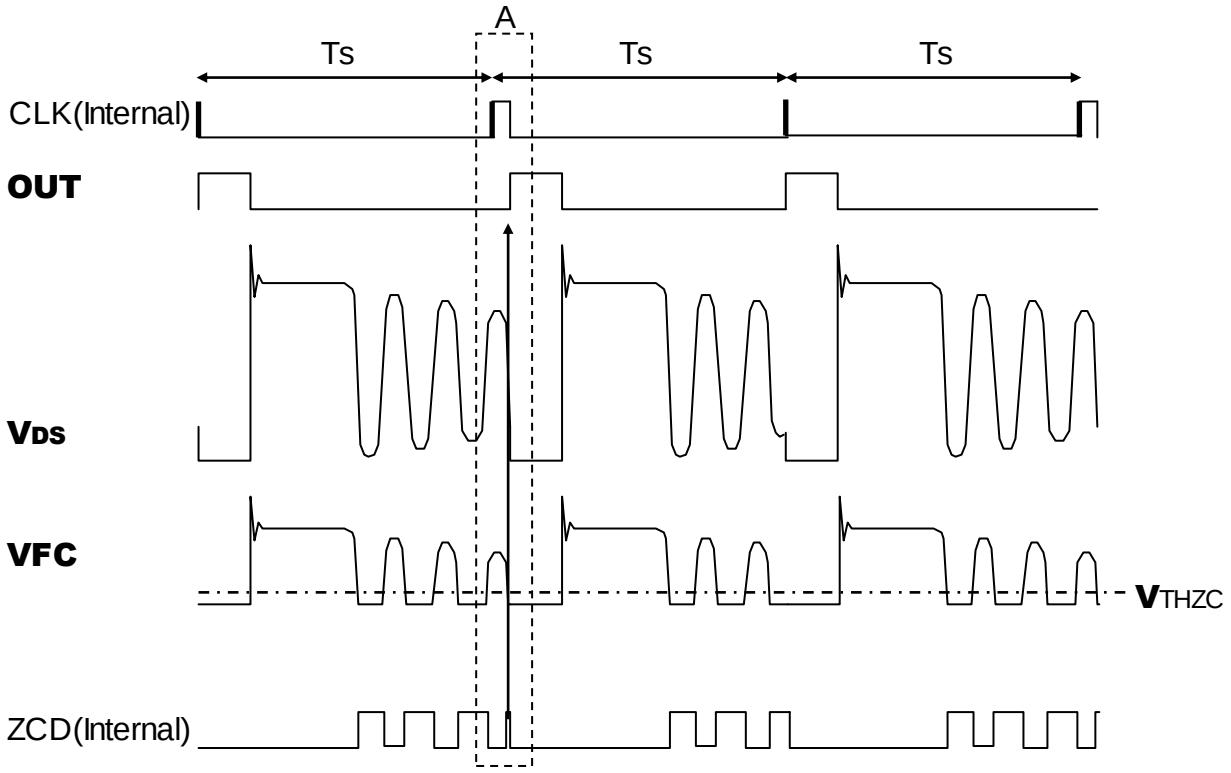


Figure 8. Bottom voltage detection (VTHZC)

By this bottom voltage detection function, the external MOSFET is able to turn on in low voltage and current level, and a noise-reduction effect can be expected. Furthermore, switching-loss can be reduced and power efficiency will be improved.

2-2-2) Fixed off-time mode

CCM chopper (buck) circuit using the AP1601 fixed off-time mode controls the peak current and the bottom current of the coil constant (constant ripple control). By this control, the switching frequency is changed for input voltage and LED V_F variation.

Figure 4 shows the current path of a chopper (buck) circuit, current, or voltage waveform for each part. The primary side of the transformer is controlled by the OUT pin which turns the MOSFET (Q_1)on and off.

The current path when the OUT pin turns on (V_{OUTH}) is Vin－LED－L_p－Q_1－R_{13}－GND.

The current path when the OUT pin turns off is L_p－D_5－LED. The peak current of L_p when the OUT pin turns on is controlled by turning the OUT pin off and detecting the CS pin voltage. The bottom current should be set by the transformer primary winding self inductance, LED V_F, off-time (t_{OFF}).

If the diode D V can be ignored (V_{FD5}<<V_F), the transformer primary side current when the MOSFET turns off will be decreasing with time $-\frac{V_F}{L_p}\times t_{OFF}$. t_{OFF} is the time after Q_1 turns off.

For example, the I_{Lp} bottom current is constant when V_F, L_p and t_{OFF} are constant.

When V_F is varied, the transformer auxiliary winding is affected by the variation, off-time changes inversely according to the V_{VFC} voltage which is changed by the variation, the bottom current is kept constant.

Fixed off-time control allows the DC voltage input to be on the VFC pin because the bottom voltage detection on the VFC pin is not performed (refer to Figure 4).

LED average current I_{LED_ave} is,

$$I_{LED\_ave} = I_{Lp\_peak} - \frac{1}{2}\times\frac{V_F \times t_{OFF}}{L_p}$$

I_{Lp_peak} is peak current on the transformer primary side.

Relationship between off-time t_{OFF}(us) and R_{15}(kΩ) connected between the OSC pin and GND when V_{VFC} is 1V is,

$$t_{OFF}\,[\mu s] = \frac{1}{10}\times R_{15}[k\Omega]$$

If V_{VFC} is considered further,

$$t_{OFF}\,[\mu s] = \frac{1}{10}\times\frac{R_{15}[k\Omega]}{V_{VFC}\,[V]}$$

V_{VFC} is proportional to the V_F, even when V_F is varied; LED average current is held constant, offset by t_{OFF}.

However, if the off-time is long and the bottom current becomes zero (from CCM to DCM), LED average current is affected by on-time, so the LED current cannot be compensated by V_{VFC}. Thus, the off-time setting is approximately limited by the following formula.

$$t_{OFF} \le \frac{L_p}{V_F}\times I_{Lp\_peak}$$

Constant ripple current control maintains the peak current and the bottom current constant, and the current control can be done without being affecting by the input voltage fluctuation and LED V_F variation, in spite of the fact that the switching frequency is changed by input and output voltage changes.

Figure 9 shows examples of frequency change when the input voltage changes and the number of LEDs connected in series (V_F) changes. In order to be within desired switching frequency range, the transformer primary side inductance (Lp), ripple width between the peak current and the bottom current needs to be configured properly.

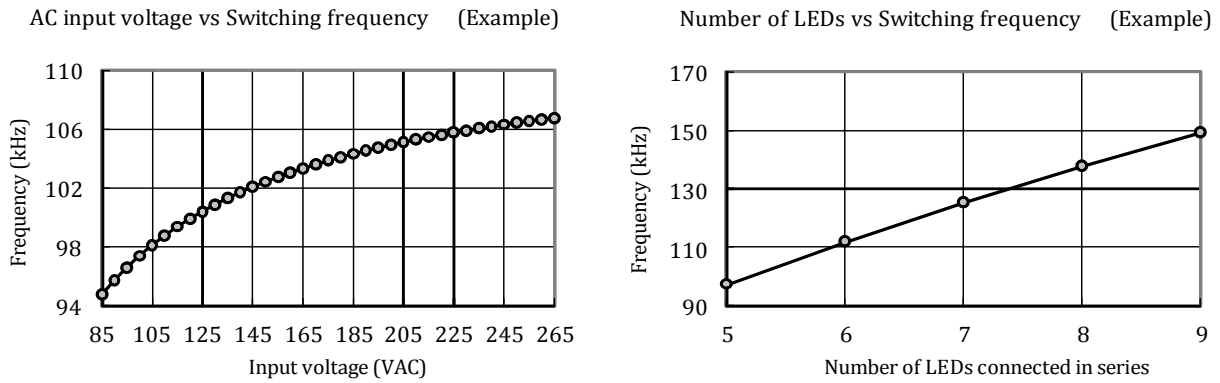


Figure 9. Examples of frequency changes as in input voltage changes or number of LEDs change

Switching frequency F_{sw} is approximately given by the following formula,

$$F_{sw} = \frac{V_{in} - V_F}{L_p \times \left(I_{Lp\_peak} - I_{Lp\_bottom}\right)} \times \frac{V_F}{V_{in}}$$

I_{Lp_bottom} is the bottom current on the transformer primary side after the off-time t_{OFF} period.

2-2-3) Analog dimming

LED analog dimming is available using the LD pin. Analog dimming is achieved by decreasing the peak current on the transformer primary side. Analog diming is controlled by applying an external voltage to the LD pin. The allowable voltage range on the LD pin is from 0 to V_{REF}(5V (typ)). The peak detection voltage on the CS pin is changed when the LD voltage is less than 2.65V(typ) as shown in Figure 10. Switching will not stop even if the LD pin connects to GND.

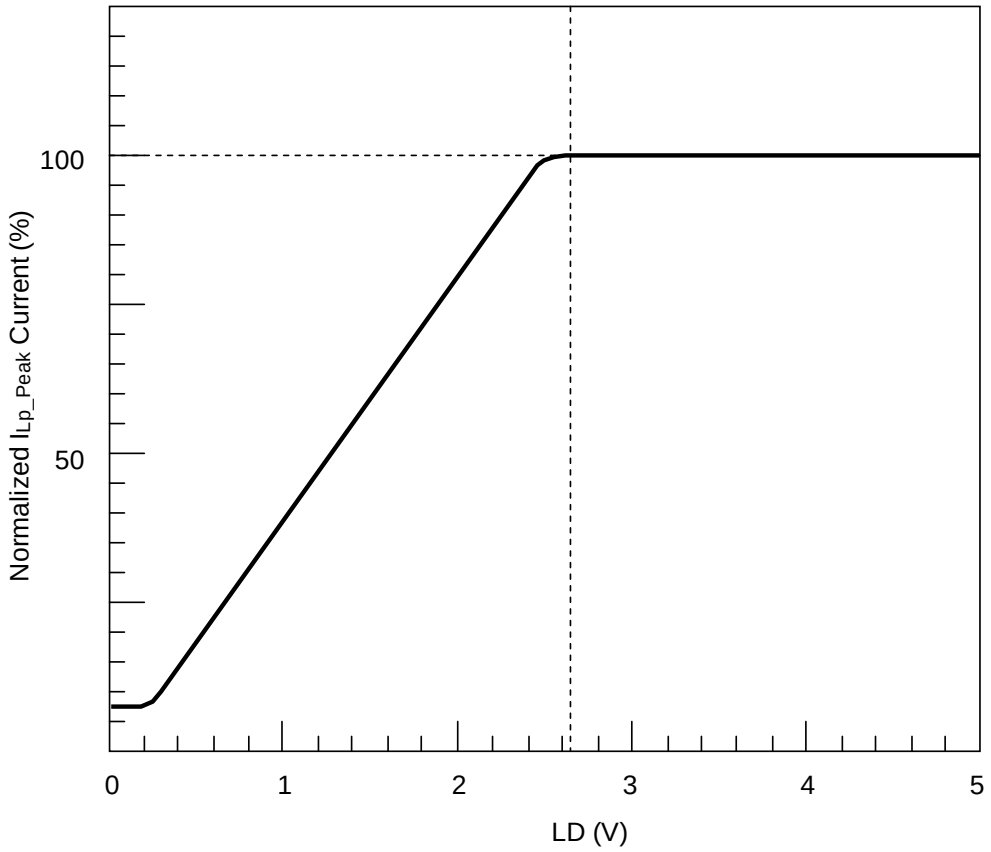


Figure 10. Relationship between LD pin voltage and transformer primary side current (**I_{Lp_peak}**)

2-2-4) PWM dimming

PWM dimming is available using the PWM pin. PWM diming is controlled by applying an external pulse to the PWM pin, which is referenced to GND. The allowable voltage range on the PWM pin is from 0 to V_{REF}(5V (typ)) and up to 2kHz PWM pulse signal may be used. By holding the PWM pin voltage to less than V_{PWML} (less than 0.5V), the OUT pin can be fixed to off level (V_{OUTL})

2-2-5) Leading edge blank and shortest on time of OUT pin

The AP1601 does not detect current by masking for a certain period after the Nch MOSFET turns on. This is called leading edge blank (T_{LEB}). It means, the voltage on the CS pin is ignored during this period. The period is necessary to avoid instantaneously turning OUT off and on or ceasing the switching by the over current protection function when the reverse recovery current of diode D_5 or the discharge current from parasitic capacitor is large while Q_1 is on.
However, all current detection on the CS pin is started after T_{LEB} , the shortest on time of Q is limited by the leading edge blank. Worst case of T_{LEB} at 25°C is 450ns.

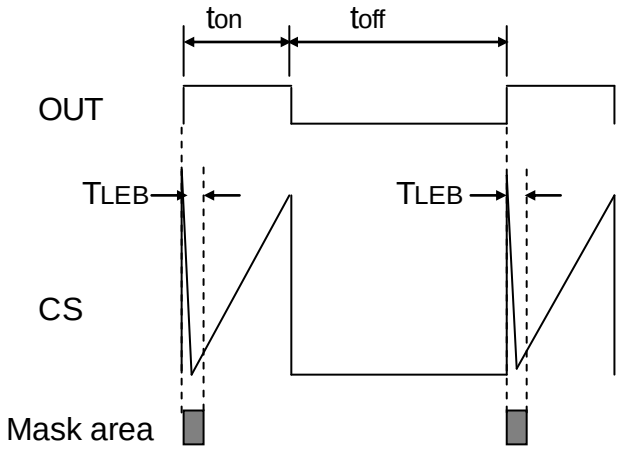


Figure 11. CS pin voltage leading edge blank

Thus, input voltage range, output voltage range, ripple width and the transformer primary side inductance should be determined to guarantee that the on-time during the operation is always more than T_{LEB} . On-time is approximately given by the following formula and limited by T_{LEB}.

$$\text{Flyback circuit;}\quad t_{on} = \frac{L_p \times I_{Lp\_peak}}{V_{in}} + t_{d\_MOS} \quad > T_{LEB} + t_{d\_MOS}$$

$$\text{Chopper (buck) circuit;}\quad t_{on} = \frac{L_p \times (I_{Lp\_peak} - I_{Lp\_bottom})}{V_{in} - V_{out}} + t_{d\_MOS} \quad > T_{LEB} + t_{d\_MOS}$$

T_{d_MOS} represents a delay time until MOSFET (Q_1) turns off after the OUT pin is turned off.
If on-time is less than the delay time during the operation condition, the peak current will be higher than the set value and the average current will also shift higher. Furthermore, if the CS pin voltage after T_{LEB} becomes higher than the over current protection threshold voltage, the switching will be ceased.

2-3) Gate drive

The OUT pin is the gate driver output, which can drive 1000pF capacitor at 50ns(typ) of raising and falling time by using the VDD voltage.

2-4) TRIAC dimming

The AP1601 has a built-in circuit which is compatible with TRIAC dimmers.

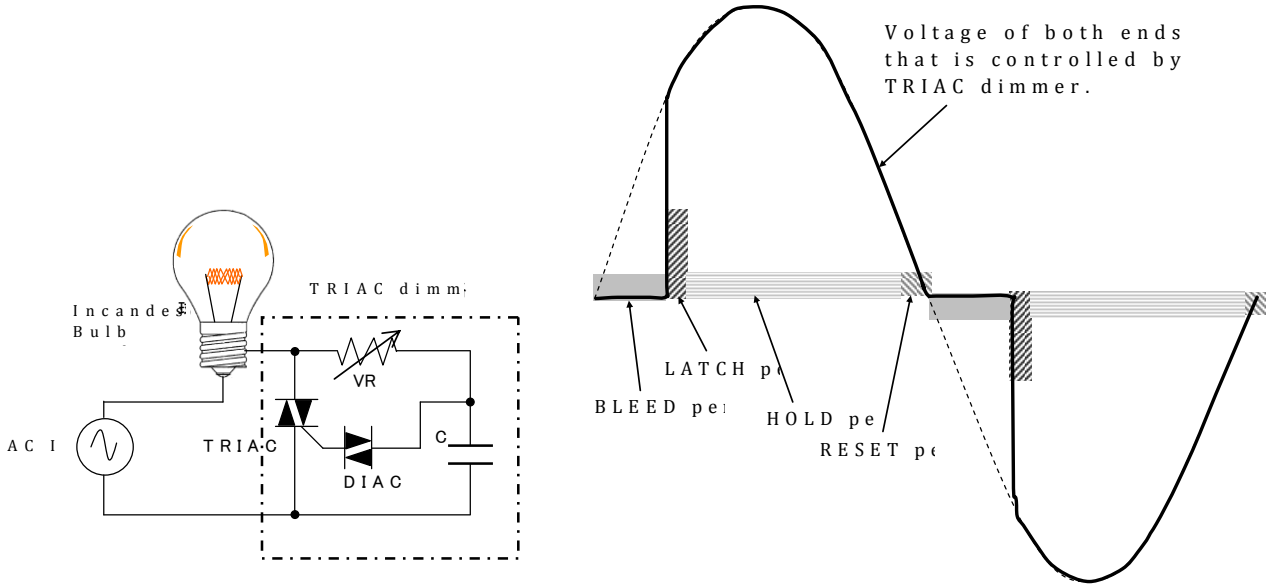


Figure 12. TRIAC dimmer

As shown in Figure 12, a TRIAC Dimmer for resistive loads like incandescent lamps performs dimming by changing the input power which is controlled by cutting any angle of the phase for the input sine-wave. The time constant determined by the Variable resistor (VR) turns the TRIAC (bidirectional thyristor) on in the dimmer and supplies the power to the load. The TRIAC sustains its conduction once turned on until the current to sustain the operation becomes lower than the threshold.
The Input current of the switching circuit becomes discontinuous because the diode-bridge turns off when it is below the input capacitor (C1) voltage.
AP1601 is a switching power supply, but to be compatible with a TRIAC Dimmer, it needs to emulate a resistive load for the TRIAC Dimmer (between the BLEED period and RESET period in Figure 12).
AP1601 has a BLEED current function for efficiency reasons, which supplies a current from the DB1 (Diode-bridge) plus pin to the minus pin through a resistor in the IC only while the TRIAC Dimmer needs a current to stay on. The function allows normal operation for TRIAC Dimmer applications.

Setting of BLEED current as a TRIAC dimmer supporting current is shown below.
V_{BLEED} to determine when BLEED current flows is 1.2V(typ), On resistance of the HV pin to sink BLEED current is 450Ω(typ), If maximum BLEED current is 20mA, the resistor to be connected between the BLEED pin and the HV pin is approximately given by the following formula.
Resistors R_5, R_6 to determine when BLEED current flows are given as follows.
If, in case of V_{rf_th} to determine when BLEED current flows is 35V and R_5=510kΩ, R_6 is,

$$R6 = \frac{1.2V \times R5}{V_{rf\_th} - 1.2V} = \frac{1.2 \times 510}{35 - 1.2} \approx 18\,[k\Omega]$$

Resistor R_2 connected on the HV pin to limit current is given as follows.

$$R2 \geq \frac{V_{rf\_th} - 450\Omega \times 20mA}{20mA} = 1.3\,[k\Omega]$$

2-5) Startup circuit

The AP1601 has a startup circuit which is supplied power from the high voltage HV pin. By using the auxiliary winding (L_b) of the transformer, the external device count relevant to startup can be further reduced, this also, allows power loss after startup to be reduced significantly. The internal startup circuit is also connected to the VDD pin through a diode as shown below, and the VDD pin voltage increases in accordance with the applied input voltage.
When the VDD pin voltage reaches the operating startup voltage (U_{VLOH}=18V typical), the internal circuit is activated and switching is started. The internal startup circuit is cut off from the HV pin in this state, and the power to the internal circuit is supplied directly from the auxiliary winding of the flyback transformer to the VDD pin, which is more efficient.

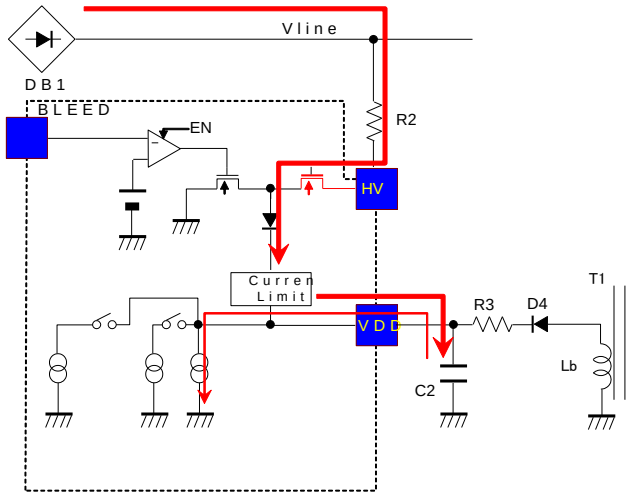
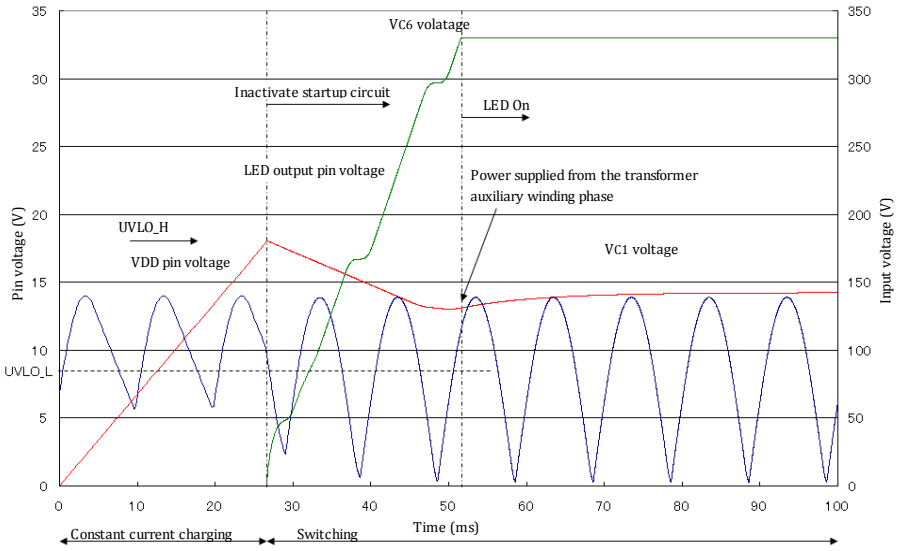


Figure 13. Startup circuit



Red: VDD pin voltage (left axis), GREEN: LED anode voltage (left axis), BLUE: Input voltage (Vrf: right axis)
Figure 14. Waveform at startup

Figure 14 shows the voltage waveform immediately after power on of an AC100V application.
Red: VDD pin voltage, Blue: primary side input capacitor (C1) voltage, Green: Output electrolytic capacitor voltage. The left vertical axis represents the VDD pin voltage and the C6 pin voltage, the right vertical axis is the C1 voltage.
In this example, the LED is lit approximately 50ms after power on. (Condition: Input voltage 100Vac, C1=0.47uF, C2=10uF, C6=100uF, VOUT=33V)

2-5-1) Power-on state – initiation of IC operation phase

External capacitor, C2 starts charging through the internal startup circuit powered from the HV pin after power on. This charging path will be cut off when the VDD pin achieves operating startup voltage ($UVLO_H$). When VDD is below the $UVLO_H$ voltage, the internal circuits, except some circuits needed for startup, cease operation.

2-5-2) Initiation of IC operation - Stable operation phase

When VDD pin voltage becomes UVLOH, REF will be supplied power from VDD first (charge C7)
If REF is rising, the internal reset signal rises, all of the IC circuits start and the switching operation starts. However, usually, the voltage of electrolytic capacitor (C6) connected on the secondary side is lower than V_{DD} immediately after switching starts, therefore, power from the auxiliary winding to the VDD pin will not be supplied, so, the switching operation is performed by consuming the power from charged capacitor (C2). When the voltage of electrolytic capacitor (C6) connected on the secondary side rises enough, power from the transformer auxiliary winding to the VDD pin becomes sufficient and V_{DD} will be stable.

To prevent the VDD pin voltage from becoming lower than UVLOL when the power from the auxiliary winding is deficient, constant current charging from the HV pin to the VDD pin is properly performed to maintain the VDD voltage to a certain voltage range by using SWVDD monitoring of the VDD pin voltage. The Startup circuit that connects between the HV pin to the VDD pin is enabled at the SWVDD lower limit voltage (V_{DDL}: 8.8V(typ)), and disabled at the upper limit voltage (V_{DDH}: 10.3V(typ)).
If there is no power from auxiliary winding and power continues to be intermittently supplied from the HV pin to VDD, the IC generates heat due to the voltage drop from the input voltage to the V_{DD} voltage (8.8V(typ)～10.3V(typ)). Please adjust the HV pin voltage to less than 120V_{RMS} by resistor R_2 connected between the HV pin and Vrf when the HV pin voltage exceeds 120V_{RMS}.

Time chart in regard to startup circuit is shown in Figure 15.

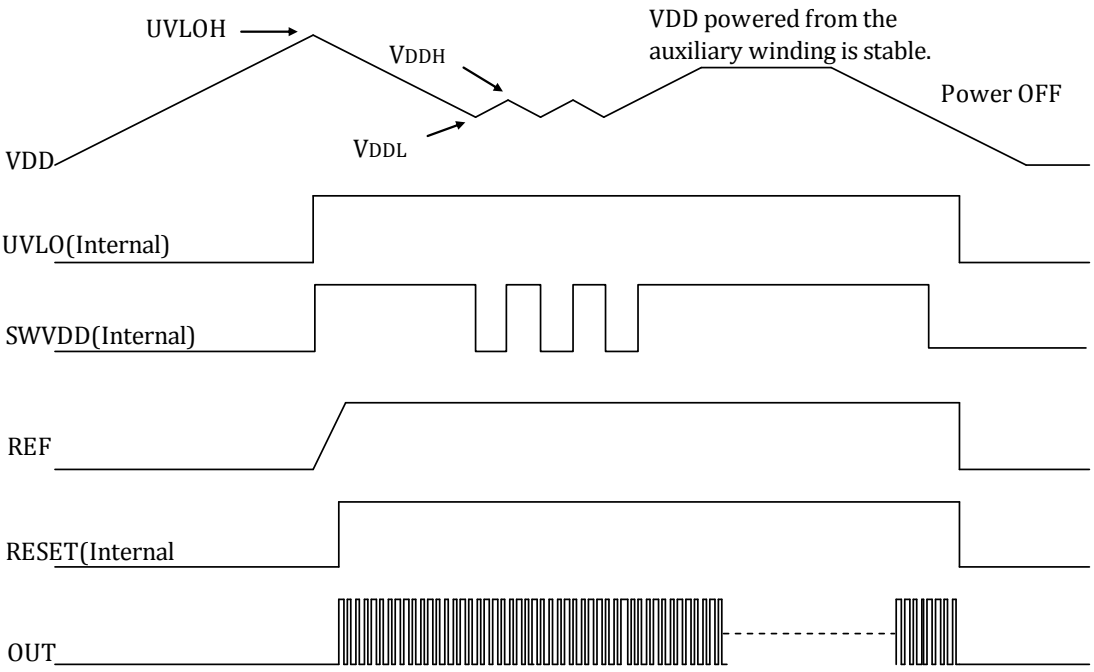


Figure 15. Image of startup circuit operation (Time chart)

2-6) Internal regulator

The AP1601 has a built in 5V regulator to supply voltage from the VDD pin to the internal circuits, And if thermal conditions are met, a maximum of a 7mA current can be supplied to external circuits from the REF pin.
For voltage stability, please connect a 0.1uF capacitor (class B) between the REF pin and GND.

3) Protection function

Protection function	Operation	Shut-off state	Detection condition	Release condition
Thermal protection	If the IC temperature exceeds the detection condition, the OUT pin turns to GND level.	Cease driver Auto-release	IC junction temp. 150°C	65°C Down from detection temp.
Over current	If an over current flows to the external MOSFET, the OUT pin turns to GND level.	Cease driver Latch off	CS pin voltage after T_{LEB} 0.8V(typ)	*1
Over voltage	If LED is open or LED V_F is high, the OUT pin turns to GND level.	Cease driver Latch off	VDD pin voltage 26V(typ)	*1
UVLO	To prevent malfunction of the IC, the OUT pin is fixed to GND level and cease 5V regulator.	Cease all Auto-release	When VDD pin voltage decreasing 6.4V(typ)	17.6V(typ)

Note:
*1. In order to release the latch off state, please apply a voltage of less than UVLOL for at least 10ms to the VDD pin.

When the REF pin is shorted to GND, the IC prevents heat generation by limiting internal regulator maximum current to 40mA (design value).
If ambient temperature is high or the HV pin voltage is high or if both are true, the junction temperature may exceed the absolute maximum rating. If the rating is exceeded, the specification can not be guaranteed.

3-1) Thermal protection

To prevent thermal runaway of the IC, the junction temperature is always monitored and the IC operation is controlled. When the junction temperature exceeds T_{SD} (design value is 150°C typical), switching stops. When the junction temperature goes below the thermal release temperature (ΔTSD, 65°C(typ)), switching restarts. Once the thermal protection is activated, the specification can not be guaranteed.

3-2) Over current protection

The CS pin voltage is monitored after turning the MOSFET on and after the leading edge blanking period (T_{LEB}:300ns (typ)). If the CS pin voltage is at the OCP voltage (0.8V typical), switching stops and is latched. For example, when the CS pin voltage is 0.5V and the current is 500mA, the OCP level reaches 800mA. The application circuit is protected when the primary winding, the secondary winding, or the auxiliary winding is shorted. For releasing the over current protection, please apply a voltage of less than UVLOL for at least 10ms to the VDD pin.

3-3) Over Voltage Protection

The VDD pin voltage is monitored, and if the voltage exceeds the OVP voltage (26V typical), switching stops and is latched. It typically functions as an open protection for secondary side where LEDs are connected. For releasing the over voltage protection, please apply a voltage of less than UVLOL for al least 10ms to the VDD pin.

3-4) UVLO

Under Voltage Lockout. The circuit provides an ON signal to the internal circuits when the VDD pin voltage is higher than $UVLO_H$ (17.6V typical) and an OFF signal when the VDD pin is lower than $UVLO_L$ (6.4V typical). If the VDD pin voltage is lower than the $UVLO_L$ voltage, the IC stops switching. If the HV pin voltage is high enough, the VDD pin is provided a current through the internal startup circuit to reach $UVLO_H$ and restart the IC.

CHARACTERISTICS

1) Temperature dependency

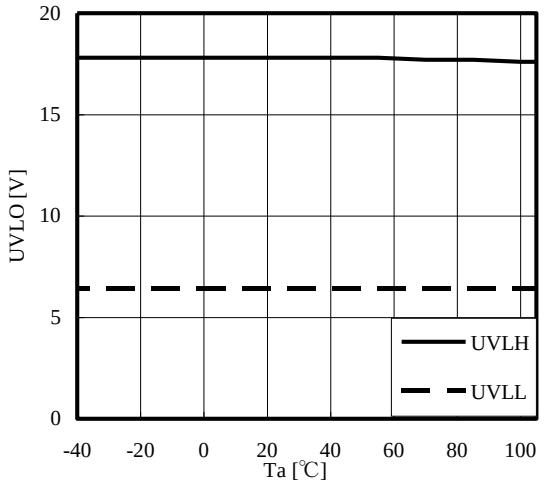


Figure 16. UVLO voltage

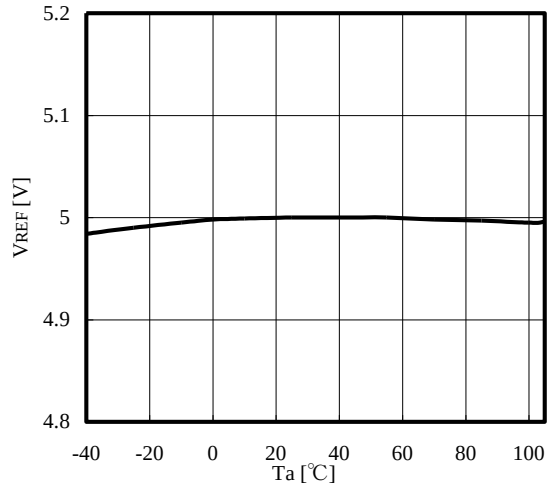


Figure 17. VREF voltage

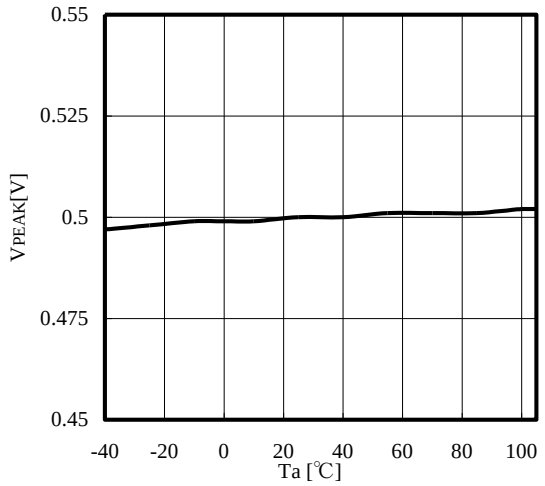


Figure 18. Peak current detection voltage (LD=REF)

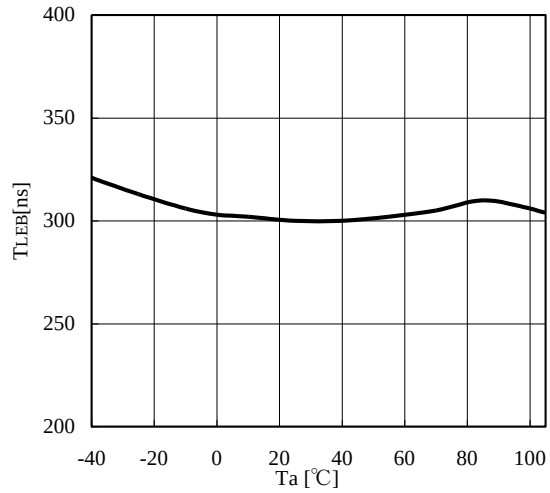


Figure 19. Leading Edge Blank

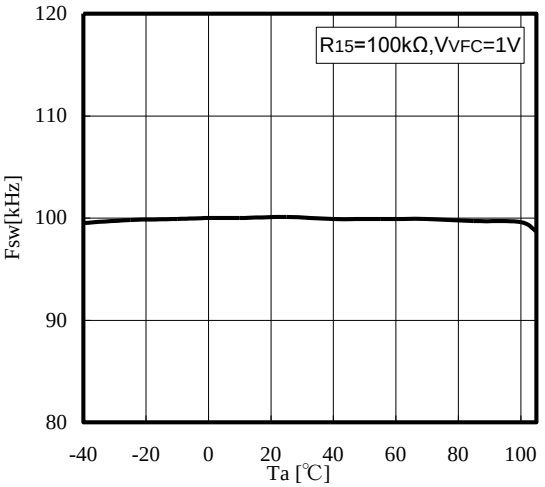


Figure 20. Switching frequency (SEL=VREF)

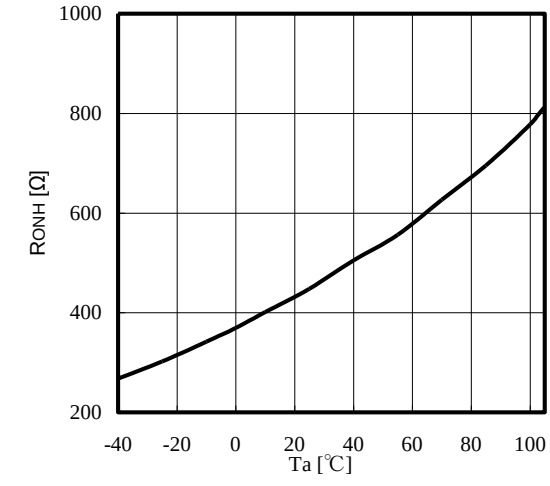


Figure 21. Equivalent R value HV-GND (IHV=20mA)

APPLICATION EXAMPLE

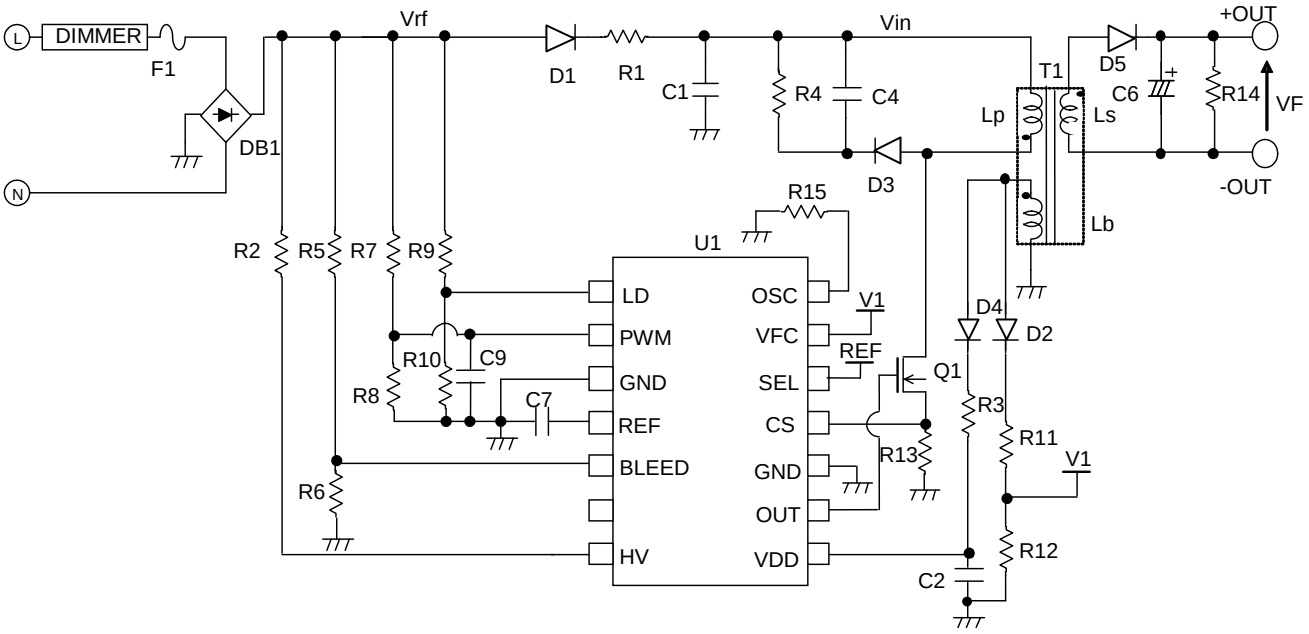


Figure 22. Typical isolated flyback circuit compatible with TRIAC dimmer

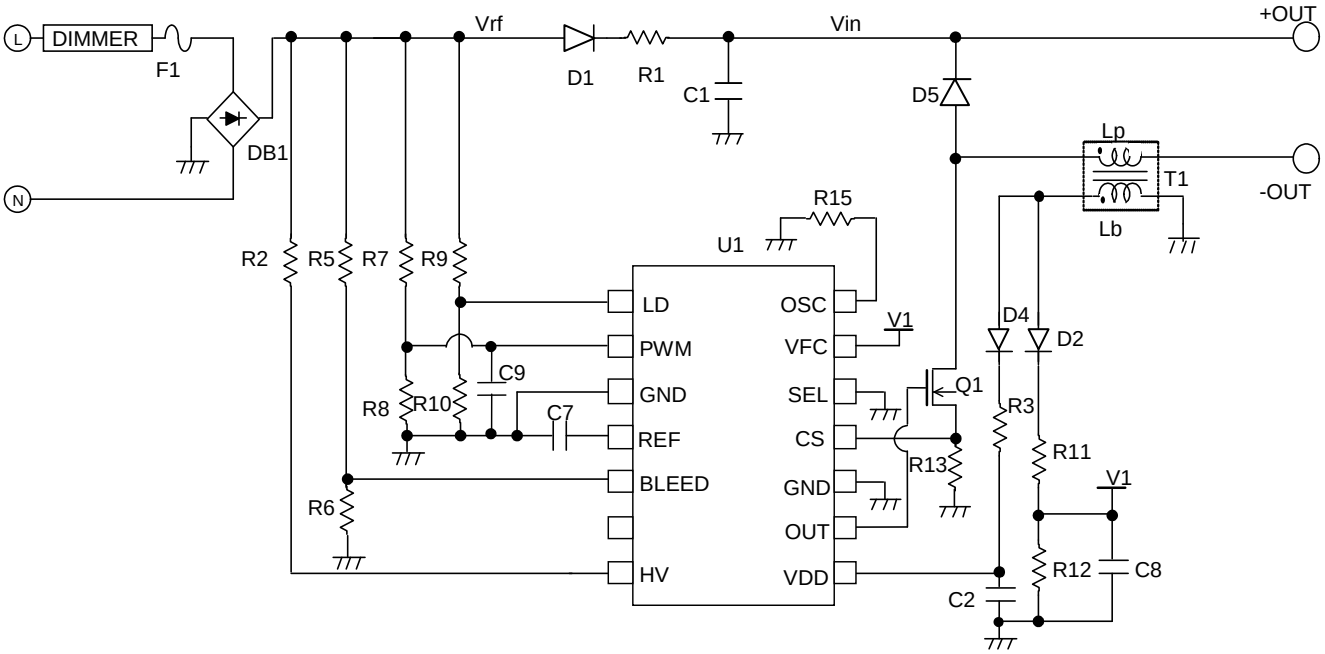


Figure 23. Typical non-isolated chopper circuit compatible with TRIAC dimmer

* The above figures are for reference only.
* A varistor to absorb a surge voltage, a common mode choke coil to reduce noise, across the line capacitor and such are not shown above.
* In order to prevent a large current from continuously flowing when the IC has failed due to incorrect wiring during assembly or abnormal pulse noises and so forth, please place the appropriate fuse to meet the appropriate standards in the appropriate place in the circuit.

PACKAGE and MARKING

1) Dimension (14 pin SOP)

[Unit:mm]

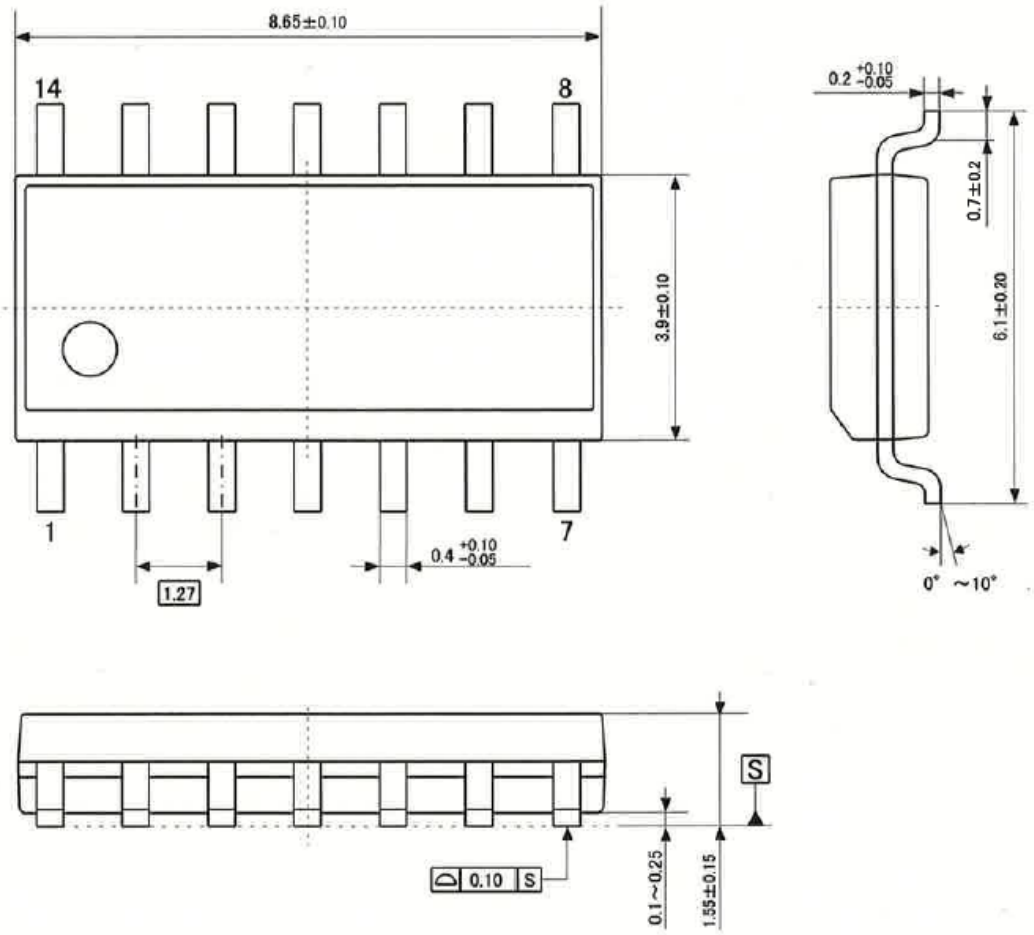


Figure 24. Package outline

2) Marking

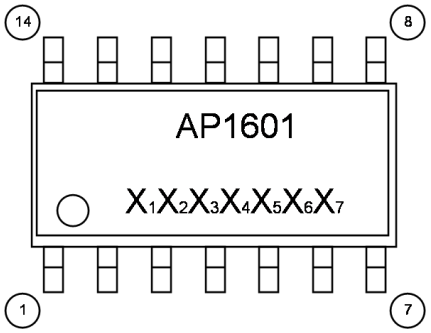


Figure 25. Marking Information

Upper	Product name：AP1601
Lower	Date code: 7 digits 2 digits (Last 2 digits of year) +2 digits (weekly code) + 3 digits (production code)