APW7324

ANPEC

4A,5V, 500KHz Synchronous Buck Converter

Features

- **High Efficiency up to 94%**
  - Automatic Skip/PWM Mode Operation
- **Adjustable Output Voltage from 0.8V to V$_{IN}$**
- **Operating from 2.9 to 6V Supply**
- **Integrated 85mΩ High Side / 75mΩ Low Side MOSFETs**
- **Low Dropout Operation: 100% Duty Cycle**
- **Stable with Low ESR Ceramic Capacitors**
- **Current up to 4A**
- **Power-On-Reset Detection on VCC and VIN**
- **Integrate Soft-Start and Soft-Stop**
- **Over-Temperature Protection**
- **Over-Voltage Protection**
- **Under-Voltage Protection**
- **High/ Low Side Current Limit**
- **Power Good Indication**
- **Enable/Shutdown Function**
- **Available in SOP-8P and TDFN3x3-10 Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Notebook Computer & UMPC**
- **LCD Monitor/TV**
- **Set-Top Box**
- **DSL, Switch HUBr**
- **Portable Instrument**

General Description

APW7324 is a synchronous buck converters with integrated 85mΩ high side and 75mΩ low side power MOSFETs. The APW7324 with a current-mode control scheme can convert wide input voltage of 2.9V to 6V to the output voltage adjustable from 0.8V to 6V to provide excellent output voltage regulation.

The APW7324 is equipped with an automatic Skip/PWM mode operation. At light load , the IC operates in the Skip mode to reduce the switching losses. At heavy load, the IC works in PWM mode.

The APW7324 is also equipped with Power-on-reset, soft start, soft-stop, and whole protections (under-voltage, over-voltage, over-temperature and current-limit) into a single package.

This device, available in SOP-8P and TDFN3x3-10 packages, provides a very compact system solution external components and PCB area.
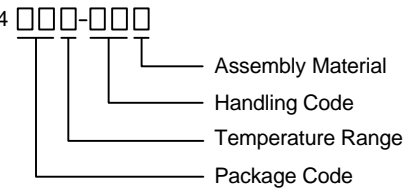
Simplified Application Circuit

Pin Configuration

SOP-8P
(Top View)

TDFN3x3-10
(Top View)
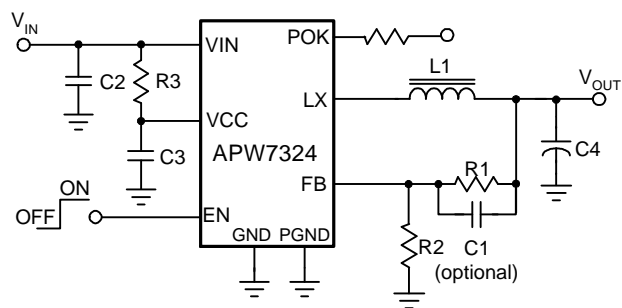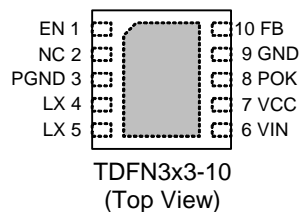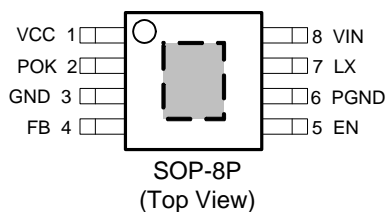
Exposed Pad (connected to GND plane for better heat dissipation

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

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Ordering and Marking Information

APW7324 □□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
   KA: SOP-8P   QB : TDFN3x3-10

Operating Ambient Temperature Range
   I : -40 to 85 ^{o}C

Handling Code
   TR : Tape & Reel

Assembly Material
   G : Halogen and Lead Free Device

APW7324 KA:	APW7324 XXXXX	XXXXX - Date Code	APW7324 QB:	APW 7324 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}, V_{CC}	VIN and VCC Input Voltage	-0.3 ~ 7	V
V_{LX}	LX to GND Voltage	-1 ~V_{CC}+0.3	V
	FB, EN, POK to GND Voltage	-0.3 ~ 6.5	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	150	^{o}C
T_{STG}	Storage Temperature	-65 ~ 150	^{o}C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	^{o}C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2)	50	^{o}C/W
θ_{JC}	Junction-to-Case Resistance in Free Air (Note 3)	10	^{o}C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of SOP-8P is soldered directly on the PCB.
Note 3: The case temperature is measured at the center of the exposed pad on the underside of the SOP-8P package.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{CC}	VCC Supply Voltage	2.9~ 6	V
V_{IN}	VIN Supply Voltage	2.5~6	V
V_{OUT}	Converter Output Voltage	0.8~6	V
I_{OUT}	Converter Maximum Output Current	4	A
T_A	Ambient Temperature	-40 ~ 85	^oC
T_J	Junction Temperature	-40 ~ 125	^oC

Note 4: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{CC}=V_{IN}=5V$, $V_{OUT}=3.3V$ and $T_A=-40~85^oC$. Typical values are at $T_A=25^oC$.

| Symbol	Parameter	Test Conditions	APW7324			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VCC}	VCC Supply Current	$V_{FB}=0.7V$	-	460	-	µA
I_{VCC_SD}	VCC Shutdown Supply Current	EN=GND	-	-	20	µA
POWER-ON-RESET (POR)						
	VCC POR Voltage Threshold	V_{CC} Rising	-	2.7	-	V
	VCC POR Voltage Hysteresis	V_{CC} Falling	-	200	-	mV
	VCC Debounce Time		-	10	-	µs
	VIN POR Voltage Threshold	V_{IN} Rising	-	2.3	-	V
	VIN POR Voltage Hysteresis	V_{IN} Falling	-	50	-	mV
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage		-	0.8	-	V
		All temperature	-1	-	+1	%
	Output Accuracy	$I_{OUT}=10mA~3A$, $V_{CC}=2.9~5V$	-1.5	-	+1.5	%
OSCILLATOR and DUTY CYCLE						
F_{OSC}	Oscillator Frequency		425	500	575	KHz
	Maximum Converter's Duty	$V_{FB}=0.7V$	-	100	-	%
	Minimum on Time		-	70	-	ns
POWER MOSFET						
	High Side MOSFET Resistance	$V_{CC}=V_{IN}=5V$, $I_{LX}=0.5A$, $T_A=25^oC$	-	85	115	mΩ
	Low Side MOSFET Resistance	$V_{CC}=V_{IN}=5V$, $I_{LX}=0.5A$, $T_A=25^oC$	-	75	105	mΩ

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $V_{CC}=V_{IN}=5V$, $V_{OUT}=3.3V$ and $T_A=-40~85^oC$. Typical values are at $T_A=25^oC$.

| Symbo	Parameter	Test Conditions	APW7324			Unit
			Min.	Typ.	Max.	
CURRENT -MODE PWM CONVERTER						
Gm	Error Amplifier Transconductance		-	680	-	µA/V
	Error Amplifier DC Gain	COMP=NC	-	50	-	dB
	Current Sense Resistance		-	400	-	mΩ
T_D	Dead Time		-	20	-	ns
PROTECEIONS						
I_{LIM}	High Side MOSFET current-limit	Peak Current	5	6	7	A
T_{OTP}	Over-temperature Trip Point		-	160	-	°C
	Over-temperature Hysteresis		-	50	-	°C
	Over- Voltage Protection Threshold		120	125	130	%V_{REF}
	OVP Debounce Time		-	3	-	µs
	Under-Voltage Protection Threshold		45	50	55	%V_{REF}
	UVP Debounce Time		-	3	-	µs
	Low Side Switch Current-Limit	From Drain to Source	-1.6	-1.9	-2.2	A
SOFT-START, ENABLE and INPUT CURRENTS						
	Soft Start Time		-	2.5	-	ms
	EN Enable Threshold Voltage	V_{EN} Rising	0.8	-	1.3	V
	EN Threshold Hysteresis		-	0.15	-	V
	EN Pull High Resistance		-	300	-	KΩ
POWER GOOD						
	POK Threshold	POK in from lower (POK goes high)	85	87.5	90	%V_{OUT}
		POK low hysteresis	-	5	-	%V_{OUT}
		POK in from higher (POK goes high)	110	112.5	115	%V_{OUT}
		POK high hysteresis	-	5	-	%V_{OUT}
	POK Pull Low Resistance		-	1	-	KΩ
	POK Low-to-High Debounce Time		-	0.5	-	ms

Typical Operating Characteristics
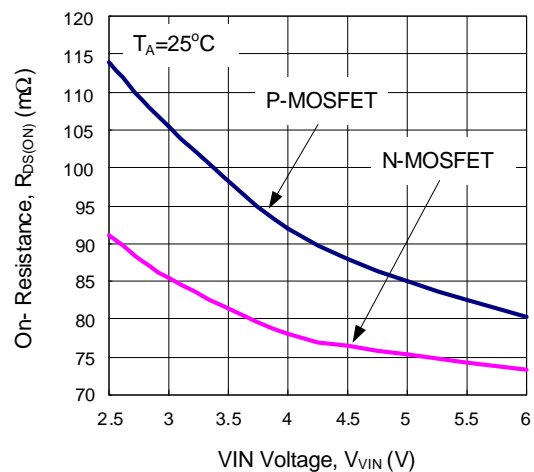
Efficiency vs. Output Current
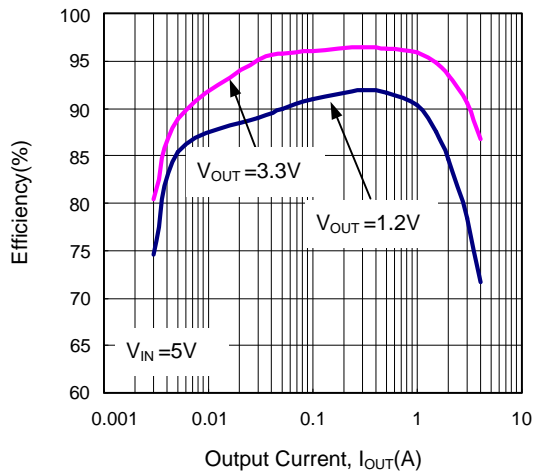
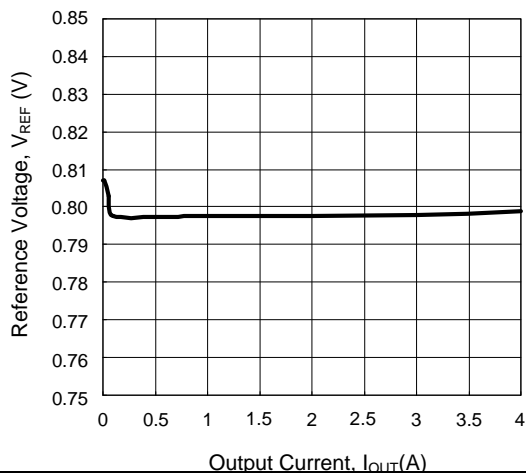**VCC Supply Current vs. VCC Supply Voltage**
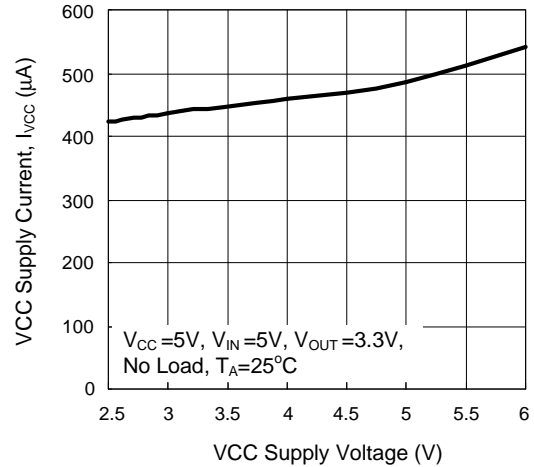
High Side MOSFET Current Limit Threshold vs. VIN Voltage
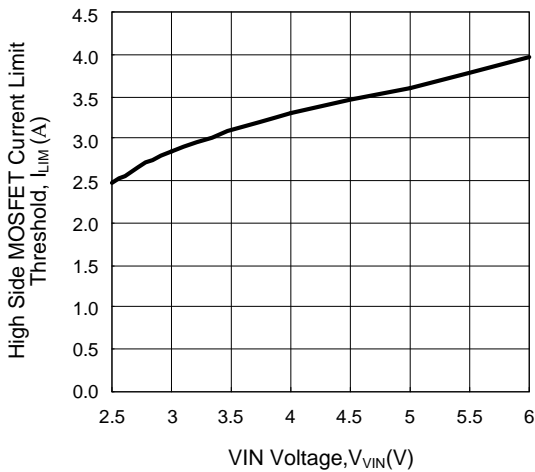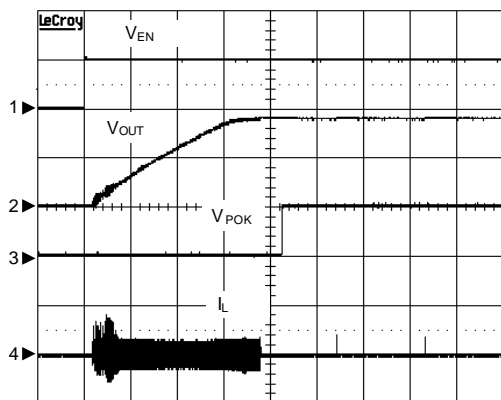

On-Resistance vs. VIN Voltage

Reference Voltage vs. Output Current

Operating Waveforms

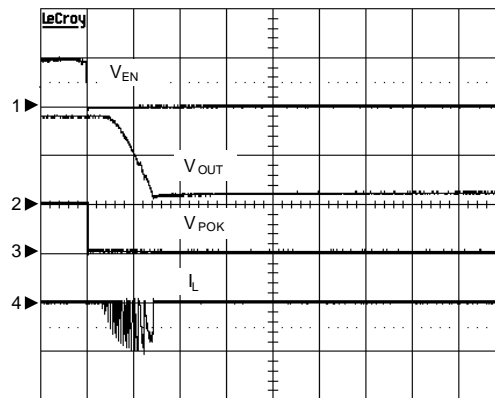The test condition is APW7324, $V_{IN}=V_{CC}=5V$, $V_{OUT}=1.8V$, $C_{OUT}=22\mu Fx2$, L=2.2μH, $T_A=25^{\circ}C$ unless otherwise specified.
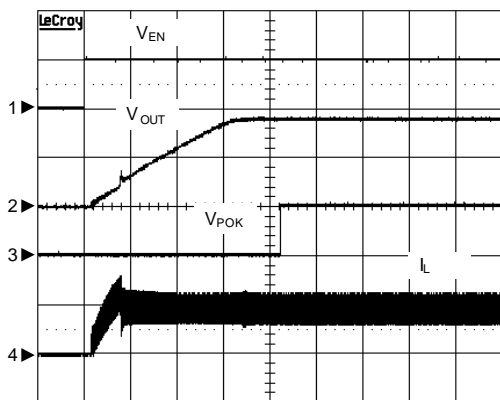
Enable without Loading

No load, EN Power On
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 2A/Div, DC
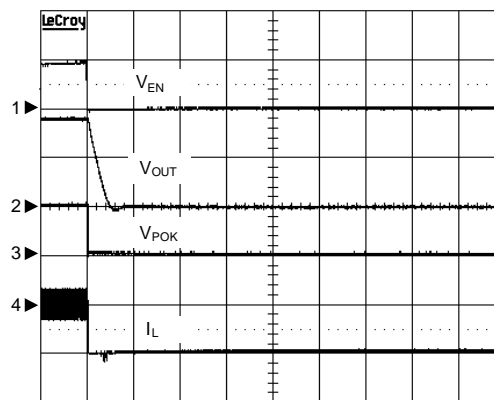TIME: 1ms/Div

Shutdown without Loading

No load, EN Power Off
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 2A/Div, DC
TIME: 100μs/Div

Enable with 2A Loading

$I_{OUT}=2A$, EN Power On
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 2A/Div, DC
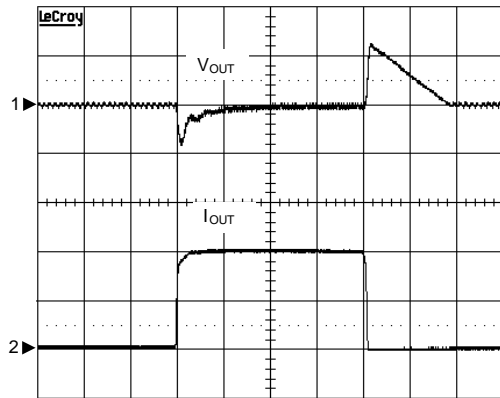TIME: 1ms/Div

Shutdown with 2A Loading

$I_{OUT}=2A$, EN Power Off
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 2A/Div, DC
TIME: 100μs/Div

Operating Waveforms

The test condition is APW7324, $V_{IN}=V_{CC}=5V$, $V_{OUT}=1.8V$, $C_{OUT}=22\mu Fx2$, L=2.2μH, $T_A=25^oC$ unless otherwise specified.

Load Transient

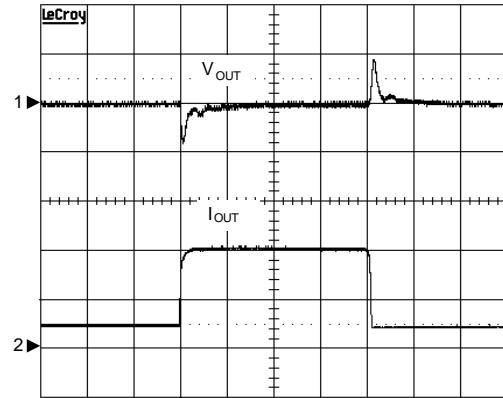I_{OUT}=100mA-4A-100mA, Slew Rate=1A/μs

CH1: V_{OUT}, 200mV/Div, offset=1.8V
CH2: I_{OUT}, 2A/Div, DC
TIME: 50μs/Div

Load Transient

I_{OUT}=1A-4A-1A, Slew Rate=1A/μs

CH1: V_{OUT}, 200mV/Div, offset=1.8V
CH2: I_{OUT}, 2A/Div, DC
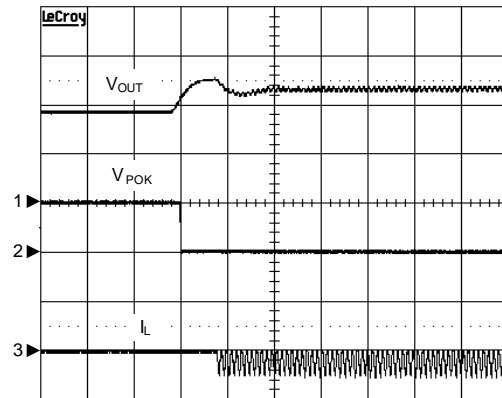TIME: 50μs/Div

Current Limit
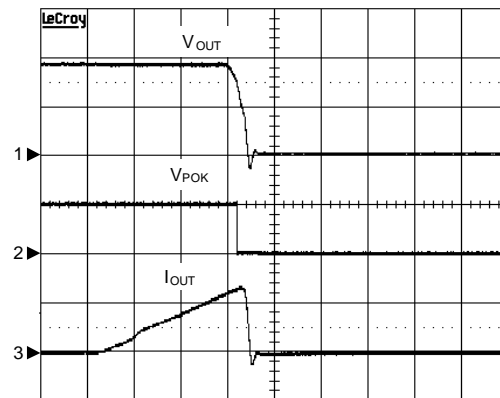
CH1: V_{OUT} ,1V/Div, DC
CH2: V_{POK}, 5V/Div, DC
CH3: I_{OUT}, 5A/Div, DC
TIME: 200μs/Div

Over Voltage Protection

No Load, a 2.5V power source is externally attached to V_{OUT}
CH1: V_{OUT}, 1V/Div, DC
CH2: V_{POK}, 5V/Div, DC
CH3: I_L, 2A/Div, DC
TIME: 50μs/Div

Operating Waveforms

The test condition is APW7324, V_{IN}=V_{CC}=5V, V_{OUT}=1.8V, C_{OUT} =22μFx2, L=2.2μH, T_A= 25°C unless otherwise specified.

Normal Operation in Ligh Load
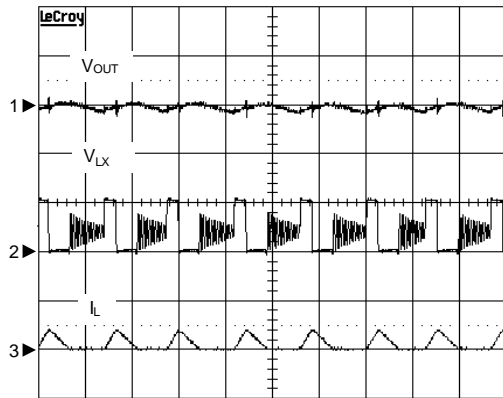
I_{OUT}=200mA

CH1: V_{OUT}, 50mV/Div, offset=1.8V
CH2: V_{LX}, 5V/Div, DC
CH3: I_{LX}, 2A/Div, DC
TIME: 2μs/Div

Normal Operation in Heavy Load

I_{OUT}=4A

CH1: V_{OUT}, 50mV/Div, offset=1.8V
CH2: V_{LX}, 5V/Div, DC
CH3: I_{LX}, 5A/Div, DC
TIME: 2μs/Div

Pin Description

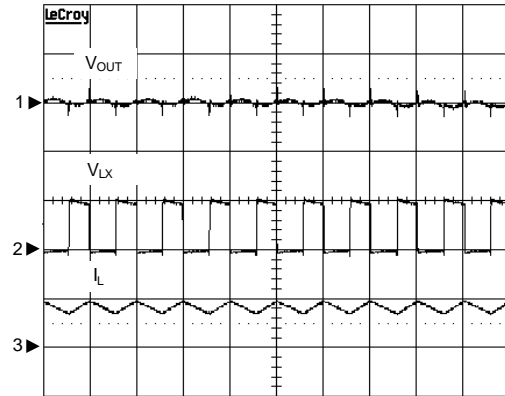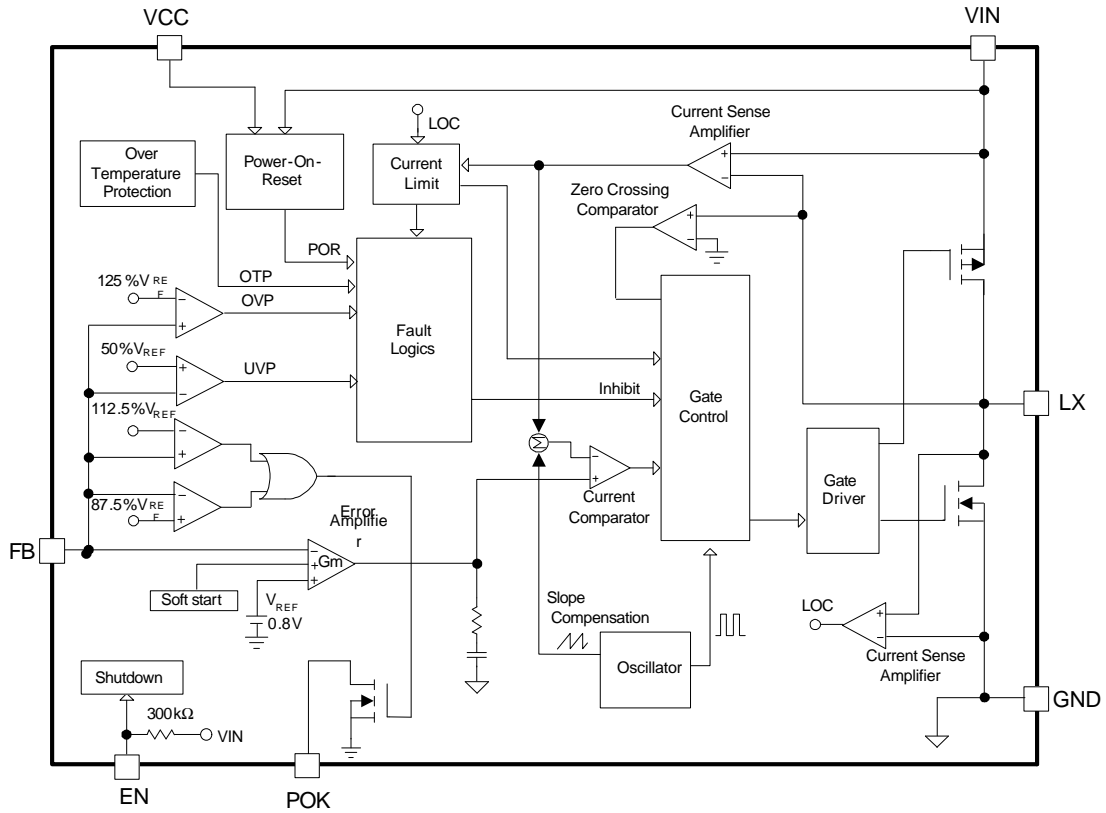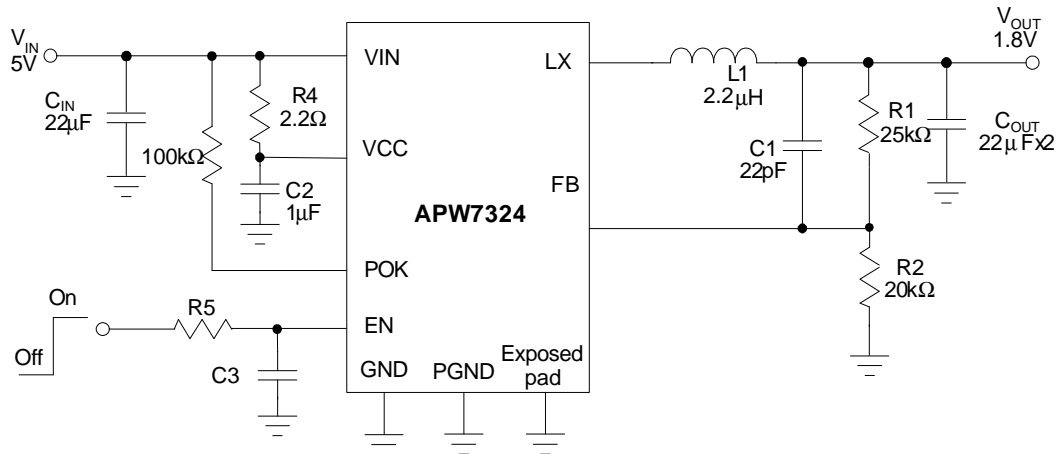| Pin			Function
NO.		Name	
SOP-8P	TDFN3x3-10		
1	7	VCC	Signal Input. VCC supplies the control circuitry, gate drivers. Connecting a ceramic bypass capacitor from VCC to GND to eliminate switching noise and voltage ripple on the input to the IC.
2	8	POK	Power Good Output. This pin is open-drain logic output that is pulled to ground when the output voltage is not within ±12.5% of regulation point. The POK pin, if used, needs an external pull high resistor in the range of 30kΩ~100kΩ
3	9	GND	Ground. Power and signal ground.
4	10	FB	Output Feedback Input. The APW7324 senses the feedback voltage via FB and regulates the voltage at 0.8V. Connecting FB with a resistor-divider from the converter's output sets the output voltage.
5	1	EN	Enable Input. EN is a digital input that turns the regulator on or off. Driving the EN high turns on the regulator, otherwise, driving it low turns it off. The EN pin is internally pulled high via a 300k resistor.
6	3	PGND	Power Ground.
7	4, 5	LX	Power Switching Output. LX is the Junction of the high-side and low-side Power MOSFETs to supply power to the output LC filter.
8	6	VIN	Power Input. VIN supplies the step-down converter switches.
9	11	Exposed Pad	Exposed pad. Connect the exposed pad to the system ground plane with large copper area for dissipating heat into the ambient air.

Block Diagram

Typical Application Circuit

APW7324

Function Description

VCC and VIN Power-On-Reset (POR)

TThe APW7324 keeps monitoring the voltage on VIN and VCC pins to prevent wrong logic operations which may occur when VIN or VCC voltage is not high enough for internal control circuitry to operate. The VCC POR rising threshold is 2.7V (typical) with 0.2V hysteresis and VIN POR rising threshold is 2.3V with 0.05V hysteresis. During startup, the VCC and VIN voltage must exceed the POR threshold. Then the IC starts a starts-up process and ramps up the output voltage to the voltage target.

Output Under-Voltage Protection (UVP)

In the operational process, if a short-circuit occurs, the output voltage will drop quickly. Before the current-limit circuit responds, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the IC shuts down converter's output.

The under-voltage threshold is 50% of the nominal output voltage. The under-voltage comparator has a built-in 3μs noise filter to prevent the chips from wrong UVP shutdown being caused by noise. The APW7324 will be latched after under-voltage protection.

Over-Voltage Protection (OVP)

The over-voltage function monitors the output voltage by FB pin. When the FB voltage increases over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over-voltage protection comparator will force the low-side MOSFET gate driver high. This action actively pulls down the output voltage and eventually attempts to blow the internal bonding wires. As soon as the output voltage is within regulation, the OVP comparator is disengaged. The chip will restore its normal operation.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7324. When the junction temperature exceeds $T_J = 160°C$, a thermal sensor turns off the both power MOSFETs, allowing the devices to cool.

The thermal sensor allows the converters to start a start-up process and to regulate the output voltage again after the junction temperature cools by 50°C. The OTP is designed with a 50°C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the APW7324.

Current-Limit Protection

The APW7324 monitors the output current, flows through the high-side and low-side power MOSFETs, and limits the current peak at current-limit level to prevent the IC from damaging during overload, short-circuit and over-voltage conditions. Typical high side power MOSFET current limit is 6A, and low side MOSFET current limit is 1.9A.

Soft-Start

The APW7324 has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during start-up. During soft-start, an internal voltage ramp connected to one of the positive inputs of the error amplifier, rises up from 0V to 0.95V to replace the reference voltage (0.8V) until the voltage ramp reaches the reference voltage. During soft-start without output over-voltage, the APW7324 converter's sinking capability is disabled until the output voltage reaches the voltage target.

Soft-Stop

At the moment of shutdown controlled by EN signal, under-voltage event or over-temperature protection, the APW7324 initiates a soft-stop process to discharge the output voltage in the output capacitors. Certainly, the load current also discharges the output voltage. During soft-stop, the internal voltage ramp (V_{RAMP}) falls down from 0.95V to 0V to replace the reference voltage. Therefore, the output voltage falls down slowly at the light load. After the soft-stop interval elapses, the soft-stop process ends and the IC turns on the low-side power MOSFET.

Enable and Shutdown

Driving EN to ground places the APW7324 in shutdown. In shutdown mode, the internal power MOSFETs turns off, all internal circuitry shuts down and the quiescent supply current reduces to less than 20μA.

Function Description (Cont.)

Power Good Indicator

POK is actively held low in shutdown and soft-start status. In the soft-start process, the POK is an open-drain. When the soft-start is finished, the POK is released. In normal operation, the POK window is from 87.5% to 112.5% of the converter reference voltage. When the output voltage has to stay within this window, POK signal will become high after 0.5ms internal delay. When the output voltage outruns 82.55% or 117.5% of the target voltage, POK signal will be pulled low immediately. In order to prevent false POK drop, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient.

Application Information

Input Capacitor Selection

Because buck converters have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes. Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 22µF input capacitor is sufficient. It can be increased without any limit for better input voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the input and GND pin of the device for better performance.

Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, ΔI_L, is 40% of maximum output current. The recommended inductor value can be calculated as below:

$$L \geq \frac{V_{OUT}\left(1 - \dfrac{V_{OUT}}{V_{IN}}\right)}{F_{SW} \cdot \Delta I_L}$$

$$I_{L(MAX)} = I_{OUT(MAX)} + 1/2 \times \Delta I_L$$

To avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

Output Voltage Setting

In the adjustable version, the output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as shown in "Typical Application Circuits". A suggestion of maximum value of R2 is 300kΩ to keep the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage can be calculated as below:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R1}{R2}\right)$$
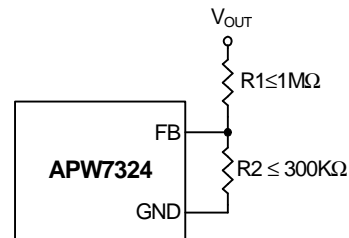
Output Capacitor Selection

The current-mode control scheme of the APW7324 allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.
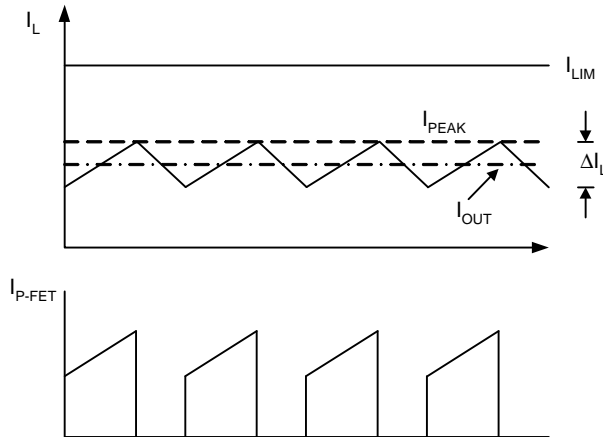
$$\Delta V_{OUT} \cong \frac{V_{OUT} \cdot \left(1 - \dfrac{V_{OUT}}{V_{IN}}\right)}{F_{SW} \cdot L} \cdot \left(ESR + \frac{1}{8 \cdot F_{SW} \cdot C_{OUT}}\right)$$

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.
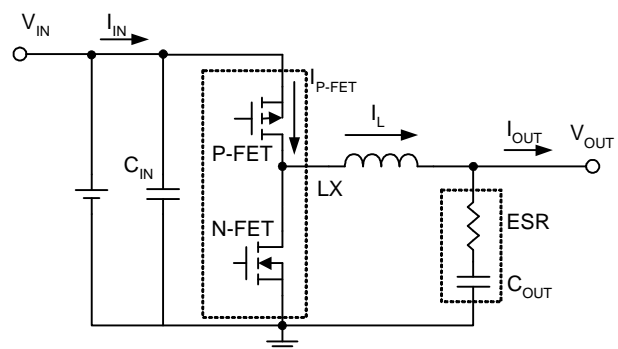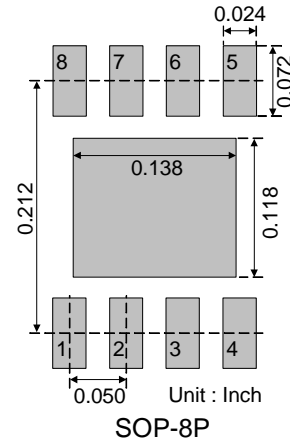
Application Information (Cont.)

Output Capacitor Selection (Cont.)

Recommended Minimum Footprint

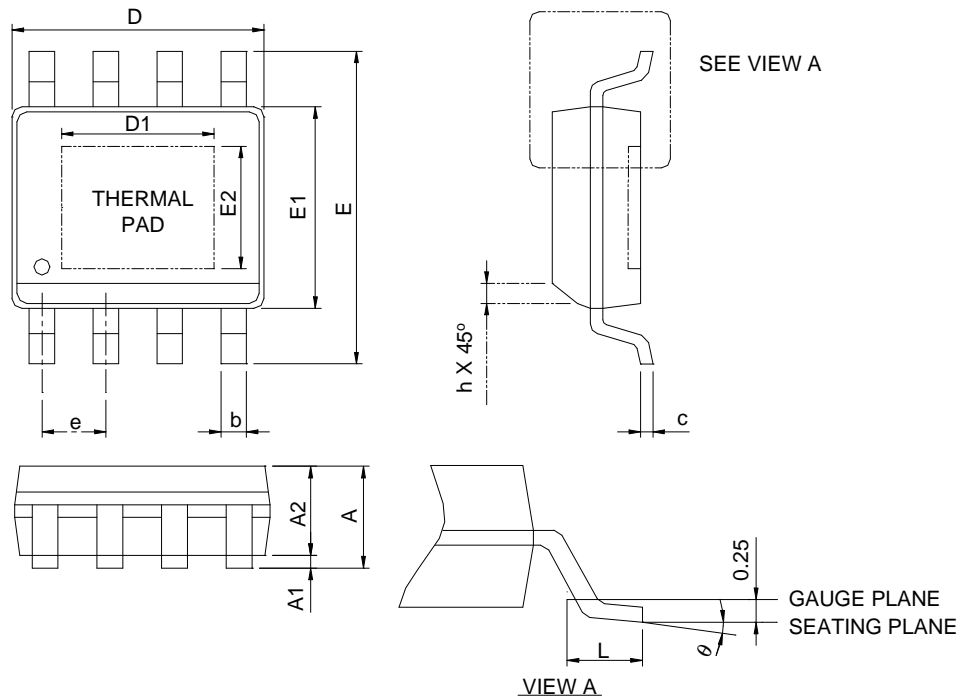**SOP-8P**

Layout Considerations

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VIN and GND. Connect the capacitor and VIN/GND with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/GND to capacitor less than 2mm respectively is recommended.

2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the LX pin to minimize the noise coupling into other circuits.

3. The output capacitor should be place closed to VOUT and GND.

4. Keep the sensitive small signal nodes (FB) away from switching nodes (LX) on the PCB. Therefore place the feedback divider and the feedback compensation network close to the IC to avoid switching noise. Connect the ground of feedback divider directly to the GND pin of the IC using a dedicated ground trace.

5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

TDFN3X3-10
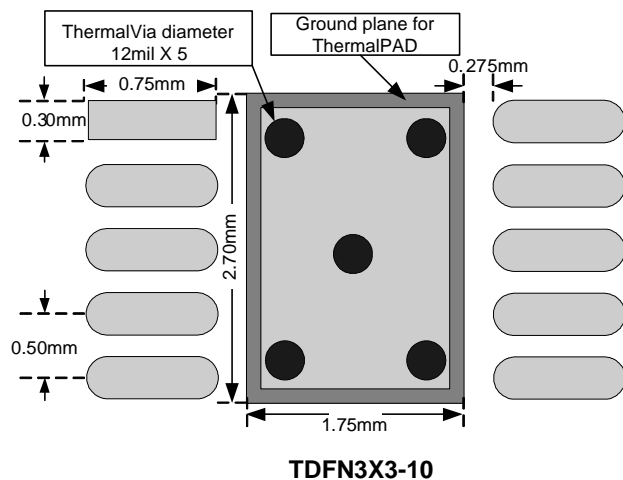
Package Information

SOP-8P

SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0ºC	8ºC	0ºC	8ºC

Note : 1. Followed from JEDEC MS-012 BA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

TDFN3x3-10
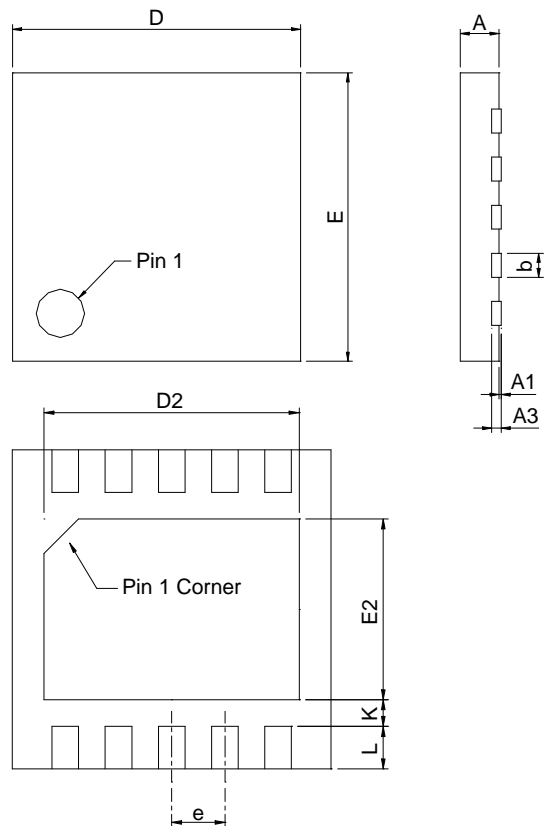
SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Carrier Tape & Reel Dimensions
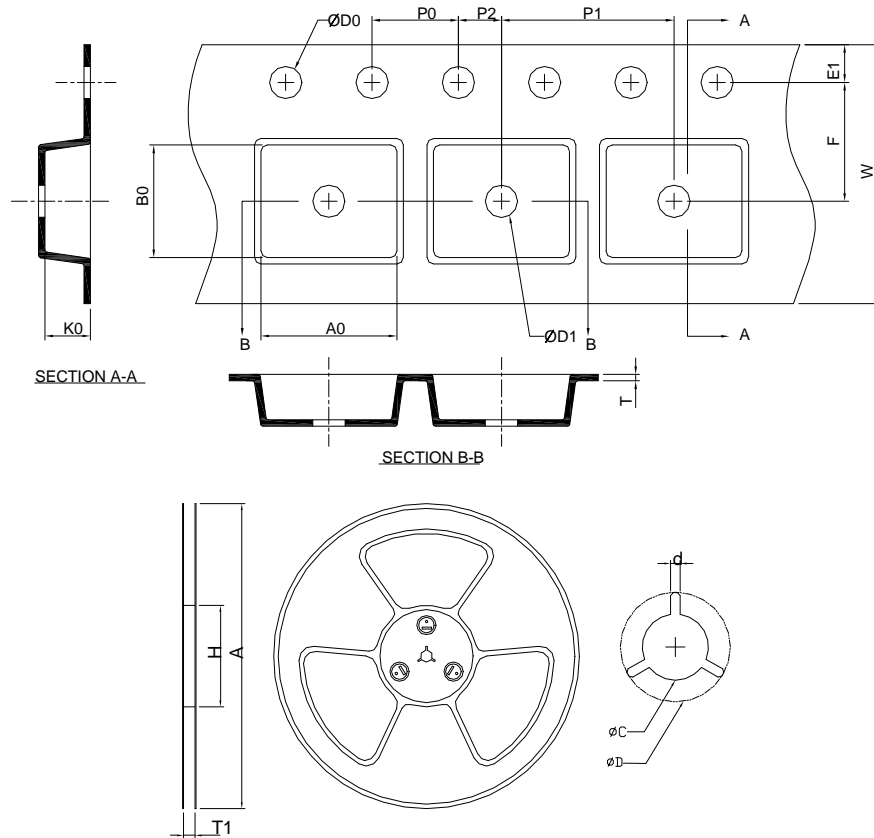
| Application	A	H	T1	C	d	D	W	E1	F
SOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TDFN3x3-10	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOP- 8P	Tape & Reel	2500
TDFN-3x3-10	Tape & Reel	3000

Taping Direction Information

SOP-8P
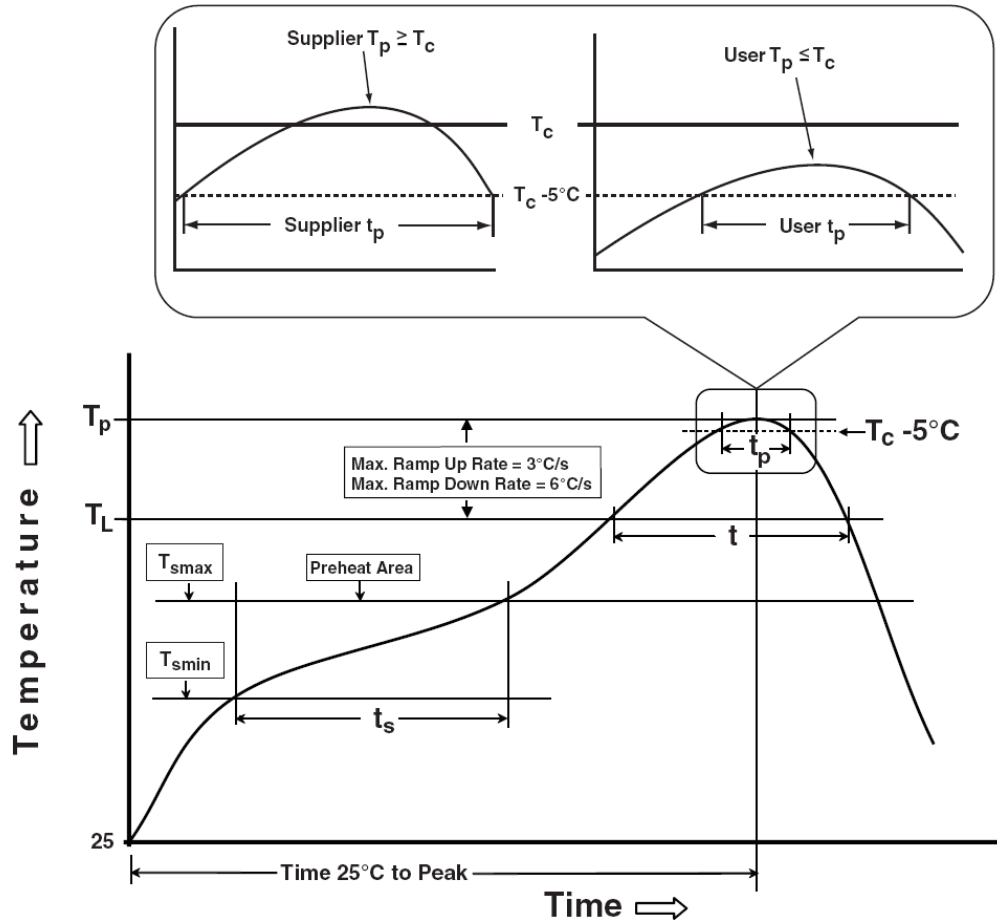
USER DIRECTION OF FEED

TDFN3x3-10

USER DIRECTION OF FEED
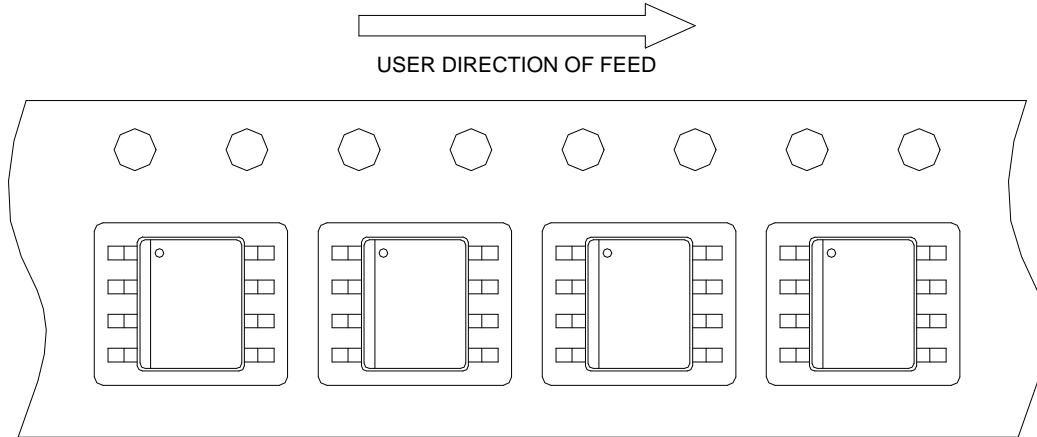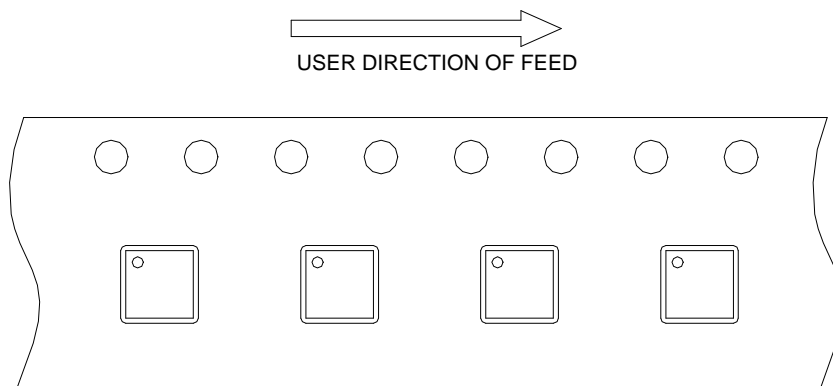
Classification Profile

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM 2KV
MM	JESD-22, A115	VMM 200V
Latch-Up	JESD 78	10ms, 1_{tr} 100mA

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