T-42-11-09

LZ93 Series CMOS Gate Array

■ Description

The LZ93 series CMOS gate array provides 300 to 5000 gates of line up with high speed and low power consumption.

It is fabricated using 1.6 μm CMOS silicon gate/ double metal technology.

■ Features

1. CMOS process
2. Number of gates : 300, 600, 1000, 1100, 1600, 2200, 3000, 4000, 5000
3. Internal gate delay : 1.7ns/gate
4. Macro cell : 95 cells
   74LS cell : 126 cells
5. I/O level : CMOS/TTL compatible
6. Supply voltage : 5V±5% (TTL interface)
   5V±10% (CMOS interface)

■ Line Up

Parameter		LZ93300	LZ93600	LZ931000	LZ931100	LZ931600	LZ932200	LZ933000	LZ934000	LZ935000
Gate count (2 input NAND conversion)		300	600	1010	1111	1596	2240	3145	4009	5000
I/O buffer count		37	51	67	77	97	97	112	128	140
Pin count		40	54	70	80	100	100	120	136	150
Process		1.6 μm CMOS silicon gate, double metal								
Delay time	Internal gate	1.7ns/gate (F.O.=3, Wiring length : 2mm)								
	Input buffer	TTL level : 2.4ns/CMOS level : 2.9ns (F.O.=3, Wiring length : 2mm)								
	Output buffer	4.0ns (C_L=20pF)								
I/O level		TTL level/CMOS level								
Supply voltage		5V±5% (TTL interface)/5V±10% (CMOS interface)								