16-Bit Floating Input, Programmable Gain, Analog Processor

Providing Very High Isolation

Introduction

The MP2316A is a floating input, programmable gain analog converter-processor front end. It provides very high isolation between high resolution digital systems and large numbers of multiplexed analog input signals, especially in high common-mode voltage industrial environments such as process control, data acquisition systems and HVAC systems.

The MP2316A consists of an input stage, a 13-gain programmable gain amplifier, a buffered dual-slope integrating A/D, a precision reference, an isolated DC/DC converter, and all the circuits required to complete the analog portion of a precision, 16-bit data acquisition system. The entire interface to the digital host system is through three transformer-isolated lines; two inputs for control and one output line for conversion results, which are in the form of an elapsed time between a pulse on one control line and the End-of-Conversion (EOC) signal from the converter.

The high isolation of the analog inputs from the digital output is achieved by an intrinsic CMRR of 90 dB due to high quality magnetic isolators, an overall CMRR of 150 dB, a 60 dB line frequency normal mode rejection ratio, and up to ±500V (AC peak and DC) of common mode isolation.

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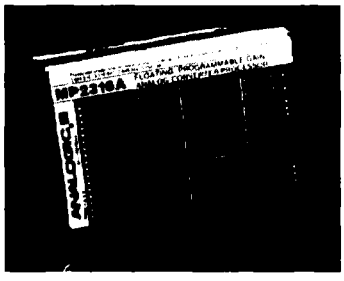

Features

- ❑ Programmable Gain Amplifier Provides 13 Switch Selectable Full Scale Ranges from ±10 mV to ±50V
- ❑ Floating Isolated Input Provides 500V Isolation from Signal Common to Output Common
- ❑ 150 dB Common Mode Rejection Ratio
- ❑ Guarded Input Allows Multiplexing of Input Lead Shields
- ❑ Time Interval Output Proportional to Input Voltage
- ❑ ±0.001% FSR Linearity Consistent Performance with 16-Bit Resolution
- ❑ Isolated Output Voltages Provides Power for Sensors
- ❑ High Stability; 0.3 µV/°C Offset, 12 ppm/°C Range
- ❑ Flexible Power Supply Requirement +12V to +15V
- ❑ Small Size – 2" x 3" x 0.51"

Applications

- ❑ Industrial Process Control
- ❑ Heating, Ventilating and Air Conditioning (HVAC)
- ❑ Thermocouple Measurement
- ❑ Bridge Measurement
- ❑ Data Acquisition Systems

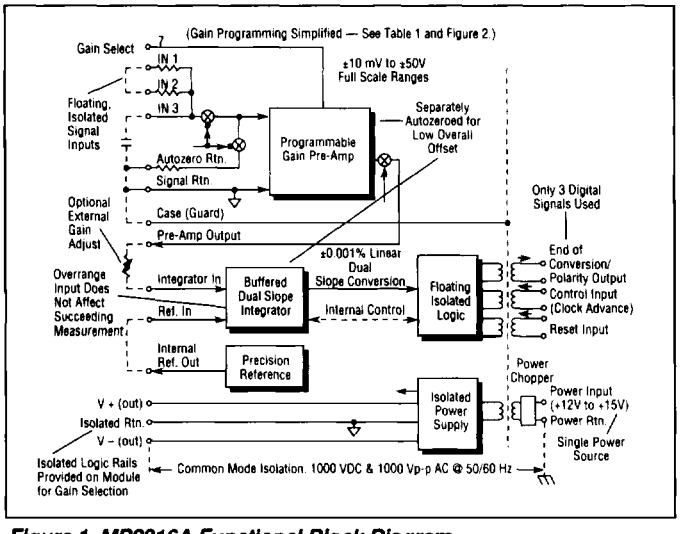

Figure 1. MP2316A Functional Block Diagram.

MP2316A
Specifications[1]

ANALOG INPUT

Configuration
Floating, isolated, three wire

Full Scale Range (FSR)
Selectable ranges from ±10 mV to ±50V (See Table 1)

Maximum Common Mode Voltage
±500 VDC or AC peak, (SIGNAL RETURN to POWER RETURN) [2]

Common Mode Rejection Ratio
150 dB minimum at 50 or 60 Hz, with integration period within ±0.05% of the power line frequency

Input Impedance
FSR ≤ ±5V – 100 MΩ minimum
FSR > ±5V – 1 MΩ nominal

Bias Current
300 pA, typical [3]

Maximum Input
264 VAC RMS continuous without damage [2,4]

ISOLATED VOLTAGE OUTPUTS

Output Voltage
+8V nominal (V+); –10V nominal (V–); the amount of current drawn from V+ must never exceed that drawn from V– by more than 3 mA; the total current drawn from both outputs must not exceed 6 mA.

ACCURACY

Output Coding
Time interval proportional to the magnitude of the input voltage, plus sign decision based on polarity of input

Resolution
Depends on count rate of external counter; up to 16 bits (15 magnitude bits plus sign bit) achievable with appropriate external logic

Transfer Accuracy
Consistent with 15-bit resolution, with external calibration adjustment

Differential Non-linearity
±0.001% FSR, typical

Integral Non-linearity
±0.006% FSR, typical

Offset
RTI – Externally adjustable to zero [5]
RTO – ±15 ppm FSR, maximum [6]

Noise
3 µV RMS or 10 ppm FSR RMS maximum, whichever is greater; assumes a 1.5 µF capacitor (Cx) across IN3 and SIGNAL RETURN per Figure 2

STABILITY

Range Tempco (0°C to 70°C)

FSR ≤ ±5V
±12 ppm FSR/°C typical,
±25 ppm FSR/°C maximum

FSR > ±5V
±20 ppm FSR/°C typical,
±30 ppm FSR/°C maximum

RTI Offset Tempco (0°C to 70°C)
±0.3 µV/°C typical

Power Supply Rejection Ratio
±0.002% FSR/percent power supply change

Recommended Recalibration Intervals
6 months

DYNAMIC PERFORMANCE

Input Integration Time (Phase 1)
1/60 second ±0.05% when synchronized to 60 Hz power line; 1/50 second ±0.05% when synchronized to 50 Hz power line [7]

Full Scale Reference Integration Time (Phase 2)
One-half the input integration time, nominal

Integrator Autozero Time (Phase 3)
1.9 µs, minimum, no maximum limit

Time to recover from Overrange Input
1.9 µs [8]

Overall Throughput Rate
Up to 37 measurements/second when synchronized to 60 Hz line; Up to 31 measurements/second when synchronized to 50 Hz line

DIGITAL INPUT/OUTPUT

(See Figure 7)

Input Lines
12V CMOS compatible; negative pulses

Reset Line
A negative pulse on this line initiates the autozero phase; low level is active; 200 ns pulse width minimum, 3 µs maximum [9]

Clock Advance Line (See Figure 6)
Negative-going (leading) edge is active; each pulse must be low for 100 ns minimum

First Pulse (Φ1)
Initiates input integration

Second Pulse (Φ2)
Strobes out the Polarity (decision) Pulse

Third Pulse (Φ3)
Initiates reference integration

Output Line
12V CMOS-compatible, positive pulses; positive-going (leading) edge is active; 100 ns minimum pulse width, 4 µs maximum; 100 ns rise and fall times, typical

Polarity Pulse
Occurrence of an output pulse upon receipt of the polarity strobe (Φ2) indicates that the input signal has a negative polarity; absence of a pulse at this time indicates positive polarity

End-of-Conversion (EOC) Pulse
The elapsed time from the start of reference integration until EOC occurs is directly proportional to the magnitude of the input signal plus a constant 1 µs, nominal, delay

POWER SUPPLY REQUIREMENTS

+12V to +15V
80 mA typical, 125 mA maximum

ENVIRONMENTAL & MECHANICAL

Operating Temperature Range
0°C to +70°C

Storage Temperature Range
–25°C to +85°C

Relative Humidity
0 to 80%, non-condensing to 40°C

Dimensions
2.0" x 3.0" x 0.51"
(50.8 x 76.2 x 12.9 mm)

Shielding
Electrostatic 6 sides, Electromagnetic 5 sides

Case Potential
At the GUARD potential (equals common mode potential referenced to POWER RETURN)

NOTES:

1. Assumes a 1 kΩ gain adjust potentiometer is connected per Figure 1.
2. With Cx = 1.5 µF installed between AUTOZERO RETURN and IN3, or with external diode input protection circuit per Figure 2.
3. 500 pA maximum at 40°C; doubles every 10°C above 40°C.
4. Input 1 to SIGNAL RETURN; INPUT 2 to SIGNAL RETURN.
5. ±50 µV maximum, externally adjustable to zero via AUTOZERO RETURN (See Autozero Connection Section).
6. Externally adjustable via 1 µs nominal delay between Clock Advance Φ3 and start of user's counter.
7. Sign decision is made immediately prior to completion of the input integration phase.
8. Assumes that Reset is issued whenever EOC does not occur within the nominal full scale integration time.
9. Measured between 50% points.

All specifications guaranteed at 25°C unless otherwise noted. Specifications subject to change without notice.

Continued from page 91.

The programmable gain amplifier (PGA) provides a simple and flexible scheme for selecting a ±10 mV to ±50V full scale range while maintaining full isolation. Gain may be changed by applying the MP2316A's own isolated auxiliary voltage outputs, via switches, to the gain programming pins (see GAIN PROGRAMMING). An autozero return from the PGA allows long-term system offset drifts to be essentially eliminated. Both the PGA and the integrator are autozeroed between conversions, so that DC offset is less than 50 µV RTI (adjustable to zero).

By fully implementing the most difficult (analog) functions, the MP2316A is an ideal starting point for designing a wide variety of low speed, precision data acquisition systems. By parallel connection of multiple units, higher throughputs can be achieved.

USING THE MP2316A

Gain Programming

The three gain stages shown in Figure 2 allow selecting any of the 13 gains from 0.05 to 250 inclusive, providing full scale ranges from ±50V to ±10 mV. The external potentiometer connections shown allow fine adjustment of any selected range. For example, a 1 kΩ pot provides a ±4.5% adjustment, more than adequate for obtaining either a ±1.000V FSR or a ±1.024V FSR with one basic gain selection.

Each of the gain stages may be externally configured using either switches, relays, or opto-isolators, or by any other convenient means available in the host system. The module's own floating output voltages may be used for controlling the MP2316A's internal solid-state switches, A through H, per the inset of Figure 2.

External gain and offset adjustment potentiometers, if used, can be switched similarly. It is possible, then, to configure and trim the MP2316A to provide nearly any desired full scale range(s) and/or any desired range-to-range absolute accuracy, while maintaining full isolation. When the maximum attainable accuracy is require, it is recommended that each range be calibrated individually.

Table 1. MP2316A Range Programming

	Gain Select Pin Connections [2]							
FSR [1]	A	B	C	D	E	F	H	G1 [3]
±10 mV	1	0	0	0	0	0	1	1
±20 mV	0	1	0	0	0	0	1	1
±50 mV	1	0	0	0	0	1	0	1
±100 mV	1	0	0	0	1	0	0	1
±200 mV	0	1	0	0	1	0	0	1
±1V	1	0	0	1	0	0	0	1
±2V	0	1	0	1	0	0	0	1
±2.5V	1	0	1	0	0	0	0	1
±5V	0	1	1	0	0	0	0	1
±10V	1	0	0	1	0	0	0	0.1
±20V	0	1	0	1	0	0	0	0.1
±25V	1	0	1	0	0	0	0	0.1
±50V	0	1	1	0	0	0	0	0.1

Notes to Table 1.

1. Full scale ranges (FSRs) specified with 500Ω nominal between gain adjust terminals @ 25°C ±5°C. A resistance change of 0 to 1 kΩ between gain adjust terminals results in a nominal gain change of 9%.
2. "0" denotes this pin connected to the V– isolated output; "1" denotes this pin connected to the V+ isolated output through a resistor.
3. Input Gain (see Figure 2 and Input Connections).

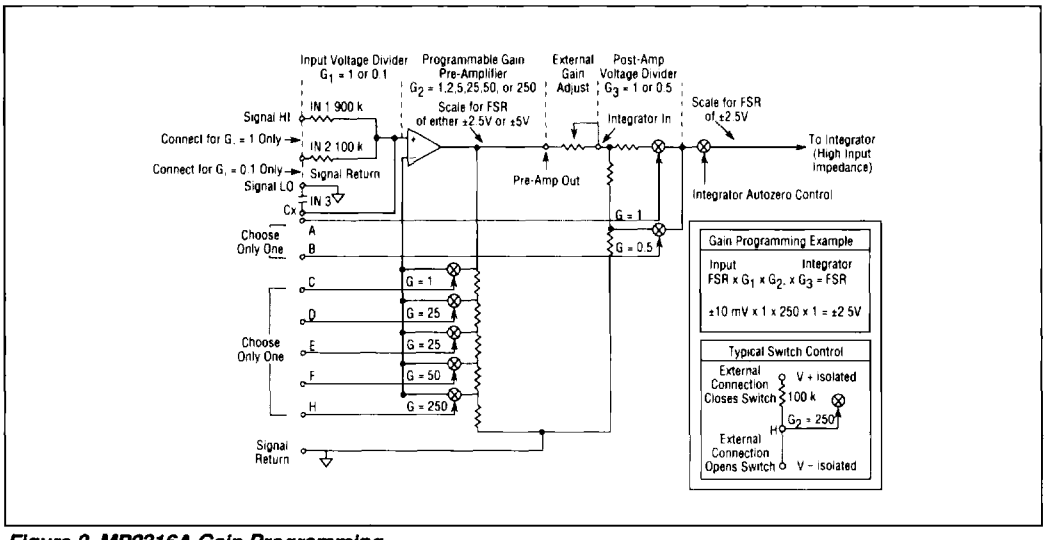

Figure 2. MP2316A Gain Programming.

INPUT CONSIDERATIONS

Input Connections

For full scale ranges larger than ±5V, the analog input signal is connected to IN1, and IN2 is externally connected to SIGNAL RETURN. In this configuration, the input stage's gain of 0.1 allows use with input signals having full scale ranges up to ±50V.

For full scale ranges nominally ≤ ±5V, the analog input signal is connected to IN2, which provides unity gain. IN1 should be tied to IN2 to prevent noise pick up. By connecting a 1.5 µF capacitor between IN3 and ground, high frequency noise filtering on any range can be accomplished. The low-pass filter thus formed (RC = 900 kΩ/1.5 µF for IN1 and RC = 100 kΩ/1.5 µF for IN2) will reduce the usable input signal bandwidth.

Case Potential

The Case (GUARD) pin may be tied to SIGNAL RETURN as shown in Figure 1, and/or to the lead shield, if one is used. If lead shields for different channels carry different potentials in the system, and the shields, are not multiplexed to the Case pin, it is recommended that each shield be tied to local earth at its sensor, while the Case pin is tied to SIGNAL RETURN. Optimum system performance will generally be obtained by using twisted shielded pair for each channel.

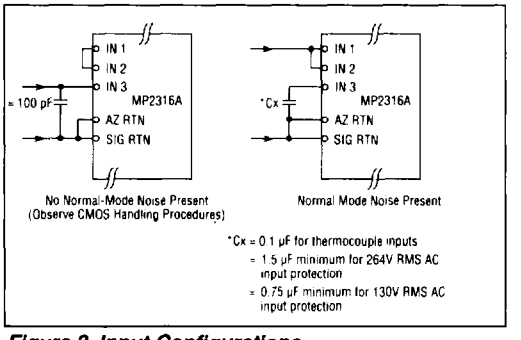

Figure 3. Input Configurations.

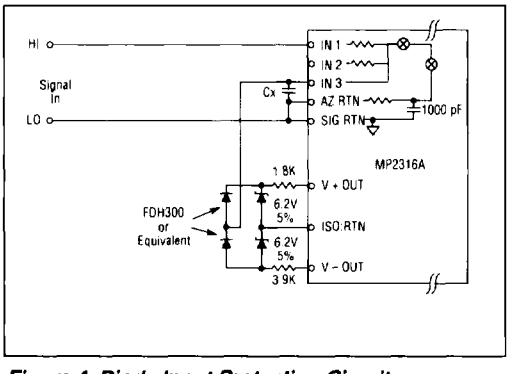

Figure 4. Diode Input Protection Circuit.

Input Overvoltage

The specifications call out a maximum continuous input without damage of 264 VAC RMS. This assumes a value for Cx of 1.5 µF connected between the IN3 and SIGNAL LO pins as shown in Figure 2. Failure to use this capacitor will result in damage to the unit under the specified input conditions. It should be noted that this capacitor will form a low-pass filter on the input (RC = 900 kΩ/1.5 µF for INPUT 1 and RC = 100 kΩ/1.5 µF for INPUT 2). This will reduce the usable signal bandwidth at the input to the A/D.

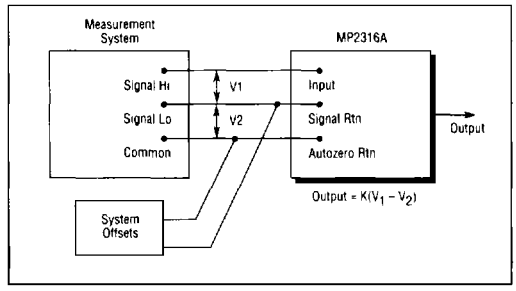

Figure 5. The MP2316A's Three-Wire Input Configuration Essentially Eliminates Long Term Sensor System Offsets.

Noise

The specification for noise performance assumes a value of 1.5 µF for Cx. If the capacitor is not used to low-pass filter the input, noise in excess of the specification can occur.

The input configuration can be modified depending on whether or not normal mode noise is present. See Figure 3.

Thermocouple Inputs

When used with thermocouple inputs, the value of Cx between IN3 and SIGNAL LO should be ≥0.1 µF to limit the input response to approximately 12 Hz.

Input Protection

It is recommended that the diode input protection circuit in Figure 4 be used to protect the MP2316A from large common mode and normal mode spikes, such as those that occur when relay contacts are switching signal sources to the MP2316A input.

Autozero Connection

Using the AUTOZERO RETURN, offsets that may occur between the SIGNAL RETURN and the common of the sensor subsystem (see Figure 5) can essentially be eliminated. The maximum offset that can be eliminated is 20% of the selected full scale range if the input voltage divider gain is set at unity. For larger full scale ranges where the input divider is set at 0.1, the maximum offset eliminated is 2% of the full scale range. A small signal potentiometer installed between SIGNAL RETURN and AUTOZERO RETURN can be used to zero the MP2316A's small (±50 µV RTI maximum) offset, per Figure 5.

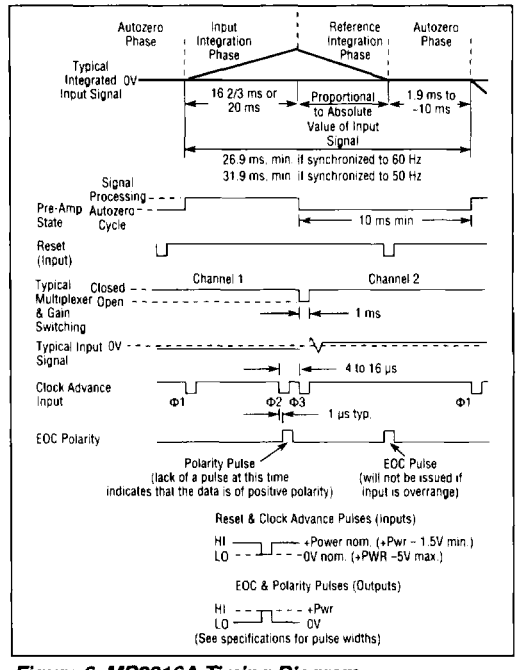

Figure 6. MP2316A Timing Diagram.

Table 2. Reference Integration Time (Linear).

	Line Frequency	
Input	60 Hz	50 Hz
–Full Scale	8.333 ms	10.000 ms
0V	0.001 ms	0.001 ms
+Full Scale	8.333 ms	10.000 ms

Isolated Output Voltages

The MP2316A is provided with isolated voltage outputs of +8V and –10V nominal. These can be used to power strain gauges, or other sensors. It is important to limit the total current drawn from both outputs to 6 mA or less, and to ensure that the amount of current drawn from the V+ output never exceeds that drawn from the V– output by more than 3 mA.

Reference Connections

The MP2316A contains its own isolated precision reference source (–4.75V). This reference is brought out as a test point (INTERNAL REFERENCE OUT), and should be jumpered to REFERENCE IN for most applications.

For true ratiometric applications, a floating external supply that excites the system's sensors may also be applied, via a buffer, to REFERENCE IN (while INTERNAL REFERENCE OUT floats). If used, such a reference should be –4.75V ±10%.

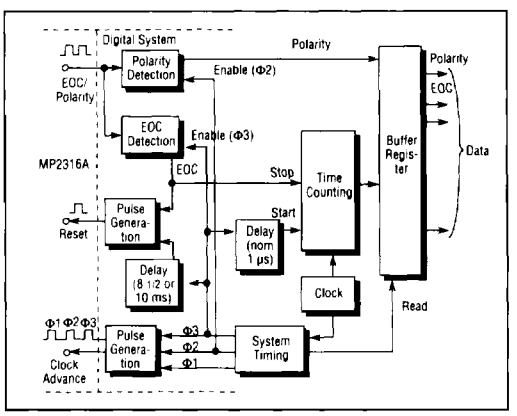

Figure 7. Applications Diagram — Functional Block Diagram of MP2316A External Control Logic, Implementable in Either Hardware/Software.

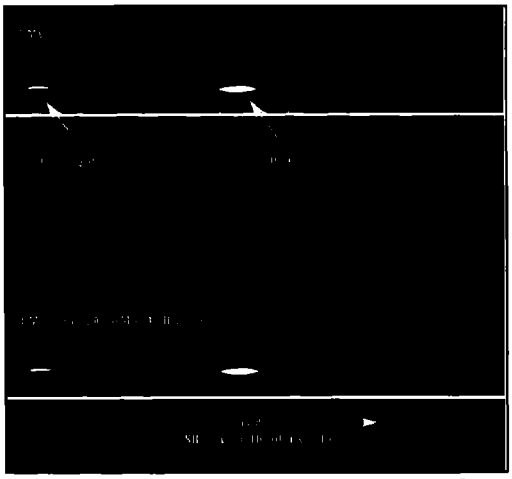

Figure 8. MP2316A Common Mode Rejection Ratio Test (360V RMS CMV, 37 Hz Measurement Rate, ±50 mV FSR).
Note: Pulse polarity inverted for display only.

The upper trace shows the Polarity and EOC pulses for a zero volt input with no common mode voltage present. The lower trace shows the same pulses when 360V RMS of CMV is present, also with a zero volt input signal. A time exposure is used to display both conversion results. In the lower trace, EOC occurs 0.5 µs later than in the upper trace. At 16-bit resolution, this shift is equivalent to 2 LSBs, or only 3 µV common mode error — on a full scale range of ±50 mV — resulting from 360V RMS CMV. Thus the CMRR measured is greater than 160 dB, 10 dB better than the MP2316A specification!

Timing and Control

The Timing Diagram (see Figure 6) shows the operation of a multiplexed data acquisition system that uses the MP2316A; the Applications Diagram (Figure 7) indicates the corresponding external logic functions. These functions can be implemented via either hardware or software, depending on the economics of the host digital system. The operational timing contains three phases summarized as follows:

1. Integrate the input signal
2. Integrate the precision reference for a maximum of one-half of the input integration time
3. Autozero the integrator

A description of operation during each of these phases follows, starting with the autozero phase.

Autozero Phase

Each measurement cycle begins with a pulse on the RESET line, which initiates autozeroing of the precision integrator. A minimum of 1.9 ms should be allowed for autozeroing. If the MP2316A input is overranged, the autozero circuit will ensure recovery within this time.

Input Integration Phase

When the first pulse (Φ1) is received on the CLOCK ADVANCE line, the autozero cycle terminates and integration of the input signal begins.

The second pulse on the CLOCK ADVANCE line (Φ2) strobes out the results of a polarity test that the module performs on the input signal during the integration. This second pulse should occur from 10 μs before the end of this signal integration period. If the input signal is negative, the MP2316A issues a pulse on the EOC/POLARITY line nominally within 1 μs of receipt of the Φ2 pulse. If the input signal is positive, the MP2316A issues no pulse on the EOC/POLARITY line at this time.

Reference Integration Phase

The third pulse is applied to the CLOCK ADVANCE (Φ3) from 4-16 μs after the Φ2 pulse, at which time the module automatically switches the integrator's input to the precision reference, and the preamplifier's input to the AUTOZERO RETURN line. Because the preamplifier is disconnected from the integrator, any gain and/or multiplexer switching needed for the next measurement may be made during this phase without affecting the accuracy of the reference integration.

Within nominally 1 μs after receiving Φ3, the MP2316A begins discharging the integration capacitor via a precision reference of opposite polarity from that of the input signal. If the magnitude of the integrated signal is within the integrator's full scale range, the capacitor will be fully discharged during this phase, causing a pulse to appear on the EOC/POLARITY line. The table in Figure 8 shows the linear relationship between (1) the integrated input signal, and (2) the elapsed time between the Φ3 and EOC pulses.

If the magnitude of the integrated signal exceeds the integrator's full scale range, EOC will not be issued. In such a case, a pulse must be issued on the RESET line after the maximum reference integration time has elapsed; this will cause the overrange condition to be cleared by the autozero circuit.

Timing Resolution and Code Conversion

The resolution of the analog-to-digital conversion may be established at any desired level continuously up to 16 binary bits or 4 full BCD digits plus sign. Linearity will be 0.001% FSR regardless of the resolution selected. Selection of resolution is accomplished by specifying the external counter's clock rate in accordance with the following relationship:

$$\text{Fclock} = \frac{B^{(n-1)}}{T} \quad \begin{array}{l}\text{(the maximum counts at}\\ \pm\text{full scale)}\end{array}$$

where n is the desired resolution (including the sign bit), B is the counting base (normally 2 or binary) and T is the maximum reference integration time. As an example, for 15-bit binary resolution with 60 Hz power line:

$$\text{Fclock} = \frac{2^{(15-1)}}{8.33\ \text{ms}} = 1.966\ \text{MHz}$$

A 2 MHz clock may be used for convenience in this case, which will slightly increase the resolution with no change in linearity. As a second example, for a full 4 digit BCD display plus sign with 50 Hz power line:

$$\text{Fclock} = \frac{10^{(5-1)}}{10.0\ \text{ms}} = 1.00\ \text{MHz}$$

Other coding, such as two's complement, can be established by simple logic at the counter's output.

Calibration

The MP2316A is inherently stable, and in most applications will not require recalibration more often than every six months. When recalibrating the system, adjust offset before adjusting range.

Offset Adjustment

RTI offset may be adjusted to zero via an external potentiometer installed between AUTOZERO RETURN and the SIGNAL RETURN (see Figure 9); RTO offset may be adjusted via a time delay between 03 and the start of the external software or hardware counter. With a 0V input signal, adjust the offset signal via the selected method(s) so that the reference integration time is within the desired tolerance (e.g., within one or two clock periods of the counter start).

Range Adjustment

Range may be adjusted via a potentiometer installed between the PGA OUTPUT pin and the INTEGRATOR INPUT pin (see section on gain programming). It is recommended that an input voltage of roughly 10% less than full scale be used during this adjustment procedure to avoid overrange conditions during adjustment. Adjust the range so that the dual-slope-derived reference integration time, as shown by an external counter, is proportional to the input voltage to within the desired tolerance.

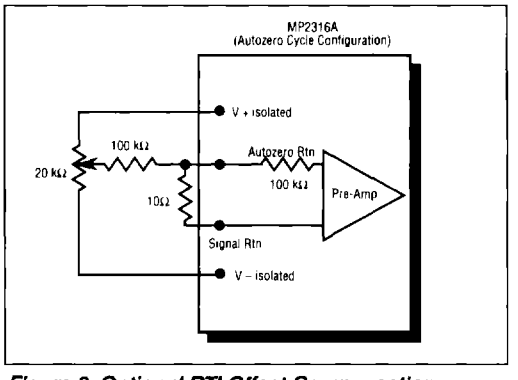

Figure 9. Optional RTI Offset Compensation.

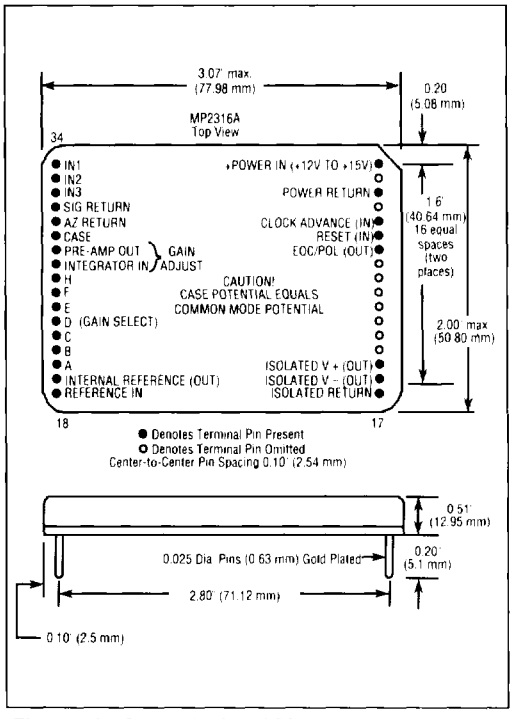

Figure 10. Mechanical and Pinout.

Ordering Guide

Specify **MP2316A**

Notice: The Analogic MP2316A is protected under one or more of the following U.S. patents and others pending:

3,051,939; 3,054,910; 3,316,547; 3,649,924; 3,750,146