

Agilent U7231A DDR3 Compliance Test Application for Infiniium 9000 and 90000 Series Oscilloscope

Datasheet



The image shows an Agilent Infiniium DSO91304A Digital Storage Oscilloscope. The main display shows a waveform with a play button in the center. The interface includes a menu bar (File, Control, Setup, Measure, Analyze, Utilities, Help) and various control knobs and buttons on the right side. Overlaid on the oscilloscope are several software windows from the DDR3 Test application:

- DDR3 Test -- DDR3 Device 1**: A window showing the test environment setup, including a task flow (Set Up, Select Tests, Configure, Connect, Run Tests, Results, Hit Report) and a 'DDR3 Test Environment Setup' section with options for Speed Grade (DDR3-1067, DDR3-1333, DDR3-1600) and Test Mode (Compliance, Advanced Debug).
- DDR3 Test -- DDR3 Device 1***: A window showing a 'Connection Diagram for DDR3 Test Measurements (Live Signal)' with a diagram of the test setup and a 'Run Tests' button.
- DDR3 Test -- DDR3 Device 1***: A window showing a list of tests with columns for Test Name, Worst Actual, Worst Margin, and Spec Range. The 'ICCK (abs) Period Rising Edge Measurements' test is highlighted.
- DDR3 Test -- DDR3 Device 1***: A window showing 'Details: ICCK (abs) Period Rising Edge Measurements' with a table of parameters and values.

Test Name	Worst Actual	Worst Margin	Spec Range
ICCK (abs) Period Rising Edge Measurements	2.44ns	-8.1%	2.67ns <=
ICCK (avg) Rising Edge Measurements	2.45ns	0.0%	2.02ns <=
ICCK Average High Measurements	497ns	42.5%	400ns <=

Parameter	Value	Reference Range
Test Limit	2.47ns to 8	ICCK Rising
Parameter Tested	2.44ns	
Actual Value	2.44ns	
Summary		
Trials: 2		
Failed: 2		
Passed: 0		
Worst Trial	2.44ns	
Trial 1		
Min	2.44ns	
Max	2.44ns	
Abs. Diff	99.50ps	
Average	2.49ns	

Test, debug and characterize your DDR3 designs quickly and easily

The Agilent Technologies U7231A DDR3 compliance test application provides a fast and easy way to test, debug and characterize your DDR3 designs. The tests performed by the U7231A software are based on the JEDEC¹ JESD79-3C DDR3 SDRAM Specification. In addition, the application features Advanced Debug mode, which covers crucial measurements such as eye-diagram, mask testing, ringing and other tests that are not covered in the specifications but are critical for characterizing DDR3 devices. The test application offers a user-friendly setup wizard and a comprehensive report that includes margin analysis.

DDR3 is an evolutionary upgrade to DDR2 and DDR1 memory systems. DDR3 technology enables even higher bandwidth for data transfer than

DDR2 and allows you to build devices with even smaller chip footprints that consume less power and generate less heat. DDR3 achieves these advances with enhanced fine ball-grid array (FBGA) packaging, enhanced on-die termination, self calibration and automatic self-refresh for improved control of signal integrity.

Signal integrity is crucial for memory system interoperability. Reference clock jitter measurements help you ensure that jitter is well within the specifications, which is the key to reliable and interoperable modular memory systems. At the same time, electrical and timing characteristics of other signals are critical as well, to ensure the memory system functions correctly and stays error free.

The U7231A DDR3 compliance test application is compatible with Agilent 9000 and 90000 Series Infiniium digital storage oscilloscopes.

¹ The JEDEC (Joint Electronic Device Engineering Council) Solid State Technology Association is a semiconductor engineering standardization body of the Electronic Industries Alliance (EIA), a trade association that represents all areas of the electronic industry.

Features

The U7231A DDR3 compliance test application offers several features to simplify the validation of your DDR3 designs:

- New setup wizard for quick setup, configuration and test
- Enhanced execution speed and proven test algorithm for clock test, which minimizes your compliance test time
- User-selected tests and configurations based on JEDEC JESD79-3C Specification data rate and user-defined speed for embedded designs
- Unique technique to provide read-write burst signal separation on the same bus in real-time mode, allowing powerful debug and analysis
- Ability to analyze the loading effect of adjacent RANK of the same memory channel
- Test framework provides powerful characterization through multiple trials that show a full array of statistics for each measurement and returns the worst measurement value
- Automatically perform derating table calculations for setup and hold time measurements based on slew rate

Comprehensive test coverage

With the DDR3 compliance test application, you can use the same oscilloscope you use for everyday debugging to perform automated testing and margin analysis based on the JEDEC electrical and timing specifications. The application automatically configures the oscilloscope for each test and provides informative results. It includes margin analysis indicating how close your device comes to passing or failing the test for each specification.

Some of the difficulties in performing DDR3 tests are connecting to the target device, configuring the oscilloscope, performing the tests and analyzing the measured results. The DDR3 compliance test application does most of this work for you. If you discover a problem with your device, the Advanced Debug feature in the test application and debug tools in the oscilloscope are available to aid in root-cause analysis.

Easy test definition

The test application enhances the usability of Agilent Infiniium oscilloscopes for testing DDR3 devices. The Agilent automated test framework guides you quickly through the steps required to define the setup, perform the tests and view the test results. On the environmental setup page, you can select the type of DDR3 devices, and the framework automatically filters the tests based on your selection. You can then select a category of tests or specify individual tests. The user interface is designed to minimize unnecessary reconnections, which saves time and minimizes potential operator error. You can save the tests and configurations as project files and recall them later for quick testing and review of previous results. Clear menus let you perform tests with minimum mouse clicks.

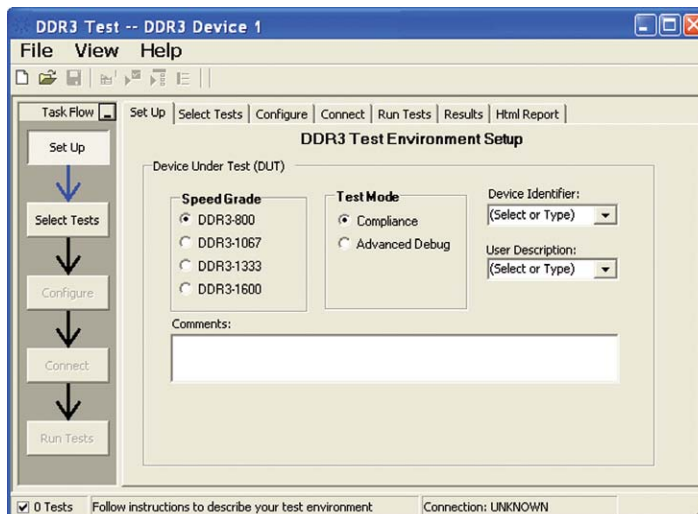


Figure 1. DDR3 application test setup screen. Select Compliance or Advanced Debug test mode and the speed grade of your device.

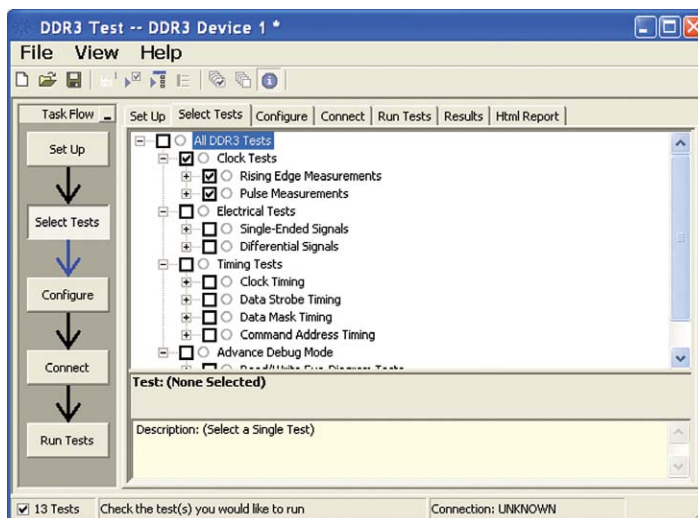


Figure 2. The Agilent automated test engine filters the test selection based on your test setup. You can easily select individual tests or groups of tests with a mouse-click.

Configurability and guided connection

The U7231A DDR3 compliance test application provides flexibility in your test setup. The application lets you define controls for critical test parameters such as voltage threshold values, number of waveforms used for analysis and customizable violation settings. Once you have configured the tests, the connection page will display the connection diagram for the test you have selected.

With the multiple test trial capability, you can extensively characterize the performance of your DDR3 devices. You can run the selected tests until the stop condition is met. The application will then save the worst-case conditions and help you track down the anomalies in your signals.

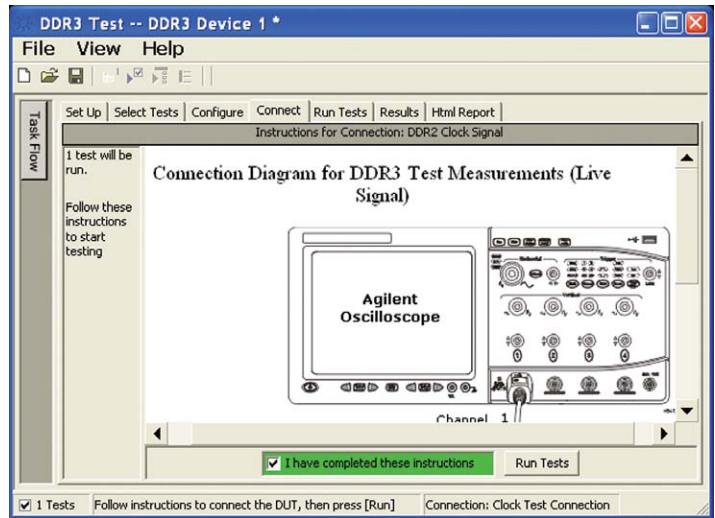


Figure 3. The software prompts you with the connection diagrams for the tests you have selected.

Comprehensive results analysis

In addition to providing you with measurement results, the U7231A DDR3 compliance test application reports how close you are to the specified limit. You can specify the level at which warnings are to be issued. You are provided with a full array of statistics for each measurement, and you can save worst-case conditions to extensively test the performance of your device.

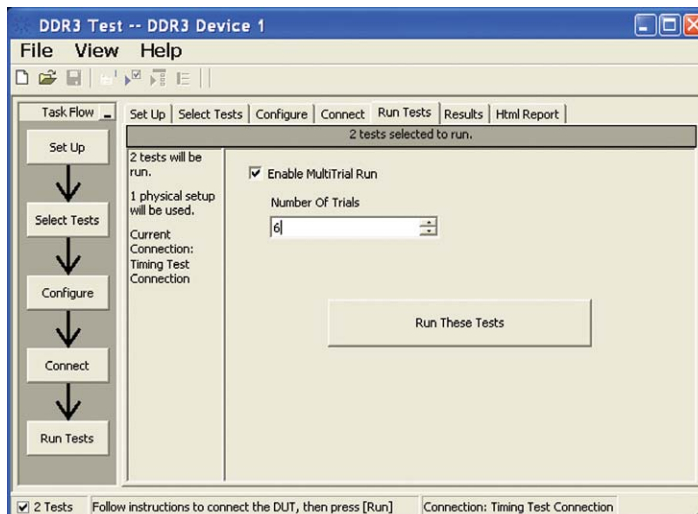


Figure 4. The Repetitive Run feature allows you to run the selected tests until the stop condition is met. It allows you to extensively test the performance of your device.

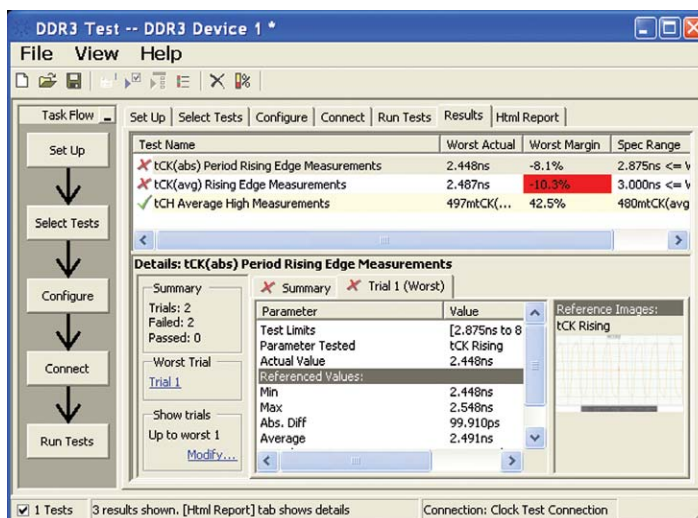


Figure 5. The DDR3 test application documents your test parameters, pass or fail status, test specification range, measured values and the pass/fail margin.

Thorough performance reporting

The U7231A DDR3 compliance test application generates thorough HTML reports that capture the performance, status and margins of your device. It also captures screen shots of critical measurements for your reference and documentation. This report is suitable for printing and sharing with your vendors, customers or colleagues.

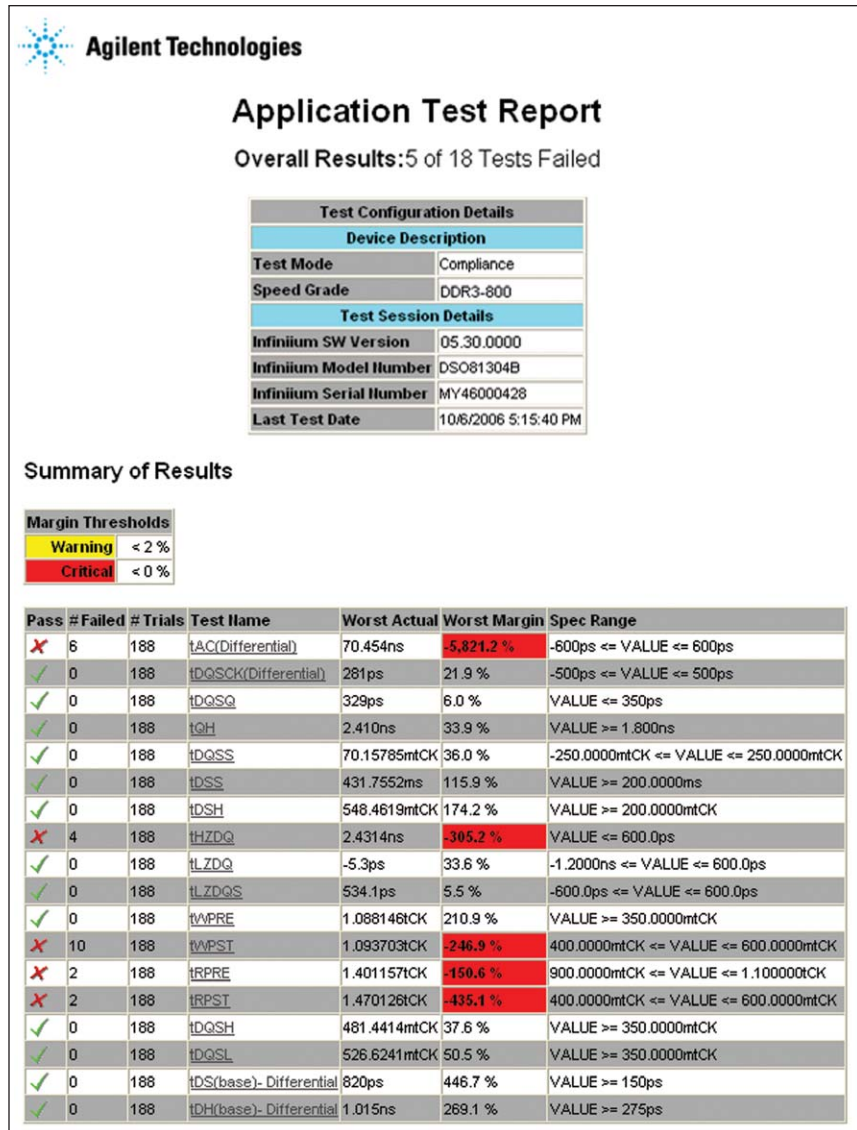


Figure 6. The DDR3 test application generates a summary report where you can see your device's test results quickly and clearly. Details are available for each test including the test limits, test description and test results, including saved waveforms. In addition, the pass/fail margin is indicated to give you further insight.

System device requirements

In order to speed your test time, you must use the appropriate RAM test reliability software with the memory system to generate random activity on the memory bus. Memtest, is commonly used RAM reliability test software that can run on DOS, Windows® and Linux systems.

Test performed

The Agilent U7231A DDR3 compliance test application covers clock, electrical and timing parameters of the JEDEC JESD79-3C DDR3 SDRAM Specifications. The application helps you test all DDR3 devices for compliance, using an Agilent 9000 or 90000 Series Infiniium oscilloscope.

In addition, the test application's Advanced Debug feature provides popular test methodologies that are not covered in any specification. These tests help users who want to perform extensive validation beyond the test specification. It also sets up the scope to isolate the read and write signals so you can immediately jump in to debug the signals.

Table 1. JEDEC tests covered by the U7231A test application

Specification	Speed supported			
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
<i>AC and DC input measurement levels</i>				
Table 24 – Single-ended AC and DC input levels (page 115)	x	x	x	x
Table 25 – Differential AC and DC input levels (page 118)	x	x	x	x
Table 27 – Single-ended levels for CK, DQS (page 119)	x	x	x	x
Table 28 – Cross point voltage for differential input signals (CK, DQS) (page 120)	x	x	x	x
Table 31 – Single-ended AC and DC output levels (page 123)	x	x	x	x
Table 32 – Differential AC and DC output levels (page 123)	x	x	x	x
Table 34 – Output slew rate (single-ended) (page 124)	x	x	x	x
Table 36 – Differential output slew rate (page 125)	x	x	x	x
Table 37 – AC overshoot/undershoot specifications for address and control pins (page 127)	x	x	x	x
Table 38 – AC overshoot/undershoot specifications for clock, data, strobe and mask (page 128)	x	x	x	x
<i>Electrical characteristics and AC timing</i>				
Table 67 – Timing parameters by speed bin (page 164)	x	x	x	x

Table 2. Advanced Debug feature covered by the U7231A test application

Measurement items	Speed supported
All JEDEC tests from compliance mode	User configurable
Read/write eye-diagram test	User configurable
High/low state ringing test	User configurable

Oscilloscope compatibility

The U7231A DDR3 compliance test application is compatible with Agilent 9000 or 90000 Series oscilloscopes with operation software revision 2.0 or higher and 54850/80000 Series oscilloscopes with operation software revision 5.70 or higher (Windows XP Pro). For oscilloscopes with earlier software revisions, free upgrade software is available at <http://www.agilent.com/find/scope-apps-sw>.

DDR3 data rate	Recommended oscilloscope	Bandwidth	Sampling rate
Up to 1600 MT/s	9254A	2.5 GHz	10 GSa/s
	9404A	4 GHz	10 GSa/s
	90404A	4 GHz	20 GSa/s
	90604A	6 GHz	29 GSa/s
	90804A	8 GHz	40 GSa/s
	91204A	12 GHz	40 GSa/s
	91304A	13 GHz	40 GSa/s

Note:

1. Recommended 8 GHz bandwidth or greater for full characterization.
2. Option 005 noise reduction is recommended for 8-GHz or higher bandwidth oscilloscopes.
3. The JEDEC JESD79-3C specification does not specify the rise time and fall time for DDR3 signals. The required oscilloscope bandwidth is also not mentioned. It is advisable for you to determine the oscilloscope bandwidth requirement based on the fastest rise time and fall time of the DDR3 signals. Please refer to Table 3.

For 9000 and 90000 Series oscilloscope, you can choose the oscilloscope bandwidth using the calculation below.

Maximum signal frequency content = $0.4/\text{fastest rise or fall time (20 - 80\%)}$

Scope bandwidth required = 1.4x maximum signal frequency for 3% accuracy measurement

Scope bandwidth required = 1.2x maximum signal frequency for 5% accuracy measurement

Scope bandwidth required = 1.0x maximum signal frequency for 10% accuracy measurement

Table 3. Infiniium 9000 and 90000A Series oscilloscope rise/fall time specifications

Rise time/ fall time	90254A	90404A	90604A	90804A	91204A	91304A
10 – 90%	140 ps	105 ps	70 ps	54 ps	35 ps	32 ps
20 – 80%	105 ps	79 ps	53 ps	38 ps	26 ps	24 ps

Ordering information

To purchase the U7231A DDR3 compliance test application for your new and existing Infiniium 9000 or 90000 Series oscilloscope, order the following:

Oscilloscope requirements

Model number	Description
9000/90000 or 54850A/80000	Infiniium Series scope with software 2.0 or higher
U7231A or N5459A	DDR3 compliance test application (Option 033 on new 9000/90000 Series oscilloscope DDR 1, 2 and 3 Software Bundle Option (contain options U7233A, N5413A, U7231A)
E2688A	High-speed serial data analysis and clock recovery software (Option 003 on new 9000 or 90000 Series oscilloscopes or Option N5435A-003 for application server license)
N5414A	InfiniiScan event identification software (Option 009 on new 9000 or 90000 Series oscilloscopes or Option N5435A-004 for application server license)
116xA/113xA ^{1,2}	InfiniiMax I/II probe amplifier (minimum quantity 3 required)

1 Ensure that the probe amplifier meets the bandwidth requirement for your signal measurements. Refer to the "Probe accessories" section below to configure the probe head to go with your probe amplifier.

2 For multiple RANK testing, a quantity of 4 probes are required for additional probing of Chip Select (CS) pin.

Probe accessories

InfiniiMax probe amplifiers

Model number	Description
1169A	12-GHz differential probe amplifier
1168A	10-GHz differential probe amplifier
1134A	7-GHz differential probe amplifier
1132A	5-GHz differential probe amplifier

InfiniiMax probe heads

Model number	Description
N5381A	InfiniiMax II 12-GHz differential solder-in probe head and accessories
N5382A	InfiniiMax II 12-GHz differential browser
E2677A	InfiniiMax 12-GHz differential solder-in probe head and accessories
E2675A	InfiniiMax 6-GHz differential browser probe head and accessories
N5425A	InfiniiMax 12-GHz ZIF probe head
N5426A	ZIF tips (x10)
N5451A	Long Wire tips (x10)

DDR3 BGA Probe Adapters

Model Number	Description
W2635A-010	x4 and x8, 10mm width DDR3 BGA probe adapter for oscilloscopes
W2635A-011	x4 and x8, 11mm width DDR3 BGA probe adapter for oscilloscopes
W2636A-010	x16, 10mm width DDR3 BGA probe adapter for oscilloscopes
W2636A-011	x16, 11mm width DDR3 BGA probe adapter for oscilloscopes
W2631A	x16 DDR3 BGA probe for oscilloscopes and logic analyzers
W3633A	x4, x8 DDR3 BGA probe for oscilloscopes and logic analyzers
W2639A	Scope adapter board for DDR3 BGA probe

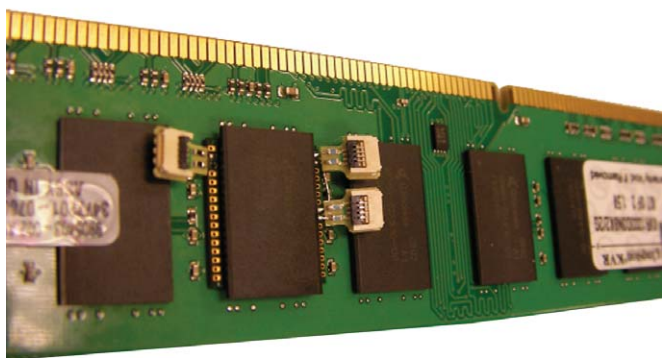


Figure 8. Probing of DDR3 signals with DDR3 BGA probe adapter and ZIF tips

Related literature

Publication title	Publication type	Publication number
<i>Agilent Infiniium DSO/DSA 90000A Series Oscilloscopes and InfiniiMax Probes</i>	Data Sheet	5989-7819EN
<i>Infiniium DSO80000B Series Oscilloscopes and InfiniiMax Series Probes</i>	Data Sheet	5989-4606EN
<i>Agilent InfiniiScan Event Identification Software for Infiniium 80000 and 8000 Series Oscilloscopes (N5414A and 5415A)</i>	Data Sheet	5989-4605EN
<i>Agilent Technologies E2688A, N5384A High-Speed Serial Data Analysis and Clock Recovery Software for Infiniium 54830, 54850 and 80000 Series Oscilloscopes</i>	Data Sheet	5989-0108EN
<i>Agilent Technologies EZJIT and EZJIT Plus Jitter Analysis Software for Infiniium Series Oscilloscopes</i>	Data Sheet	5989-0109EN
<i>W2635A and W2636A DDR3 BGA Probe Adapter for Infiniium Oscilloscopes</i>	Data Sheet	5989-0109EN
<i>A Time-Saving Method for Analyzing Signal Integrity in DDR Memory Buses</i>	Application Note	5989-6664EN
<i>W3630A Series DDR3 BGA Probes for Logic Analyzers and Oscilloscopes</i>	Data Sheet	5990-3179EN

Product Web site

For the most up-to-date and complete application and product information, please visit our product Web site at: www.agilent.com/find/u7231a

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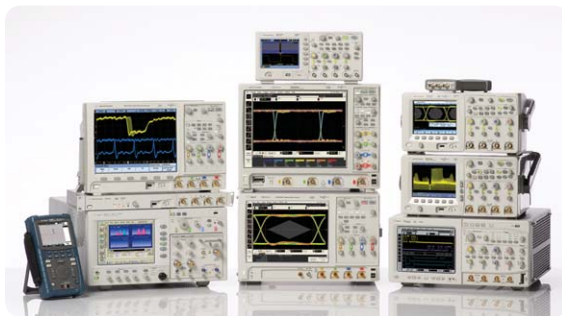
Agilent Open

www.agilent.com/find/open
Agilent Open simplifies the process of connecting and programming test systems to help engineers design, validate and manufacture electronic products. Agilent offers open connectivity for a broad range of system-ready instruments, open industry software, PC-standard I/O and global support, which are combined to more easily integrate test system development.

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www.lxistandard.org
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