AT&T Microelectronics

41MGL3
Quad Differential Line Driver

Features

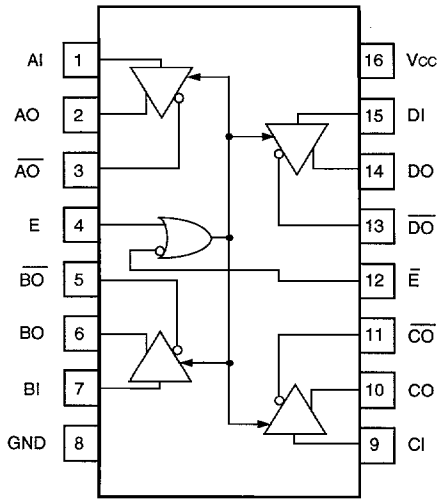
- True 3-state output
- Pin equivalent to the general-trade 26LS31 device with improved speed, reduced power consumption, and significantly lower levels of EMI
- Four line drivers per package
- Meets ESDI standards
- 2.5 ns maximum propagation delay
- Single 5.0 V supply
- Operating temperature range: 0 °C to 85 °C (See Section 9.)
- 200 Mbits/s or 400 Mbits/s maximum data rates when used with the 41L*x* and 41M*x* receivers respectively
- Logic to convert TTL input logic levels to differential, pseudo-ECL output logic levels
- High output driver for 50 Ω loads
- 250 mA short-circuit current (typical)
- <0.2 ns output skew (typical)

Description

The 41MGL3 Quad Differential Line Driver integrated circuits are quad TTL-input-to-pseudo-ECL-differential-output line drivers for digital data transmission over balanced transmission lines. The 41MGL3 is a low-power version of the 41MGA, reducing power consumption by two thirds. The 41MGL3 device also features a true 3-state output. The 41MGL3 requires the customer to supply external termination resistors on the circuit board. This device is pin equivalent to the general-trade 26LS31, but offers increased speed, decreased power consumption, and significantly lower levels of electromagnetic interference (EMI).

The packaging options that are available for the quad differential line drivers include a 16-pin DIP (41MGL3), a 16-pin J-lead SOJ (1041MGL3), a 16-pin gull-wing SOIC (1141MGL3), and a 16-pin narrow-body gull-wing SOIC (1241MGL3).

Pin Information



41MGL3
1041MGL3
1141MGL3
1241MGL3

12-2038C

Note: The device is disabled when E = 0 and $\overline{E}$ = 1.

Figure 3-5. 41MGL3 Logic Diagram

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	—	7.0	V
Ambient Operating Temperature	T_A	0	85	°C
Storage Temperature	T_{stg}	–40	125	°C

Handling Precautions

CAUTION: This device is susceptible to damage as a result of electrostatic discharge. Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

AT&T employs a human-body model (HBM) for ESD-susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. The standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is used. The HBM ESD threshold voltage presented here was obtained using this circuit.

Device	Rating
41MGL3 Driver	>2000 V

Electrical Characteristics

Table 3-13. 41MGL3 Power Supply Current Characteristics

T_A = 0 °C to 85 °C, V_{CC} = 5 V ± 0.5 V.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current:					
41MGL3*:					
All Outputs Disabled	I_{CC}	—	35	50	mA
All Outputs Enabled	I_{CC}	—	10	16	mA

* Measured with no load.

Table 3-14. 41MGL3 Voltage and Current Characteristics

T_A = 0 °C to 85 °C.

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltages, V_{CC} = 4.5 V:					
Low, I_{OL} = –8.0 mA*	V_{OL}	—	2.5	V_{OH} – 0.8†	V
High, I_{OH} = –40.0 mA*	V_{OH}	2.5	3.5	—	V
High Z, I_{OH} = –1.0 mA, V_{CC} = 4.5 V	V_{OZ}	—	0.2	0.5	V
Input Voltages:					
Low, V_{CC} = 5.5 V	V_{IL}‡	—	—	0.8	V
High, V_{CC} = 4.5 V	V_{IH}‡	2.0	—	—	V
Clamp, V_{CC} = 4.5 V, I_{IN} = –50 mA	V_{IK}	—	—	–1.5	V
Short-circuit Output Current, V_{CC} = 5.5 V	I_{OS}§	–100	–250	–350	mA
Input Currents, V_{CC} = 5.5 V					
Low, V_{IN} = 0.4 V	I_{IL}	—	—	–400	µA
High, V_{IN} = 2.7 V	I_{IH}	—	—	20	µA
Reverse, V_{IN} = 5.5 V	I_{IH}	—	—	100	µA

* Typical value of the output current for the 41MGL3 when terminated per Figure 6-5.
† V_{OL} must be a minimum of 0.8 V less than its complementary output.
‡ The input levels and difference voltage provide zero noise immunity and should be tested only in a static, noise-free environment.
§ Test must be performed one lead at a time to prevent damage to the device.

Timing Characteristics

Table 3-15. 41MGL3 Timing Characteristics (See Figures 6-1 and 6-2.)

Propagation-delay test circuit connected to output (see Figure 6-6).

T_A = 25 °C, V_{CC} = 5 V ± 0.5 V.

Symbol	Parameter	Typ	Max	Unit
	Propagation Delay:			
t_{P1}	Input High to Output	1.5	2.5	ns
t_{P2}	Input Low to Output	1.5	2.5	ns
	Disable Time:			
t_{PHZ}	High to High Impedance	10	20	ns
t_{PLZ}	Low to Low Impedance	10	20	ns
	Enable Time:			
t_{PZH}	High Impedance to High	12	20	ns
t_{PZL}	High Impedance to Low	12	20	ns
t_{skew}	Output Skew, $\|t_{P1} - t_{P2}\|$	0.1	0.3	ns
Δt_{skew}	Difference Between Drivers	0.3	0.6	ns
t_{tLH}	Rise Time	—	2.0	ns
t_{tHL}	Fall Time	—	2.0	ns