FUJITSU SEMICONDUCTOR
DATA SHEET

DS601-00001-2v0-E

Semicustom

CMOS

Standard Cell

CS401 Series

■ DESCRIPTION

The CS401 series of 28 nm standard cells is a line of CMOS ASICs that satisfy demands for lower power consumption, higher speed and higher integration.

These cells offer the minimum level of leakage current in the semiconductor industry, and are able to implement a mixture of core transistors with four different threshold voltages, as appropriate for the applications ranging from handheld terminals to digital audiovisual equipment.

The integration level in this series is twice the CS302 series with lower power consumption and higher speed.

■ FEATURES

- Technology : 28 nm Metal-gate CMOS
  : Maximum 11-metal layers. Ultra low permittivity material is used for dielectric inter-layers.
  : Four different types of core transistors (low leak, standard, high speed and ultra high speed) can be used on the same chip.
- Supply voltage : Internal power supply : + 1.0 V ± 0.1 V
  : External power supply : + 1.8 V ± 0.15 V
  (1.8V interface on dual-power supply system)
  + 2.5 V ± 0.2 V
  (2.5V interface on dual-power supply system)
  + 3.3 V ± 0.3 V
  (3.3V interface on dual-power supply system)
- Junction temperature range: − 40 °C to + 125 °C (standard specification)
- Gate power consumption: 0.61 nW / gate (operating condition: 1.0 V, operating rate 0.5, 1 MHz)
- Support high-quality, various types of cell sets developed by FUJITSU SEMICONDUCTOR (from low power versions to high speed versions).
- Support SRAMs with standby-mode and power-down mode for lower power consumption memories.
- Compiled cells (RAM, ROM, others)
- Support special interfaces (LVDS, SSTL, others).
- Support boundary SCAN test.
- Support use of industry standard libraries.
- Support use of industry standard tools.
- Short-term development using a physical prototyping tool
- One pass design using a physical synthesis tool
- Hierarchical design environment for supporting large-scale circuits
- Support Signal Integrity, EMI noise reduction.

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- Support static timing sign-off.
- Improve timing convergence by using Statistical Static Timing Analysis (SSTA).
- Design For Manufacturing (DFM) enables stable product-supply and reduced variation.
- Package lineup: FBGA, PBGA, TEBGA, FC-BGA

Note: Including items under development.

■ MACRO LIBRARIES (INCLUDING MACROS CURRENTLY BEING PREPARED)

1. Logic cells (about 400 types)

Library sets having four different threshold voltages of core transistors.

- Adder
- AND
- AND-OR
- AND-OR Inverter
- Buffer
- Clock-Buffer
- Delay Buffer
- ENOR
- EOR
- Inverter
- Latch
- NAND
- NOR
- OR
- OR-AND
- OR-AND Inverter
- SCAN Flip flop
- Non-SCAN Flip flop
- Selector
- Others

2. IP macros

CPU/DSP	ARM™* cores (ARM7TDMI-S™*, ARM946E-S™*, ARM926EJ-S™*, ARM1176JZF-S™*, Cortex-M3™*, Cortex-R4F™*, Cortex-A9™* MPCore), Peripherals IP
Mixed signal macro	ADC, DAC, OPAMP, others
Compiled macro	SRAM (1 Port, 2 Port), ROM, product sum calculator, others
PLL	Analog PLL

*: ARM, ARM7TDMI-S, ARM946E-S, ARM926EJ-S, ARM1176JZF-S, Cortex-M3, Coretex-R4F and Cortex-A9 are the trademarks of ARM Limited in the EU and other countries.

3. Special I/O interface macro

Special I/O	LVDS, SSTL18, PCI, I^2C
Interface macro	USB2.0 Device/host, Serial-ATA, PCI-Express, DDR2, HDMI, others

■ COMPILED CELL

Compiled cells are macro cells that can be automatically generated by specifying the bit/word configuration. The following compiled cells are available for the CS401 series.

- Memory capacity

Name	Category	Memory capacity (bit)
Clock synchronous single-port RAM (1RW)	High-Density	64 to 1152 K
	High-Speed	32 to 80 K
	Large-Scale	16 K to 9 M
Clock synchronous dual port RAM (2RW)	High-Density	32 to 144 K
Clock synchronous ROM	—	128 to 1152 K
Clock synchronous register file (1RW)	—	80 to 36 K
Clock synchronous register file (1R1W)	—	32 to 72 K
Clock synchronous register file (2R2W)	—	16 to 18 K

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{DD}	− 0.4	+ 1.4	V	*2
		− 0.5	+ 2.5		*3
		− 0.5	+ 3.6		*4
		− 0.5	+ 4.6		*5
Input voltage*1	VI	− 0.5	V_{DD} + 0.5 (≤ 2.5 V)	V	*3
		− 0.5	V_{DD} + 0.5 (≤ 3.6 V)		*4
		− 0.5	V_{DD} + 0.5 (≤ 4.6 V)		*5
Output voltage*1	VO	− 0.5	V_{DD} + 0.5 (≤ 2.5 V)	V	*3
		− 0.5	V_{DD} + 0.5 (≤ 3.6 V)		*4
		− 0.5	V_{DD} + 0.5 (≤ 4.6 V)		*5
Storage temperature	T_{STG}	− 55	+ 125	°C	
Operation junction temperature	Tj	− 40	+ 125	°C	
Output current*6	IO	—	—	mA	
Power supply pin current*7	ID	—	—	mA	

*1: V_{SS} = 0 V

*2: Internal gates

*3: 1.8 V interface on dual-power supply system

*4: 2.5 V interface on dual-power supply system

*5: 3.3 V interface on dual-power supply system

*6: The output current varies depending on the number of wiring layers in the chip and the wiring configuration of the I/O cells. Contact the sales representative for details.

*7: For details about the power supply pin current, contact the sales representative.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

MEMO

MEMO

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