FAIRCHILD SEMICONDUCTOR®

August 2009

FAN7318B
LCD Backlight Inverter Drive IC

Features

- High-Efficiency Single-Stage Power Conversion
- Wide Input Voltage Range: 6V to 30V
- Backlight Lamp Ballast and Soft Dimming
- Minimal External Components Required
- Precision Voltage Reference Trimmed to 2%
- Half-Bridge Topology
- Soft-Start
- PWM Control at Fixed Frequency
- Analog Dimming Function
- Burst Dimming Function
- Programmable Striking Frequency
- Open-Lamp Protection
- Open-Lamp Regulation
- Over-Voltage Protection
- Short-Lamp Protection
- CMP-High Protection
- Thermal Shutdown
- 20-Pin SOIC

Applications

- LCD TV
- LCD Monitor

Description

The FAN7318B is a LCD backlight inverter drive IC that controls P-N half-bridge topology.

The FAN7318B provides a low-cost solution and reduces external components by integrating proprietary wave rectifiers for open-lamp protection and regulation. The operating voltage range of the FAN7318B is wide, so an external regulator isn't necessary to supply the voltage to the IC.

The FAN7318B provides various protections, such as open-lamp regulation, over-voltage protection, open-lamp protection, short-Lamp protection, CMP-high protection, to increase the system reliability. The FAN7318B provides burst dimming and analog dimming.

The FAN7318B is available in a 20-SOIC package.

20-SOIC

Ordering Information

Part Number	Operating Temperature	Package	Eco Status	Packing Method
FAN7318BM	-25 to +85°C	20-Lead, Small Outline Integrated Circuit (SOIC)	RoHS	Rail
FAN7318BMX				Tape & Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Protected under U.S. patent no. 5,652,479.

Block Diagram

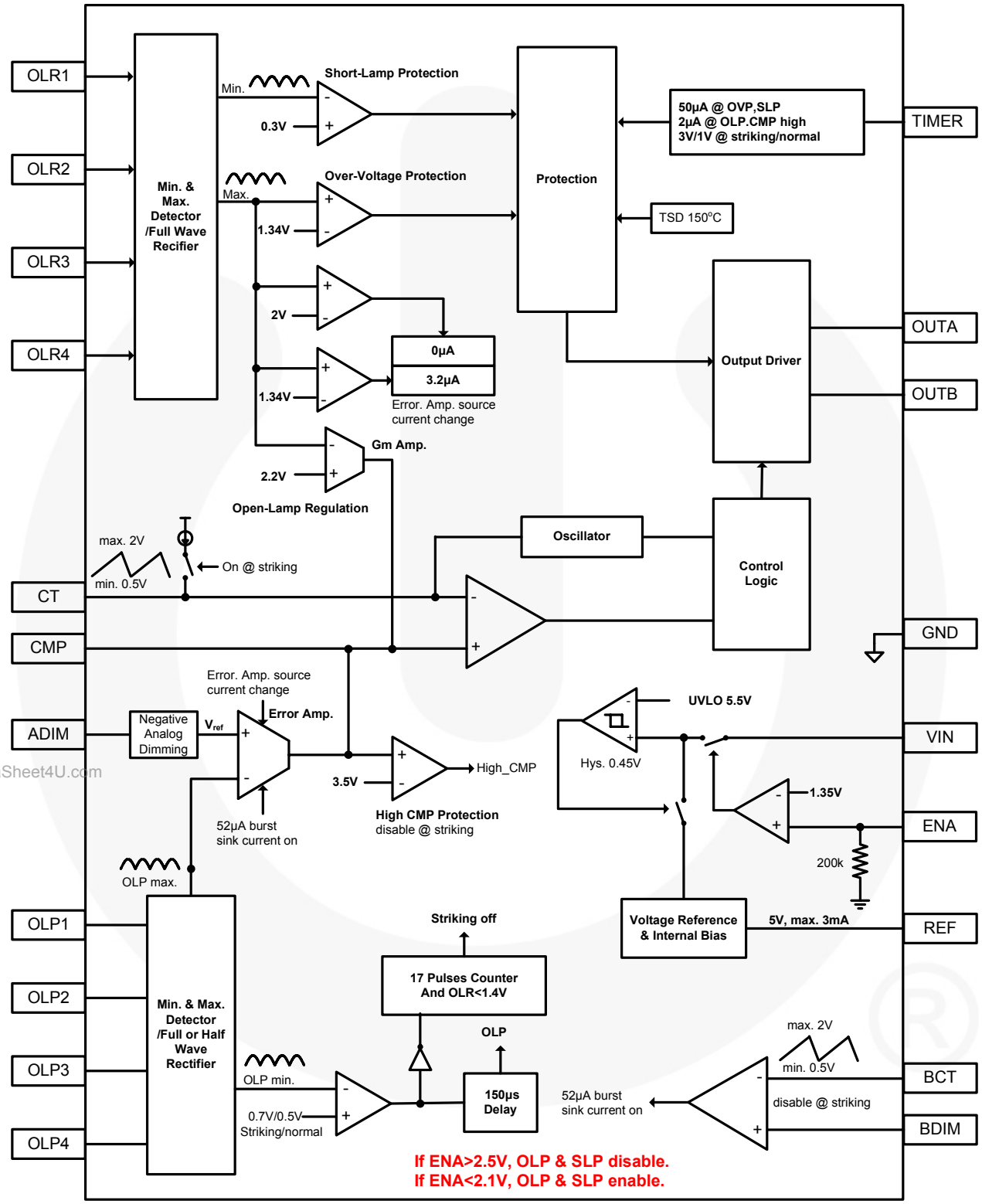

Figure 1. Internal Block Diagram

Pin Configuration

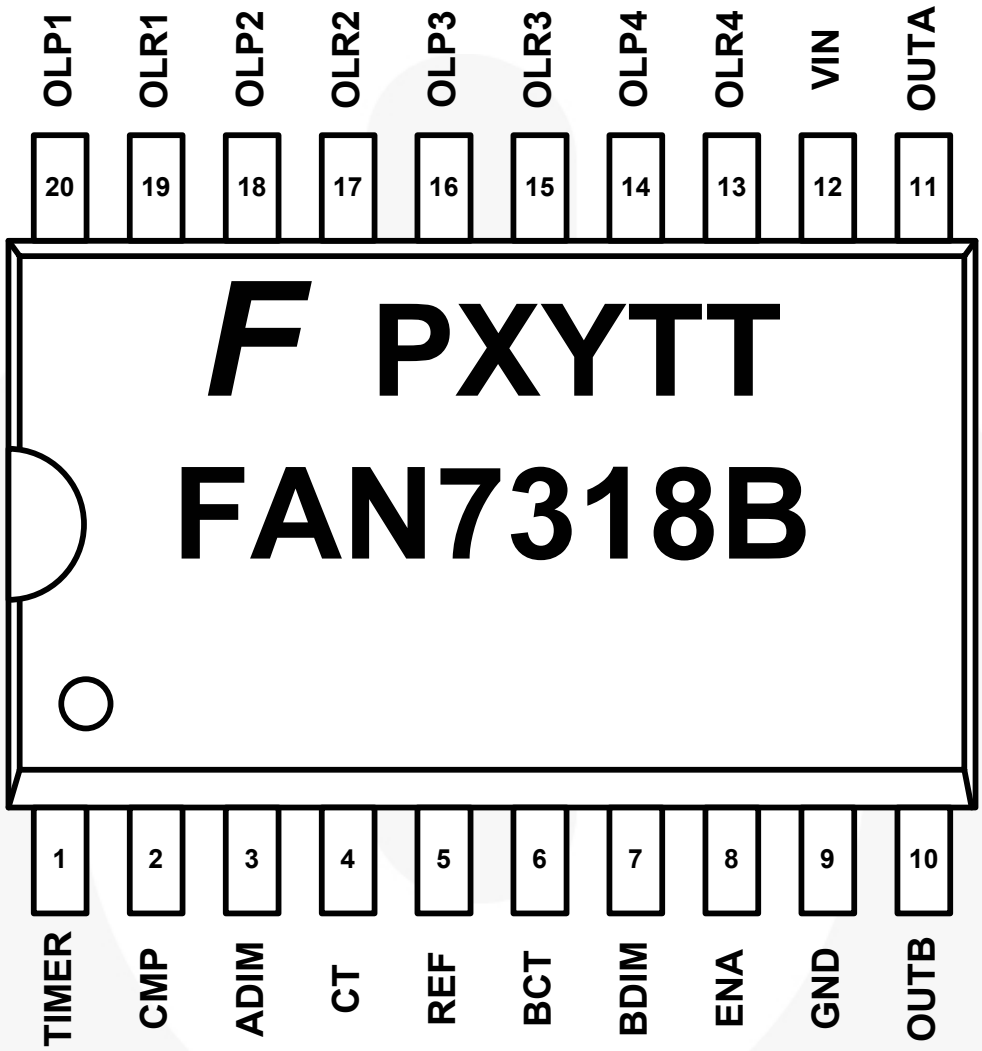

Figure 2. Package Diagram

Pin Definitions

Pin #	Name	Description
1	TIMER	This pin is for protection delay time setting.
2	CMP	Error amplifier output. Typically, a compensation capacitor is connected to this pin from the ground.
3	ADIM	This pin is the input for negative analog dimming.
4	CT	This pin is for programming the switching frequency. Typically, a capacitor is connected to this pin from ground and a resistor is connected to this pin from the REF pin.
5	REF	This pin is 5V reference output. Typically, resistors are connected to this pin from the CT pin and the BCT pin.
6	BCT	This pin is for programming the frequency of the burst dimming. Typically, a capacitor is connected to this pin from ground and a resistor is connected to this pin from the REF pin.
7	BDIM	This pin is the input for negative burst dimming. The voltage range of 0.5 to 2V at this pin controls the burst-mode duty cycle from 0% to 100%.
8	ENA	This pin turns the IC on / off.
9	GND	This pin is the ground.
10	OUTB	This pin is NMOS gate-drive output.
11	OUTA	This pin is PMOS gate-drive output.
12	VIN	This pin is the supply voltage of the IC.
13	OLR4	This pin is for open-lamp regulation. Its functions are the same as the OLR1 pin.
14	OLP4	This pin is for open-lamp protection and feedback control of lamp currents. Its functions are the same as the OLP1 pin.
15	OLR3	This pin is for open-lamp regulation. Its functions are the same as the OLR1 pin.
16	OLP3	This pin is for open-lamp protection and feedback control of lamp currents. Its functions are the same as the OLP1 pin.
17	OLR2	This pin is for open-lamp regulation. Its functions are the same as the OLR1 pin.
18	OLP2	This pin is for open-lamp protection and feedback control of lamp currents. Its functions are the same as the OLP1 pin.
19	OLR1	This pin is for open-lamp regulation and short-lamp protection. It has the same functions as other OLR pins and is connected to the full-wave rectifier internally. When the maximum of rectified OLR inputs is between 1.34V and 2V, the error amplifier output current is limited to 3.0μA. When the maximum of rectified OLR inputs reaches 2V, the error amplifier output current is 0A and its output voltage maintains constant. The maximum of rectified OLR inputs is inputted to the negative of another error amplifier for feedback control of lamp voltage. When the maximum of rectified OLR inputs is more than 2.2V, another error amplifier for OLR is operating and lamp voltage is regulated. In normal mode, if the maximum of rectified OLR inputs is higher than 1.34V or if the minimum of rectified OLR inputs is lower than 0.3V for a predetermined time by the TIMER pin capacitor and an internal current source 50μA; the IC shuts down to protect the system in over-voltage condition or short-lamp condition, respectively.
20	OLP1	This pin is for open-lamp protection and feedback control of lamp currents. It has the same functions as other OLP pins and is connected to the half-wave rectifier and the full-wave rectifier internally. In striking mode, if the minimum of rectified OLP inputs is less than 0.7V for a time predetermined by the TIMER pin capacitor and an internal current source or; in normal mode, if the minimum of rectified OLP inputs is less than 0.5V for another predetermined time by the TIMER pin capacitor and another internal current source; the IC shuts down to protect the system in open-lamp condition. The maximum of rectified OLP inputs is inputted to the negative of the error amplifier for feedback control of lamp current.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	IC Supply Voltage	6	30	V
T_A	Operating Temperature Range	-25	+85	°C
T_J	Operating Junction Temperature		+150	°C
T_{STG}	Storage Temperature Range	-65	+150	°C
θ_{JA}	Thermal Resistance Junction-Air[1,2]		90	°C/W
P_D	Power Dissipation		1.4	W

Notes:
1. Thermal resistance test board; size: 76.2mm x 114.3mm x 1.6mm (1S0P); JEDEC standard: JESD51-2, JESD51-3.
2. Assume no ambient airflow.

Pin Breakdown Voltage

Pin #	Name	Value	Unit
1	TIMER	7	V
2	CMP	7	
3	ADIM	7	
4	CT	7	
5	REF	7	
6	BCT	7	
7	BDIM	7	
8	ENA	7	
9	GND		
10	OUTB	30	
11	OUTA	30	
12	VIN	30	
13	OLR4	±7	
14	OLP4	±7	
15	OLR3	±7	
16	OLP3	±7	
17	OLR2	±7	
18	OLP2	±7	
19	OLR1	±7	
20	OLP1	±7	

Electrical Characteristics

For typical values, T_A=25°C, V_{IN}=15V, and -25°C ≤ T_A ≤ 85°C, unless otherwise specified. Specifications to -25°C ~ 85°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Under-Voltage Lockout Section (UVLO)						
V_{th}	Start Threshold Voltage	Increase V_{IN}	4.9	5.2	5.5	V
V_{thhys}	Start Threshold Voltage Hysteresis	Decrease V_{IN}	0.20	0.45	0.60	V
I_{st}	Startup Current	V_{IN}=4.5V	10	70	100	µA
I_{op}	Operating Supply Current	V_{IN}=15V, Not Switching	0.5	2.0	3.5	mA
ON/OFF Section						
V_{on}	On-State Input Voltage		1.4		5.0	V
V_{off}	Off-State Input Voltage				0.7	V
I_{sb}	Standby Current	ENA=0V	50	120	190	µA
R_{ENA}	Pull-Down Resistor	ENA=2V	120	200	280	kΩ
Reference Section (Recommend 1µF X7R Capacitor)						
V_5	5V Regulation Voltage		4.9	5.0	5.1	V
V_{5line}	5V Line Regulation	6 ≤ V_{IN} ≤ 30V		4	50	mV
V_{5load}	5V Load Regulation	10µA ≤ I_5 ≤ 3mA		4	50	mV
Oscillator Section (Main)						
f_{osc}	Oscillation Frequency	T_A=25°C, CT=220pF, RT=100kΩ	101.3	105.0	108.3	kHz
		CT=220pF, RT=100kΩ	101	105	109	
f_{str}	Oscillator Frequency in Striking Mode	T_A=25°C, CT=220pF, RT=100kΩ	126.5	131.0	135.5	kHz
		CT=20pF, RT=100kΩ	126	131	136	
I_{ctdcs}	CT Discharge Current	Striking	1.03	1.18	1.33	mA
I_{ctdc}		Normal	770	870	970	µA
I_{ctcs}	CT Charge Current	Striking	-15	-12	-9	µA
V_{cth}	CT High Voltage			2		V
V_{ctl}	CT Low Voltage			0.45		V
Oscillator Section (Burst)						
f_{oscb}	Burst Oscillation Frequency	T_A=25°C, BCT=4.7nF, BRT=1.4MΩ	321	330	342	Hz
		BCT=4.7nF, BRT=1.4MΩ	317	330	343	
I_{bctdc}	BCT Discharge current		20	26	32	µA
V_{bcth}	BCT High Voltage			2		V
V_{bctl}	BCT Low Voltage			0.5		V

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Electrical Characteristics (Continued)

For typical values, T_A=25°C, V_{IN}=15V, and -25°C ≤ T_A ≤ 85°C, unless otherwise specified. Specifications to -25°C ~ 85°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Analog Dimming Section						
AV_{rexx}	Reference Voltage	ADIM=0V, T_A=25°C	1.225	1.310	1.402	V
		ADIM=0V	1.212	1.310	1.408	
		ADIM=0.5V		1.16		
		ADIM=1.0V		0.99		
Error Amplifier Section						
I_{sin}	Output Sink Current	OLP=2.5V, ADIM=2.5V	63	76	94	µA
I_{sur1}	Output Source Current 1	OLP=0V, ADIM=0V	-65	-50	-35	µA
I_{sur2}	Output Source Current 2	CMP=3V	-1.4	-1.0	-0.6	µA
I_{bsin}	Burst CMP Sink Current	BDIM=5V, BCT=0V	41	52	63	µA
I_{olpi}	OLP Input Current	OLP=2V		0		µA
I_{olpo}	OLP Output Current	OLP=-2V	-30	-20	-10	µA
V_{lpfx}	Rectifiers Output of OLP	OLP=0.3V		0.34		V
		OLP=1.5V		1.55		V
V_{olpr}	OLP Input Voltage Range(3)		-4		4	V
Open-Lamp Regulation Section						
I_{olr1}	Error Amplifier Source Current for Open-Lamp Regulation	Striking, OLR=1.6V	-3.4	-2.8	-2.3	µA
I_{olr2}		OLR Sweep		0		µA
V_{olr1}	Open-Lamp Regulation Voltage 1	OLR Sweep	1.24	1.34	1.44	V
V_{olr2}	Open-Lamp Regulation Voltage 2	Striking, OLR Sweep	1.88	1.98	2.08	V
V_{olr3}	Open-Lamp Regulation Voltage 3		2.1	2.2	2.3	V
G_{mOLR}	OLR Error Amplifier Trans-conductance		180	310	440	µmho
I_{ors}	OLR Error Amplifier Sink Current	Normal, OLR=2.5V	40	60	80	µA
I_{olri}	OLR Input Current	OLR=2.5V		0		µA
I_{olro}	OLR Output Current	OLR=-2.5V	-35	-25	-15	µA
V_{olrr}	OLR Input Voltage Range(3)		-4		4	V

Continued on the following page…

Electrical Characteristics (Continued)

For typical values, T_A=25°C, V_{IN}=15V, and -25°C ≤ T_A ≤ 85°C, unless otherwise specified. Specifications to -25°C ~ 85°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Protection Section						
V_{olp0}	Open-Lamp Protection Voltage 0[3]	Striking	0.65	0.70	0.75	V
V_{olp1}	Open-Lamp Protection Voltage 1	Sweep OLP	0.42	0.49	0.56	V
V_{cmpr}	CMP-High Protection Voltage	Sweep CMP	3.4	3.5	3.6	V
V_{hfbp}	High-FB Protection Voltage[3]		3.4	3.5	3.6	V
V_{slp}	Short-Lamp Protection Voltage	Sweep TIMER	0.22	0.30	0.38	V
V_{tmr1}	Timer Threshold Voltage 1	Striking, Sweep TIMER	2.87	3.02	3.17	V
V_{tmr2}	Timer Threshold Voltage 2	Sweep TIMER	1.0	1.1	1.2	V
I_{tmr1}	Timer Current 1	OLP=0V	1.7	2.1	2.5	µA
I_{tmr2}	Timer Current 2	OLR=1.8V	40	50	60	µA
TSD	Thermal Shutdown[3]			150		°C
V_{ovp}	Over-Voltage Protection Voltage	Sweep OLR	1.24	1.34	1.44	V
dcr	ENA2.3V OLP Disable/Enable Change Voltage		2.1	2.3	2.5	V
Output Section						
V_{pdhv}	PMOS Gate High Voltage[3]	V_{IN}=15V		V_{IN}		V
V_{pdlv}	PMOS Gate Low Voltage	V_{IN}=15V	V_{IN}-9.0	V_{IN}-7.5	V_{IN}-6.5	V
V_{ndhv}	NMOS Gate High Voltage	V_{IN}=15V	7.5	8.5	10.0	V
V_{ndlv}	NMOS Gate Low Voltage[3]	V_{IN}=15V		0		V
V_{puv}	PMOS Gate Voltage with UVLO Activated	V_{IN}=4.5V	V_{IN}-0.3			V
V_{nuv}	NMOS Gate Voltage with UVLO Activated	V_{IN}=4.5V			0.3	V
I_{pdsur}	PMOS Gate Drive Source Current[3]	V_{IN}=15V		-300		mA
I_{pdsin}	PMOS Gate Drive Sink Current[3]	V_{IN}=15V		400		mA
I_{ndsur}	NMOS Gate Drive Source Current[3]	V_{IN}=15V		300		mA
I_{ndsin}	NMOS Gate Drive Sink Current[3]	V_{IN}=15V		-400		mA
Maximum / Minimum Duty Cycle						
DC_{MIN}	Minimum Duty Cycle[3]	f_{osc}=100kHz		0		%
DC_{MAX}	Maximum Duty Cycle[3]	f_{osc}=100kHz	45		49	%

Note:

3. These parameters, although guaranteed, are not 100% tested in production.

Typical Performance Characteristics

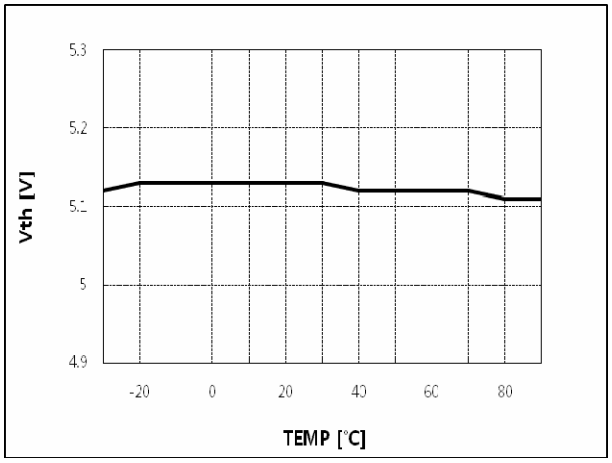

Figure 3. Start Threshold Voltage vs. Temperature

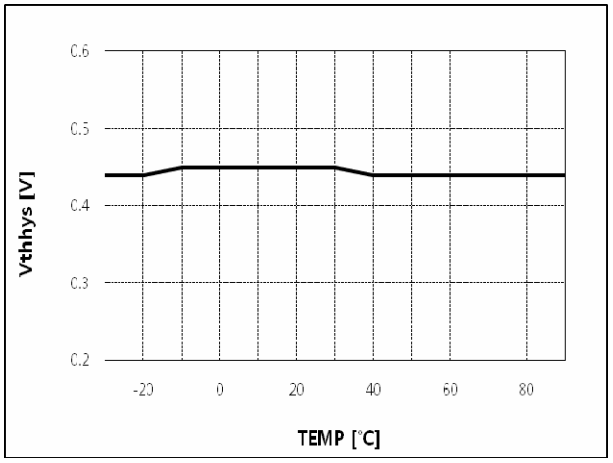

Figure 4. Start Threshold Voltage Hysteresis vs. Temperature

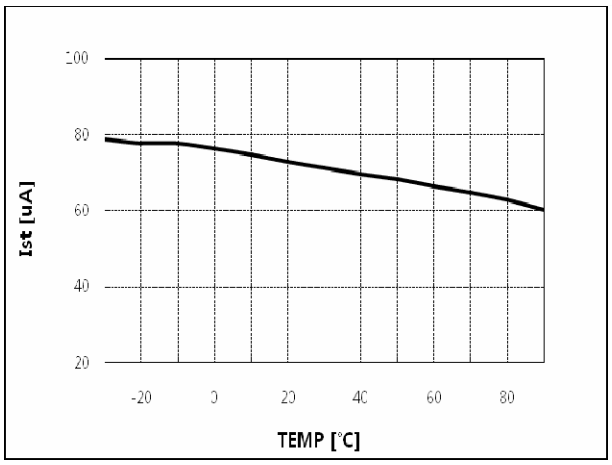

Figure 5. Startup Current vs. Temperature

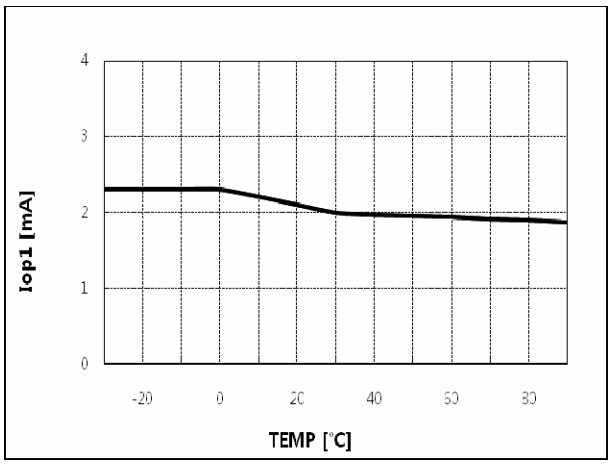

Figure 6. Operating Current vs. Temperature

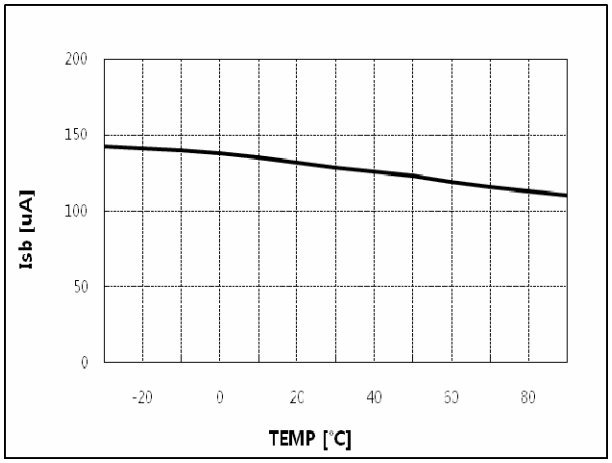

Figure 7. Standby Current vs. Temperature

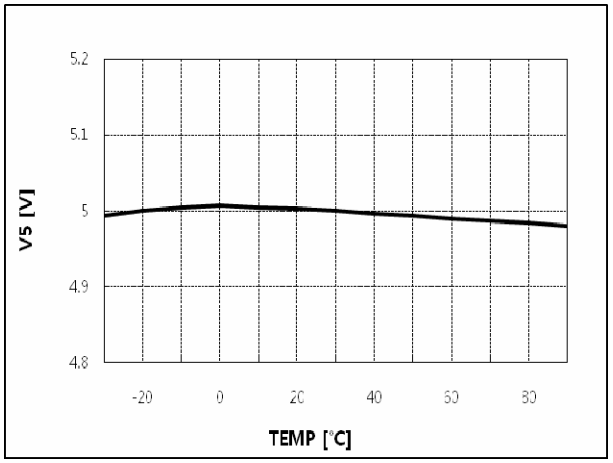

Figure 8. 5V Regulation Voltage vs. Temperature

Typical Performance Characteristics (Continued)

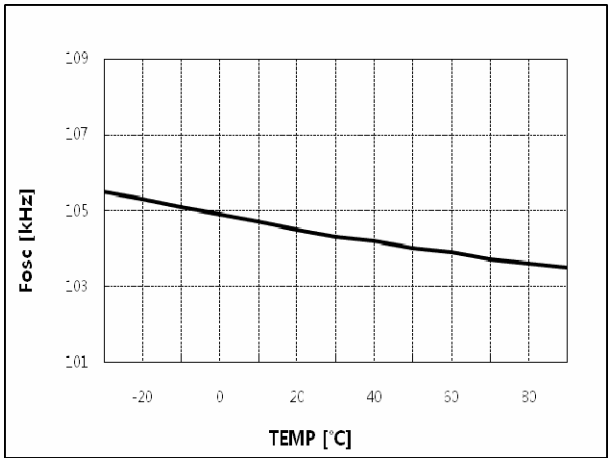

Figure 9. Oscillation Frequency vs. Temperature

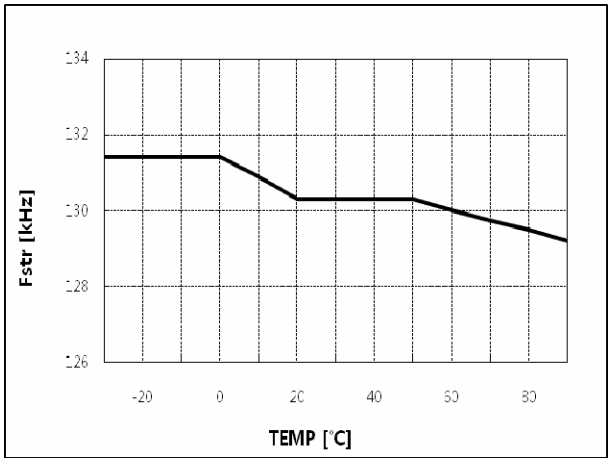

Figure 10. Oscillation Frequency in Striking vs. Temperature

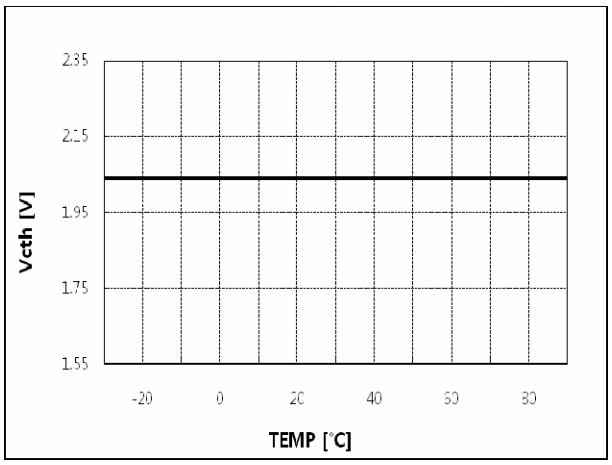

Figure 11. CT High Voltage vs. Temperature

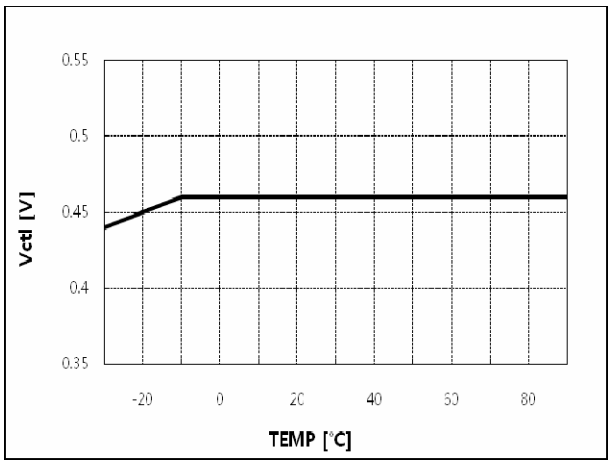

Figure 12. CT Low Voltage vs. Temperature

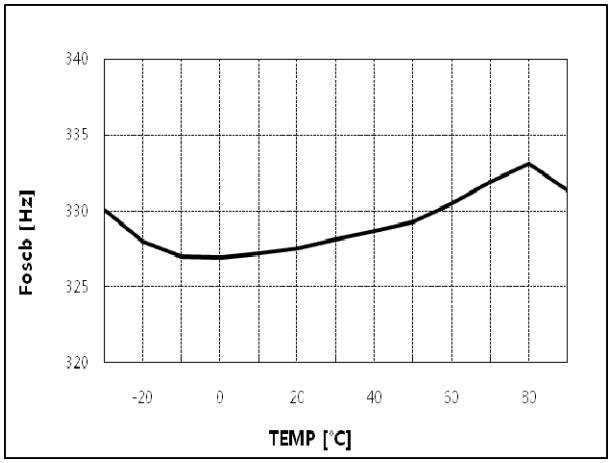

Figure 13. Burst Dimming Frequency vs. Temperature

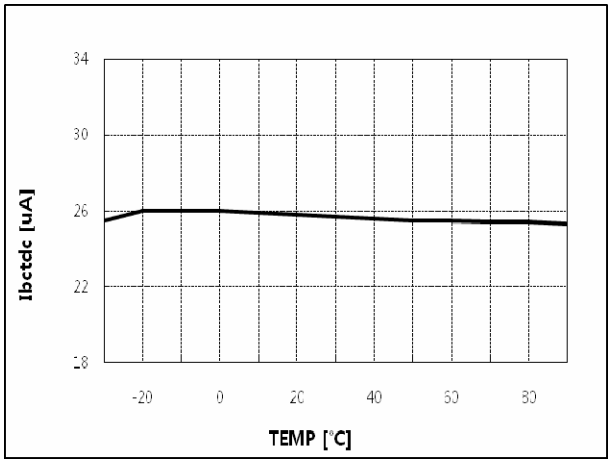

Figure 14. BCT Discharge Current vs. Temperature

Typical Performance Characteristics (Continued)

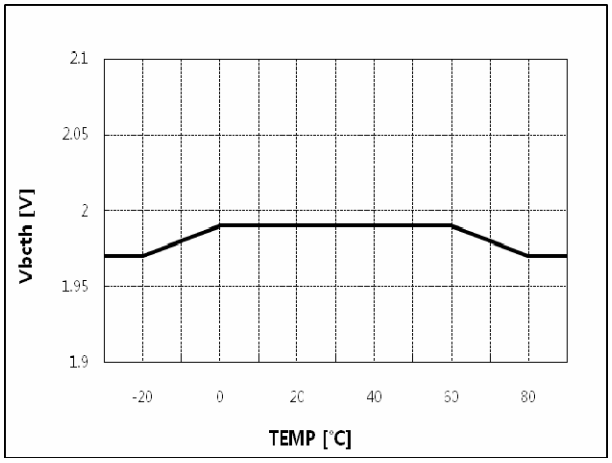

Figure 15. BCT High Voltage vs. Temperature

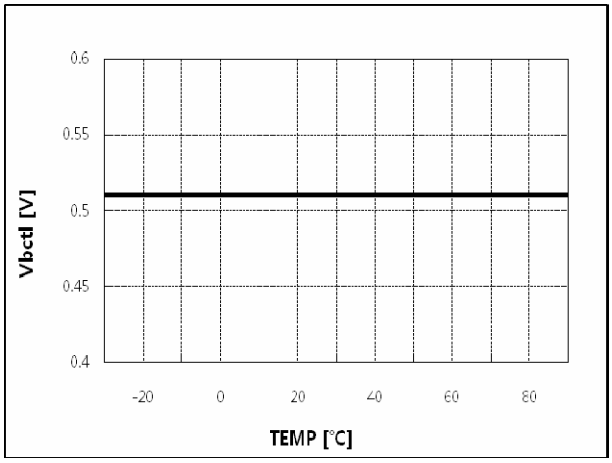

Figure 16. BCT Low Voltage vs. Temperature

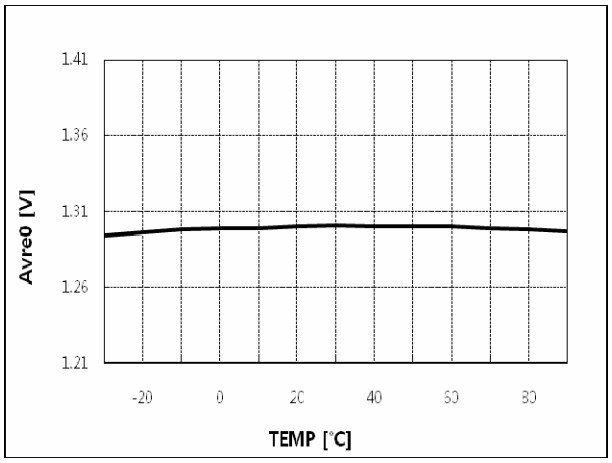

Figure 17. Analog Dimming Reference Voltage 0 vs. Temperature

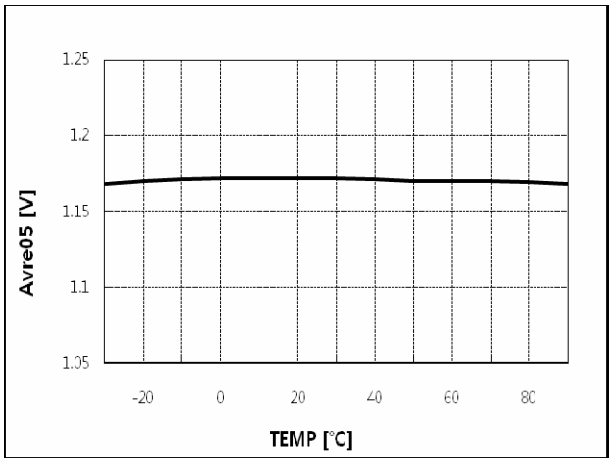

Figure 18. Analog Dimming Reference Voltage 05 vs. Temperature

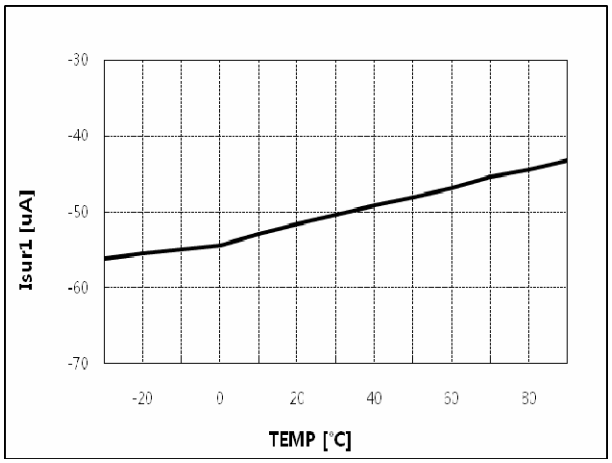

Figure 19. Error Amplifier Source Current 1 vs. Temperature

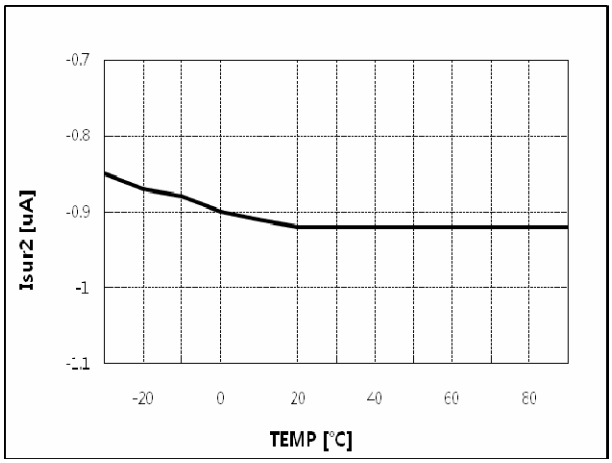

Figure 20. Error Amplifier Source Current 2 vs. Temperature

Typical Performance Characteristics (Continued)

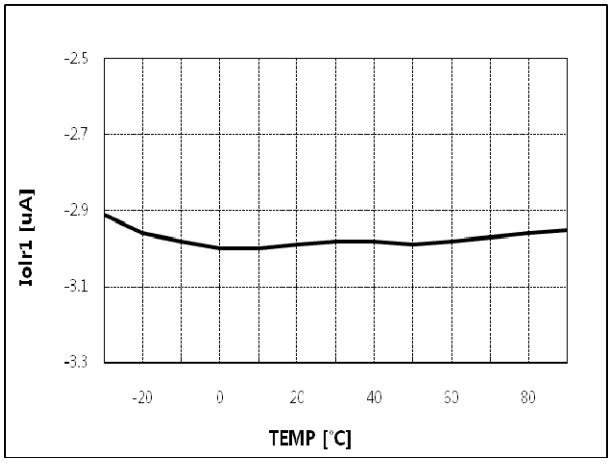

Figure 21. Error Amplifier Source Current for OLR vs. Temperature

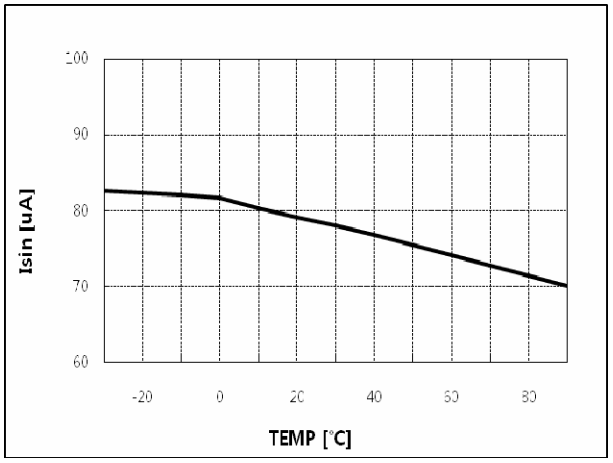

Figure 22. Error Amplifier Sink Current vs. Temperature

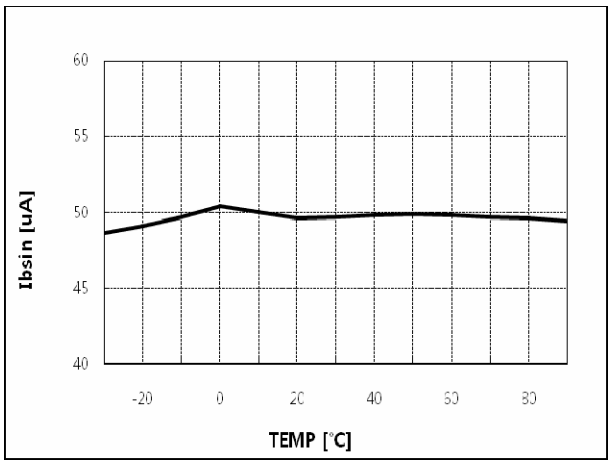

Figure 23. Burst CMP Sink Current vs. Temperature

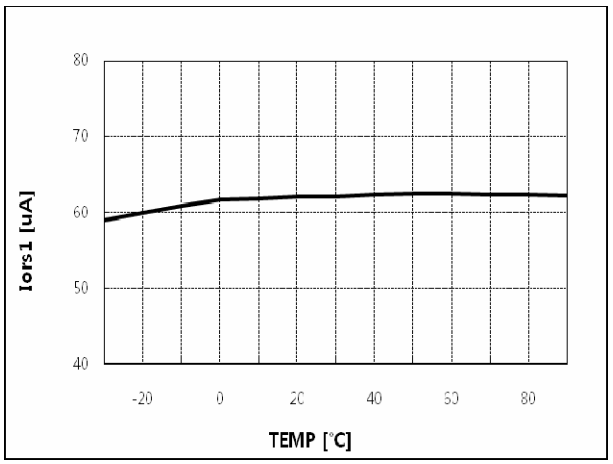

Figure 24. OLR Error Amplifier Sink Current vs. Temperature

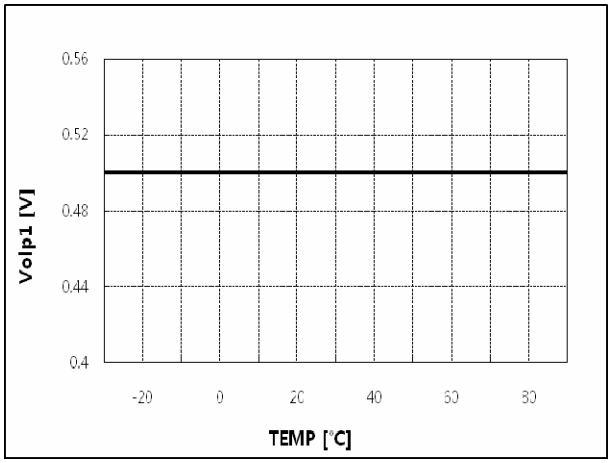

Figure 25. Open-Lamp Protection Voltage 1 vs. Temperature

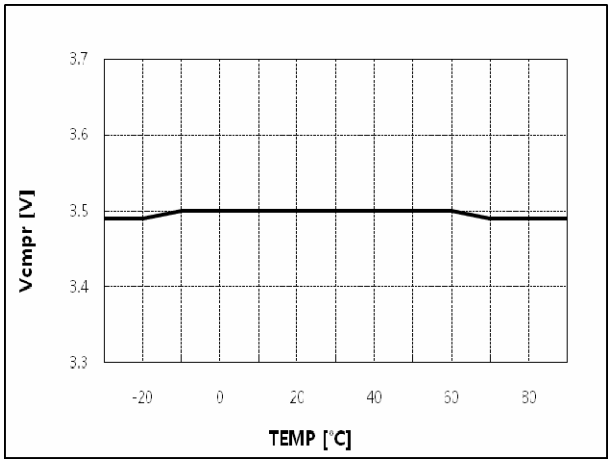

Figure 26. High-CMP Protection Voltage vs. Temperature

Typical Performance Characteristics (Continued)

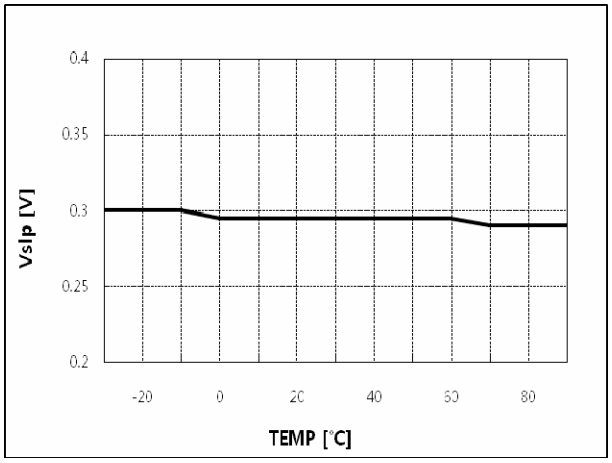

Figure 27. Short-Lamp Protection Voltage vs. Temperature

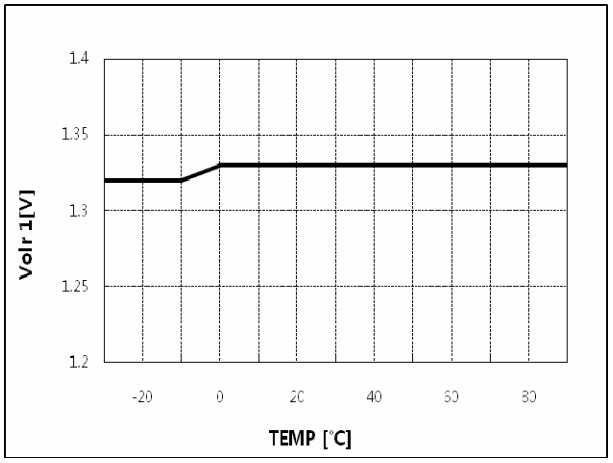

Figure 28. Open Lamp Regulation Voltage 1 vs. Temperature

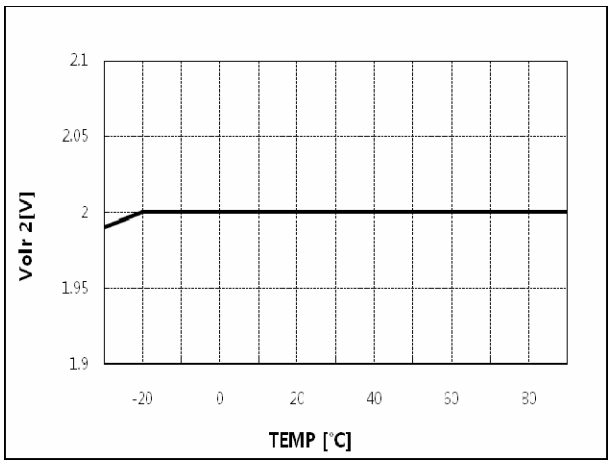

Figure 29. Open Lamp Regulation Voltage 2 vs. Temperature

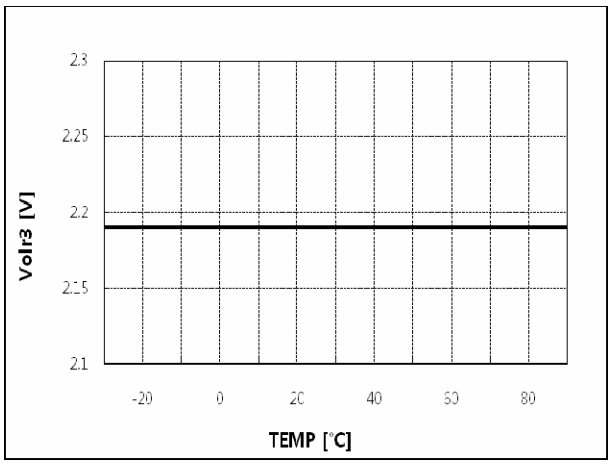

Figure 30. Open Lamp Regulation Voltage 3 vs. Temperature

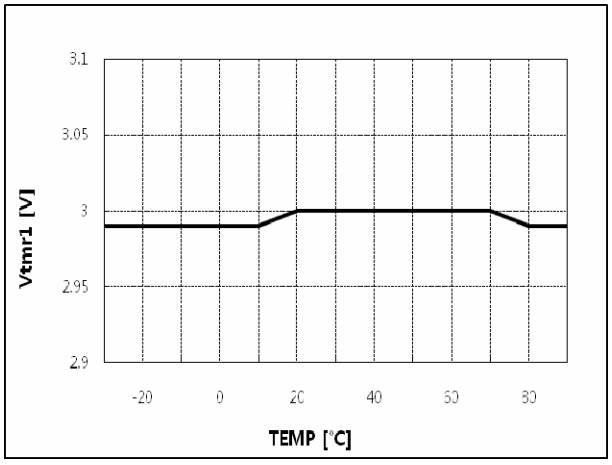

Figure 31. TIMER Threshold Voltage 1 vs. Temperature

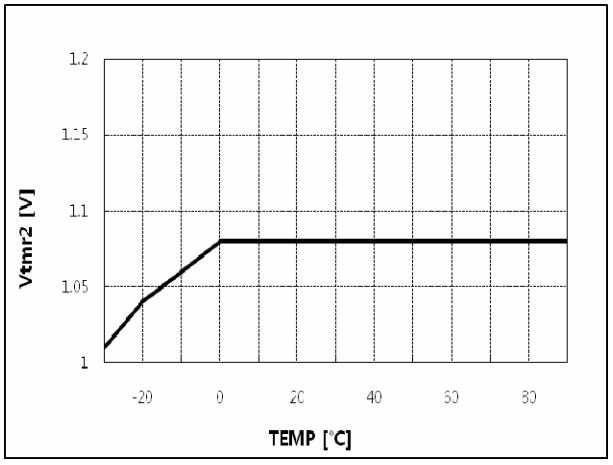

Figure 32. TIMER Threshold Voltage 2 vs. Temperature

Typical Performance Characteristics (Continued)

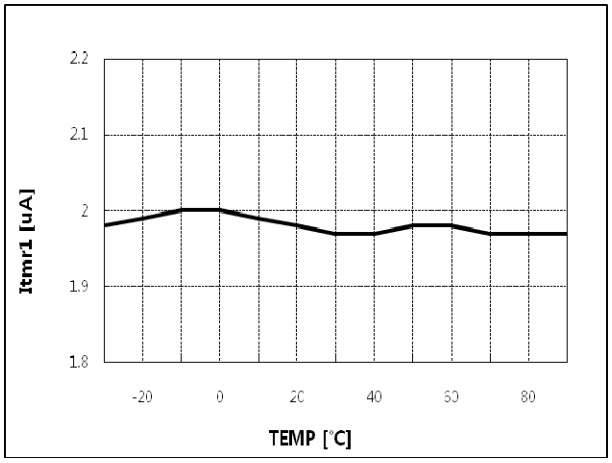

Figure 33. TIMER Current 1 vs. Temperature

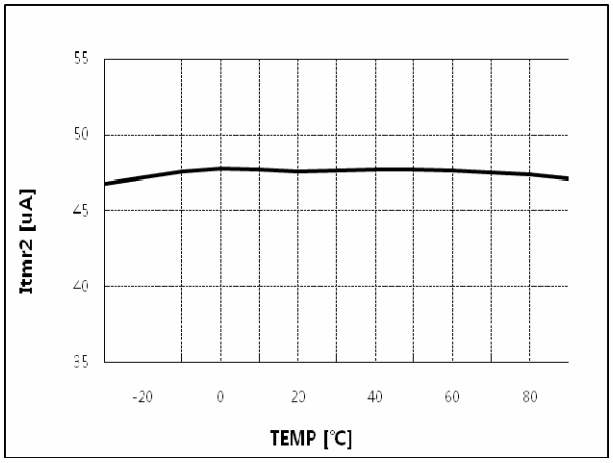

Figure 34. TIMER Current 2 vs. Temperature

Functional Description

UVLO

The under-voltage lockout (UVLO) circuit guarantees stable operation of the IC control circuit by stopping and starting it as a function of the V_{IN} value. The UVLO circuit turns on the control circuit when V_{IN} exceeds 5.2V. When V_{IN} is lower than 4.75V, the IC startup current is less than 100μA.

ENA

Applying voltage higher than 1.4V to the ENA pin enables the IC. Applying voltage lower than 0.7V to the ENA pin disables the IC. In terms of the protections, applying voltage higher than 2.5V to the ENA pin disables OLP and SLP. Applying voltage lower than 2.1V to the ENA pin enables the OLP and the SLP.

Main Oscillator

In normal mode, the external timing capacitor (CT) is charged by the current flowing from the reference voltage source, which is formed by the timing resistor (RT) and the timing capacitor (CT). The sawtooth waveform charges up to 2V. Once CT voltage reaches 2V, the CT begins discharging down to 0.4V. Next, the CT starts charging again and a new switching cycle begins, as shown in Figure 35. The main frequency is programmed by adjusting the RT and CT value. The main frequency is calculated as:

$$f_{OSC} = \frac{1}{RT \cdot CT \cdot \ln\left(\frac{3.9585 \cdot RT - 13650}{2.61 \cdot RT - 13650}\right)} [Hz] \quad (1)$$

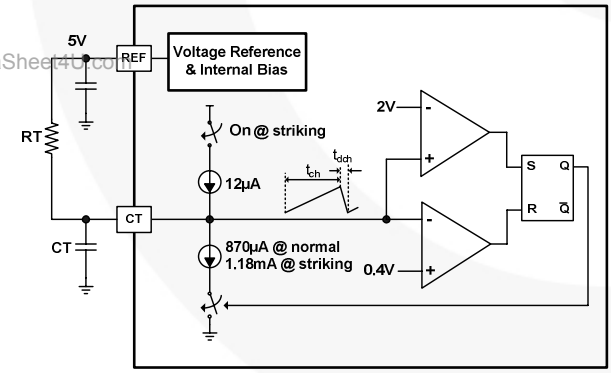

Figure 35. Main Oscillator Circuit

In striking mode, the external timing capacitor (CT) is charged by the current flowing from the reference voltage source and 12μA current source, which increases the frequency. If the product of RT and CT value is constant, the striking frequency depends on CT and is calculated as:

$$f_{str} = \frac{1}{RT \cdot CT \cdot \ln\left(\frac{13.65 + (3I_1 - 4.55I_2)RT}{13.65 + (4.55I_1 - 3I_2)RT} \cdot \frac{-I_1 \cdot I_2 \cdot RT^2}{-I_1 \cdot I_2 \cdot RT^2}\right)} [Hz] \quad (2)$$

$$\because I_1 = 12 \times 10^{-6} A,\ I_2 = 1.128 \times 10^{-3} A$$

Burst Dimming Oscillator

The burst dimming timing capacitor (BCT) is charged by the current flowing from the reference voltage source, which is formed by the burst dimming timing resistor (BRT) and the burst dimming timing capacitor (BCT). The sawtooth waveform charges up to 2V. Once the BCT voltage reaches 2V, the capacitor begins discharging down to 0.5V. Next, the BCT starts charging again and a new burst dimming cycle begins, as shown in Figure 36. The burst dimming frequency is programmed by adjusting the BCT and BRT values. The burst dimming frequency is calculated as:

$$f_{OSCB} = \frac{1}{BRT \cdot BCT \cdot \ln\left(\frac{0.039 \cdot BRT - 4500}{0.026 \cdot BRT - 4500}\right)} [Hz] \quad (3)$$

To avoid visible flicker, the burst dimming frequency should be greater than 120Hz.

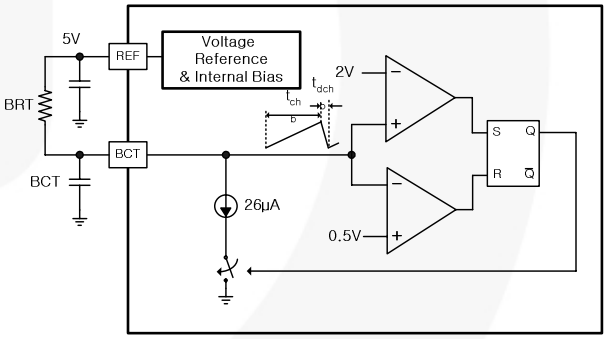

Figure 36. Burst Dimming Oscillator Circuit

Analog Dimming

For analog dimming, the lamp intensity is controlled with the external dimming signal (V_{ADIM}) and resistors. Figure 37 shows how to implement an analog dimming circuit.

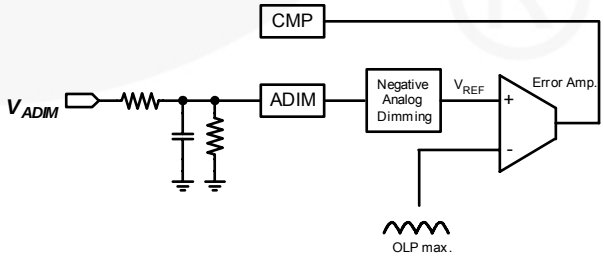

Figure 37. Analog Implementation Circuit

In full brightness, the maximum rms value of the lamp current is calculated as:

$$i_{rms}^{max} = V_{ref\_max} \frac{\pi}{2\sqrt{2}R_{S1}}[A] \quad (4)$$

The lamp intensity is inversely proportional to V_{ADIM}. As V_{ADIM} increases, the lamp intensity decreases and the rms value of the lamp current is calculated as:

$$i_{rms}^{max} = V_{ref} \frac{\pi}{2\sqrt{2}R_s}[A] \quad (5)$$
$$V_{ref} = V_{ref\_max} - 0.30V_{ADIM}[A]$$

Figure 38 shows the lamp current waveform vs. V_{ADIM} in an analog dimming mode.

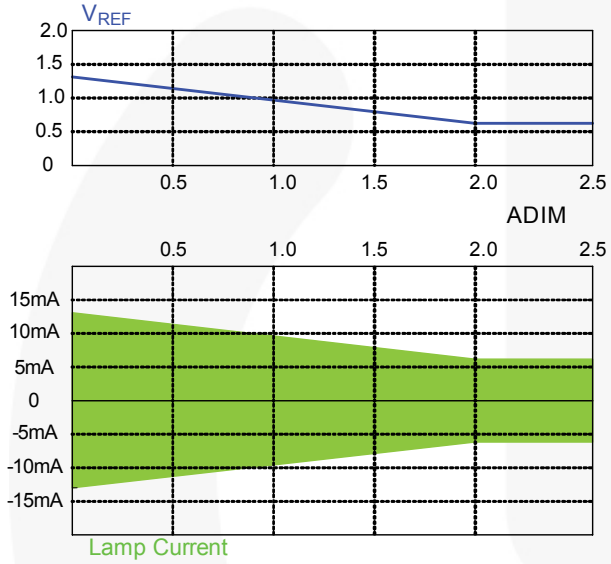

Figure 38. Analog Dimming Waveforms

Burst Dimming

Lamp intensity is controlled with the BDIM signal over a wide range. FAN7318B provides polarity selection. When BDIM is inputted, DC voltage or PWM pulse signal and BCT sets the sawtooth waveform or DC voltage, respectively. This structure can be implemented as negative dimming polarity. When BDIM voltage is lower than BCT voltage, the lamp current is turned on; 0V on BDIM commands full brightness. The duty cycle of the PWM pulse determines the lamp brightness. The lamp intensity is inversely proportional to BDIM voltage. As BDIM voltage increases, the lamp intensity decreases. Figure 39 shows the lamp current waveform vs. DIM in negative burst dimming mode.

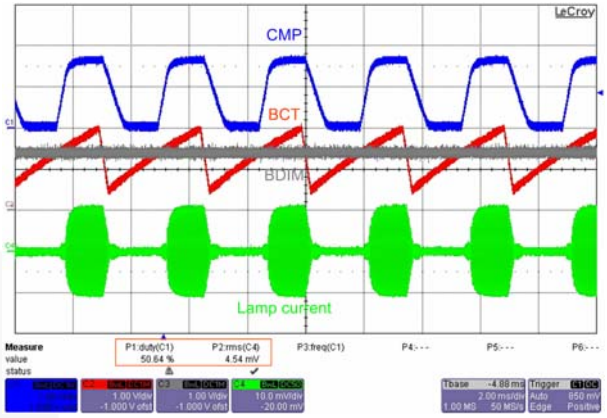

Figure 39. Negative Burst Dimming Waveform Using DC Voltage

Burst dimming can be implemented, not only with DC voltage, but also using PWM pulse as the BDIM signal. Figure 40 shows how to implement burst dimming using PWM pulse as BDIM signal.

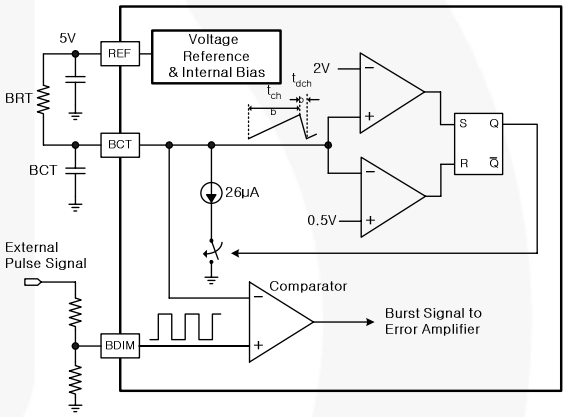

Figure 40. Negative Burst Dimming Implementation Circuit Using an External Pulse

Figure 41 shows the lamp current waveform vs. an external pulse in negative burst dimming mode.

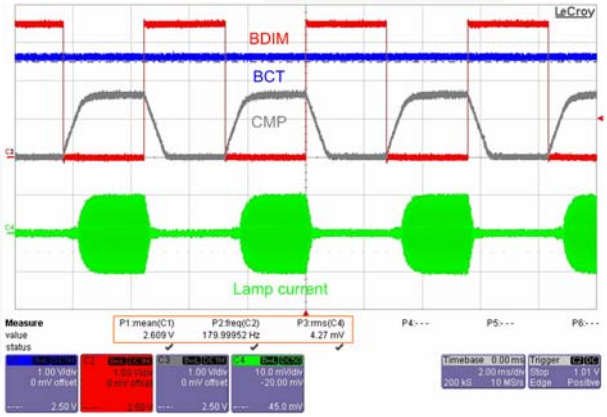

Figure 41. Negative Burst Dimming Waveform Using an External Pulse

During striking mode, burst dimming operation is disabled to guarantee continuous striking time. Figure 42 shows burst dimming disabled during striking mode.

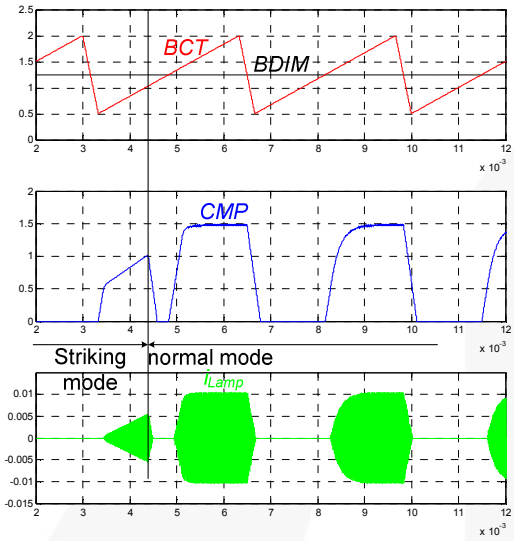

Figure 42. Burst Dimming During Striking Mode

When BDIM is setting over 2.2V_{DC} and BCT is inputted PWM pulse signal, positive dimming polarity can be implemented. Figure 43 shows how to implement burst dimming using PWM pulse as the BDIM signal.

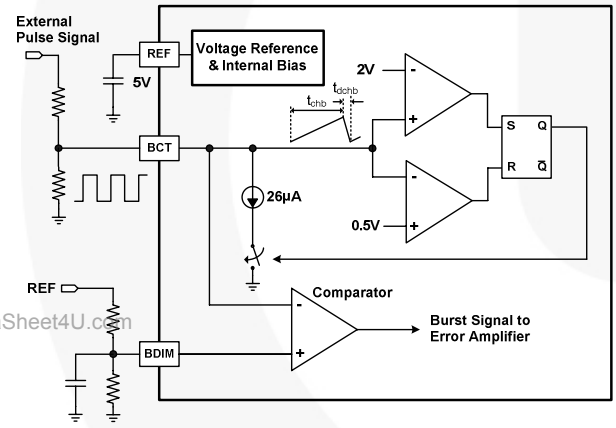

Figure 43. Positive Burst Dimming Implementation Circuit Using an External Pulse

Figure 44 shows the lamp current waveform vs. an external pulse in positive burst dimming mode.

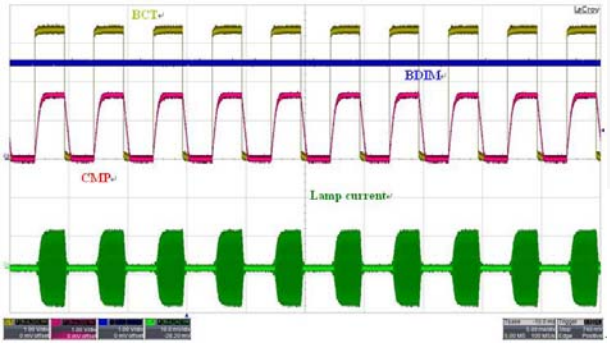

Figure 44. Positive Burst Dimming Waveform Using an External Pulse

Soft-Start

A soft-start circuit ensures a gradual increase in the input and output power. FAN7318B has no soft-start pin, but provides soft-start function using the first BCT waveform. The first BCT waveform limits CMP voltage at initial operation, so lamp current increases gradually, as shown in Figure 45 and Figure 46

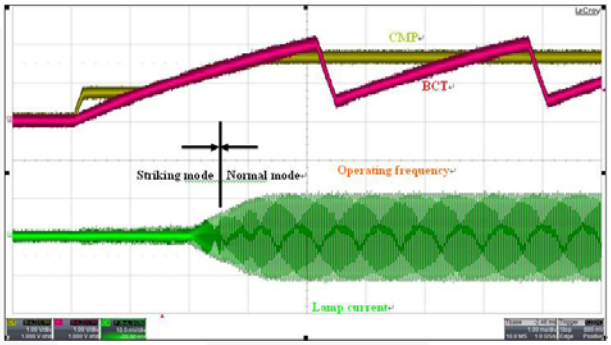

Figure 45. Soft-Start in Normal Mode

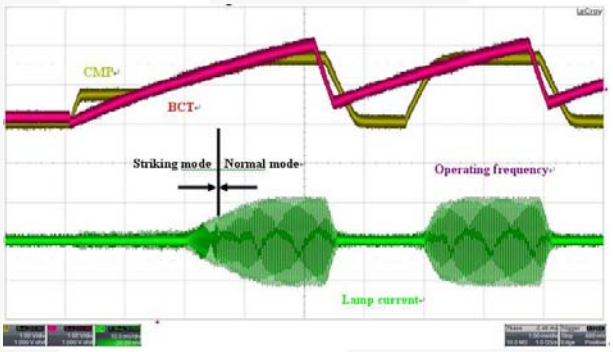

Figure 46. Soft-Start in Burst Dimming Mode

Output Drives

FAN7318B is designed to drive P-N half-bridge MOSFETs with symmetric duty cycle. FAN7318B can drive P-MOSFET directly without a level-shift capacitor and a Zener diode. A fixed dead time of 500ns is introduced between two outputs at maximum duty cycle, as shown in Figure 47.

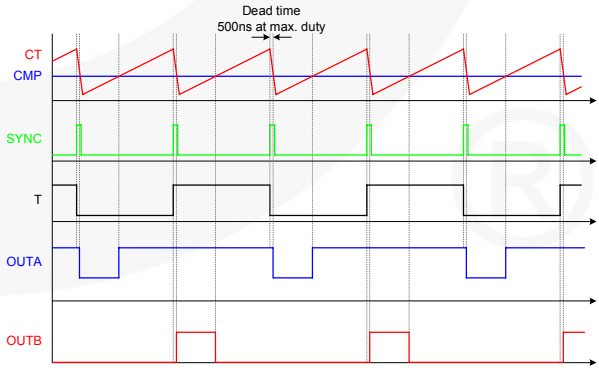

Figure 47. MOSFETs Gate Drive Signal

Lamp Current Feedback Circuit

FAN7318B has four OLP pins for lamp current feedback and protections. The inputs of four OLP pins are connected to the internal half-wave and full-wave rectifier circuits. The half-wave rectified signals of four OLP inputs are connected to the maximum detector circuit. The full-wave rectified signals of four OLP inputs are connected to the minimum detector circuit.

Two inputs of the four OLP pins should be inverse phase with the other two inputs.

Lamp Voltage Feedback Circuit

FAN7318B has four OLR pins for lamp voltage feedback and protections. The inputs of four OLR pins are connected to the internal full-wave rectifier circuit. The full-wave rectified signals of the four OLR inputs are connected to the maximum detector circuit. Furthermore, they are connected to the minimum detector circuit for protections.

Protections

The FAN7318B provides the following latch-mode protections: Open-Lamp Regulation (OLR), Open-Lamp Protection (OLP), Short-Lamp Protection (SLP), CMP-High Protection and Thermal Shutdown (TSD). The latch is reset when V_{IN} falls to the UVLO voltage or ENA is pulled down to GND.

The protection delay time can be adjusted by a capacitor between the TIMER pin and GND.

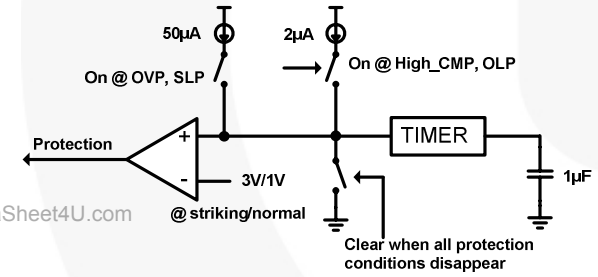

Figure 48. Protection Timing Delay

Assume that the TIMER pin capacitor is 1μF.

The striking time is calculated as:

$$t_{strike} = \frac{C\Delta V_{str}}{I_{sur1}} = \frac{1\mu F \bullet 3V}{2\mu A} = 1.5s \quad (6)$$

The OVP and SLP delay time are calculated as:

$$t_{OVP\_SLP} = \frac{C\Delta V_{nor}}{I_{sur2}} = \frac{1\mu F \bullet 1V}{50\mu A} = 20ms \quad (7)$$

The CMP high protection and OLP delay time are calculated as:

$$t_{OLP\_CMPH} = \frac{C\Delta V_{nor}}{I_{sur1}} = \frac{1\mu F \bullet 1V}{2\mu A} = 500ms \quad (8)$$

Open-Lamp Regulation

When the maximum of the rectified OLR input voltages (V_{OLR}^{max}) is more than 2V, the IC enters regulation mode and controls CMP voltage. The IC limits the lamp voltage by decreasing CMP source current. If V_{OLR}^{max} is between 1.34V and 2V, CMP source current decreases to 3.0μA. Then, if V_{OLR}^{max} reaches 2V, CMP source current decreases to 0μA, so the CMP voltage remains constant and the lamp voltage also remains constant, as shown in Figure 49.

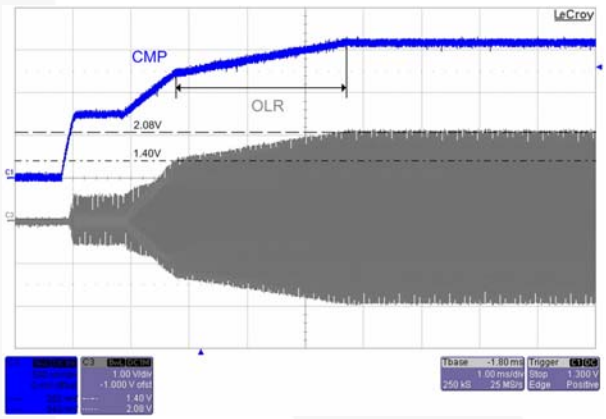

Figure 49. Open-Lamp Regulation in Striking Mode

Finally, if V_{OLR}^{max} is more than 2.2V, the error amplifier for OLR is operating and CMP sink current increases, so CMP voltage decreases and the lamp voltage maintains the determined value, as shown in Figure 50.

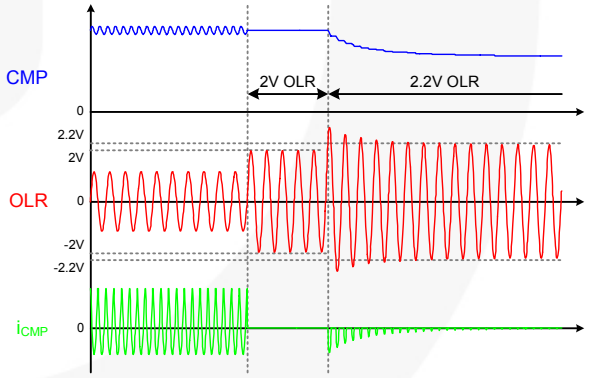

Figure 50. 2.2V Open-Lamp Regulation

Over-Voltage Protection

In normal mode, while V_{OLR}^{max} is higher than 1.34V, the TIMER pin capacitor is charged by an internal current source of 50μA. Once the TIMER reaches 1V, the IC enters shutdown, as shown in Figure 51. This protection is disabled in striking mode to ignite lamps reliably.

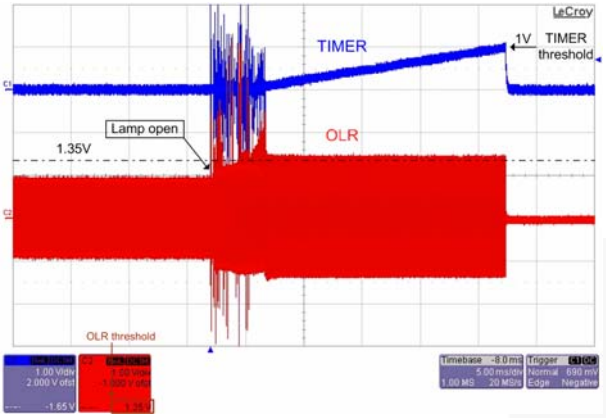

Figure 51. Over-Voltage Protection in Normal Mode

In burst dimming mode, while V_{OLR}^{max} is higher than 1.34V, burst dimming is disabled, so that the TIMER pin capacitor is charged continuously by an internal current source of 50μA. Once the TIMER reaches 1V, the IC enters shutdown, as shown in Figure 52.

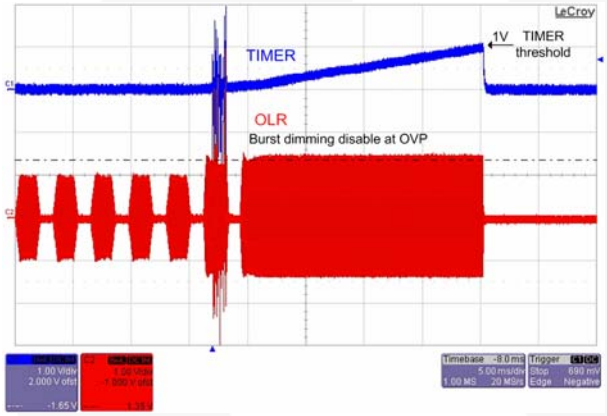

Figure 52. Over-Voltage Protection in Burst Dimming Mode

Open-Lamp Protection

If the minimum of the rectified OLP voltages (V_{OLP}^{min}) is less than 0.7V during initial operation, the IC operates in striking mode for a time predetermined by the TIMER pin capacitor and an internal current source, 2μA, as shown in Figure 53.

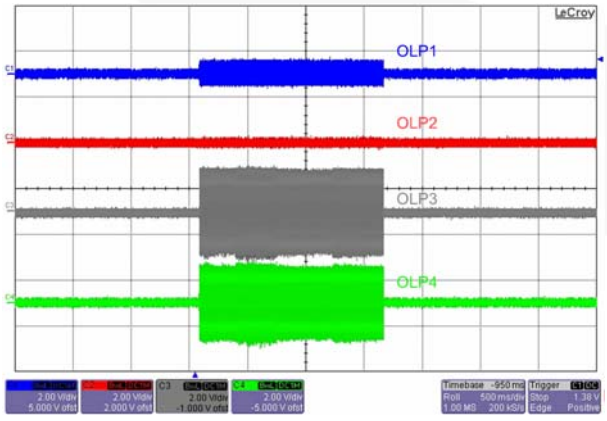

Figure 53. Open-Lamp Protection in Striking Mode

The IC starts operating in striking mode and remains in striking mode until 17 pulses of V_{OLP}^{min} higher than 0.7V and OLR < 1.34V occur. If more than 17 pulses and OLR < 1.34V, the IC changes from striking mode into normal mode, as shown in Figure 54.

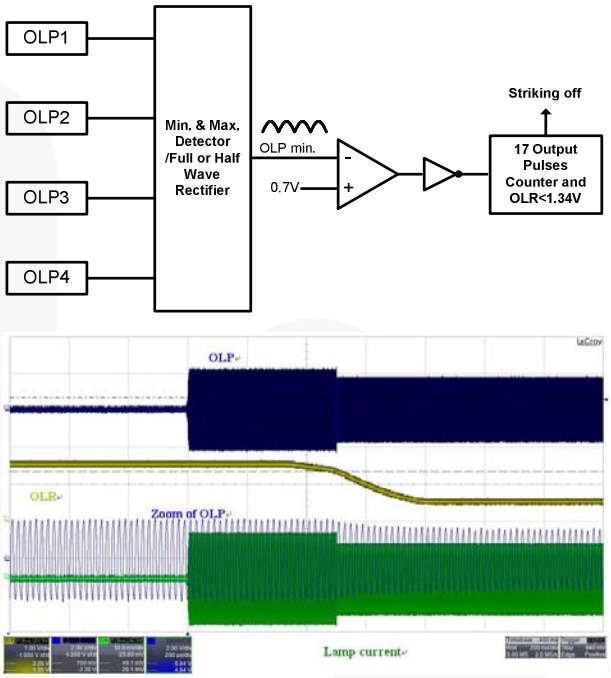

Figure 54. Mode Change from Striking to Normal

After ignition, if V_{OLP}^{min} is less than 0.5V for a time predetermined by the TIMER pin capacitor and an internal current source, 2μA in normal mode, the IC is shut down, as shown in Figure 55 and Figure 56.

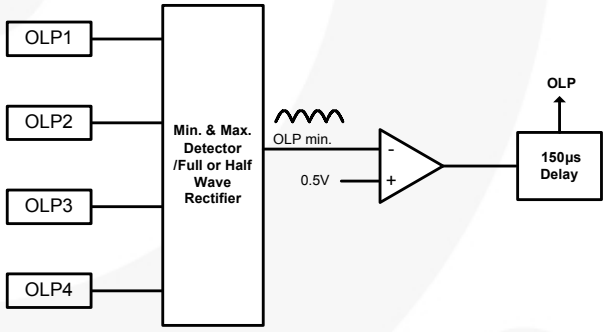

Figure 55. OLP in Normal Mode (Configuration)

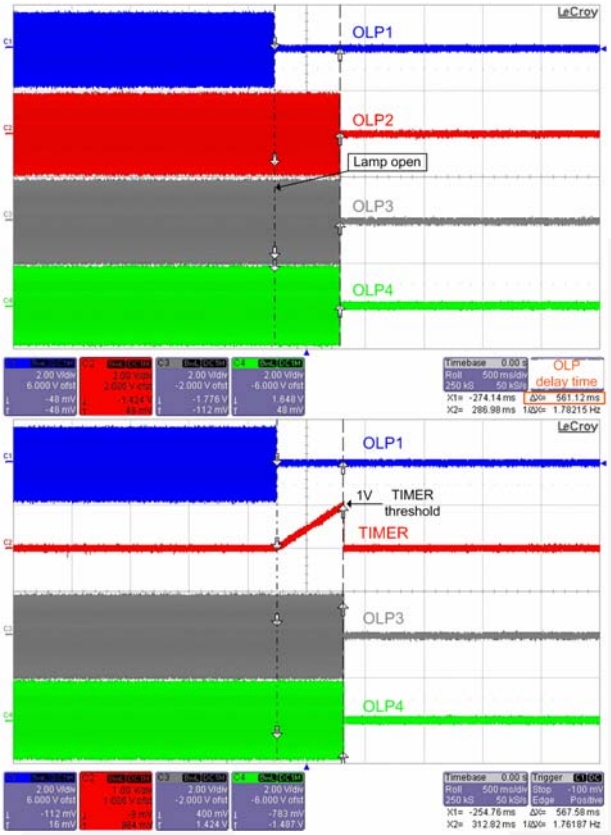

Figure 56. OLP in Normal Mode

In burst dimming mode, if V_{OLP}^{min} is less than 0.5V for another time predetermined by the TIMER pin capacitor and an internal current source, 2μA; the IC is shut down, as shown in Figure 57. The open-lamp protection delay in burst dimming mode is shorter than in full brightness because a short-lamp condition is detected at rising interval of lamp voltage in burst dimming, then another internal current source is turned on during the interval.

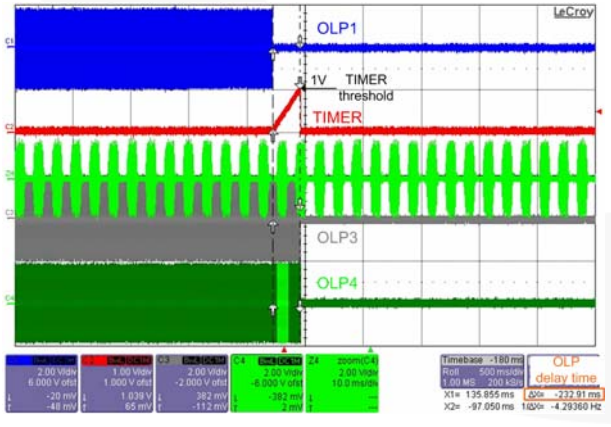

Figure 57. OLP in Burst Dimming Mode

Applying voltage lower than 2.1V to the ENA pin enables OLP. Applying voltage higher than 2.5V to the ENA pin disables OLP and is called as DCR mode. Regardless of DCR mode, OLP is enabled in striking mode.

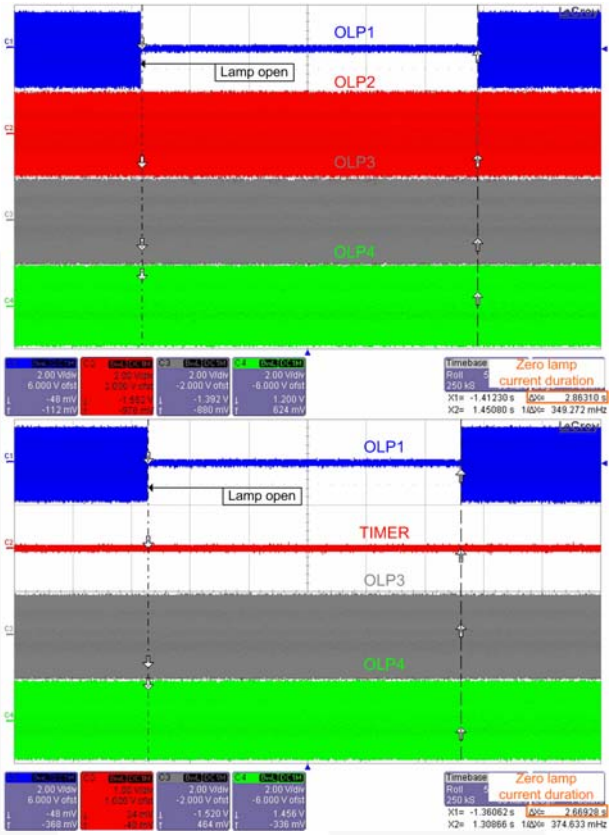

Figure 58. OLP Disable in DCR Mode

Short-Lamp Protection

If the minimum of the rectified OLR voltages (V_{OLR}^{min}) is less than 0.3V for a time predetermined by the TIMER pin capacitor and a internal current source of 50μA in normal mode, the IC is shut down, as shown in Figure 59. This protection is disabled in striking mode to ignite lamps reliably.

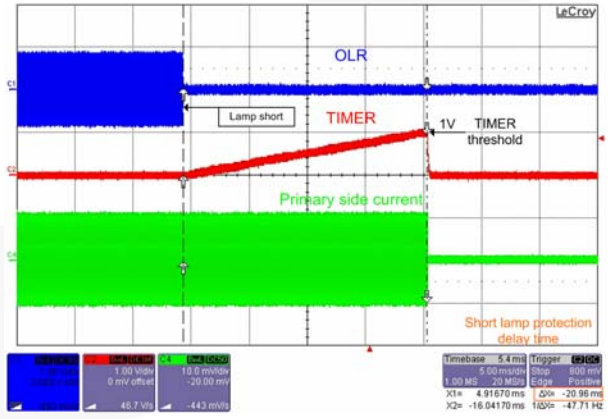

Figure 59. Short-Lamp Protection in Normal Mode

In burst dimming mode, if V_{OLR}^{min} is less than 0.3V for a time predetermined by the TIMER pin capacitor and a internal current source of 50μA turned on only burst dimming on time, the IC is shut down, as shown in Figure 60. SLP protection delay changes, depending on burst dimming on duty ratio.

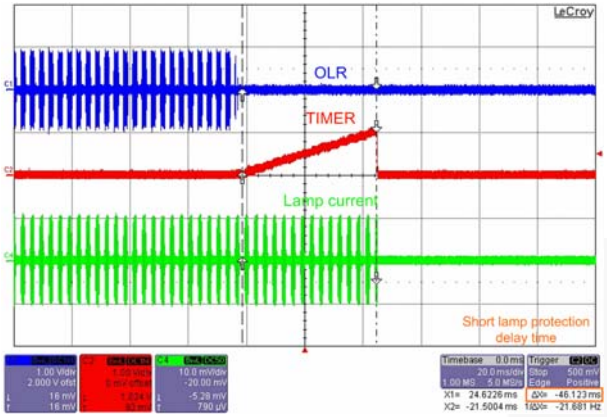

Figure 60. SLP in Burst Dimming Mode

Applying voltage higher than 2.5V to the ENA pin disables SLP. Applying voltage lower than 2.1V to the ENA pin enables SLP.

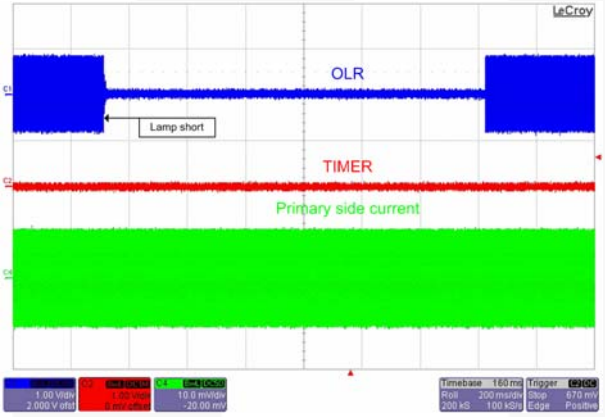

Figure 61. Short-Lamp Protection Disable in DCR Mode

CMP-High Protection

If CMP is more than 3.5V for a time predetermined by the TIMER pin capacitor and a internal current source of 50μA in normal mode, the IC is shut down, as shown in Figure 62.

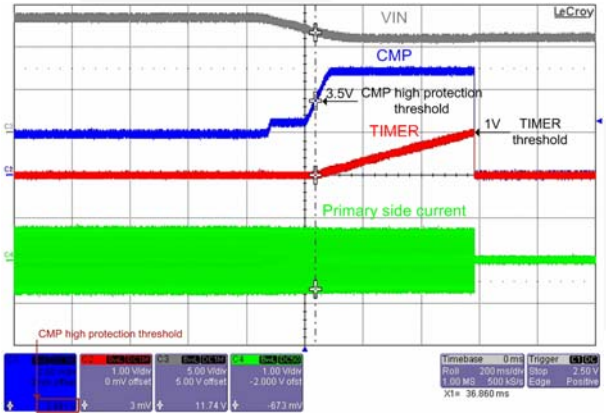

Figure 62. CMP-High Protection

This protection is disabled by a pull-down resistor (a few MΩ) between CMP and GND. If CMP voltage reaches 2.5V, CMP source current decreases to 2μA. Determine a pull-down resistor value such that the whole of this current can flow through the resistor. If so, CMP-high protection can be disabled, as shown Figure 63. This protection is disabled in striking mode to ignite the lamps reliably.

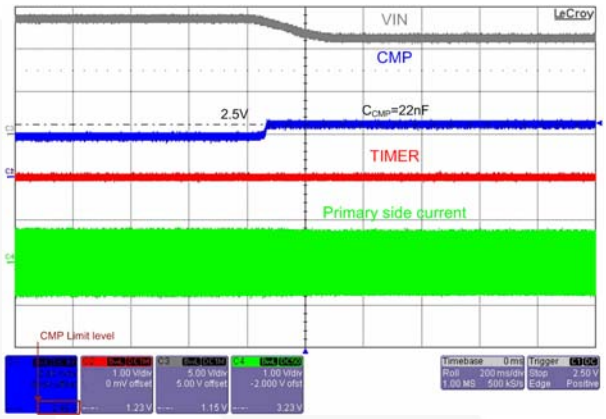

Figure 63. CMP-High Protection Disable by a Pull-Down Resistor

Thermal Shutdown

The IC provides the function to detect abnormal over-temperature. If the IC temperature exceeds approximately 150°C, the thermal shutdown triggers.

Typical Application Circuit (LCD Backlight Inverter)

Application	Device	Input Voltage Range	Number of Lamps
22-Inch LCD Monitor	FAN7318B	15V±10%	4

1. Features

- High-Efficiency, Single-Stage Power Conversion
- P-N Half-Bridge Topology
- Reduces Required External Components
- Enhanced System Reliability through Protection Functions

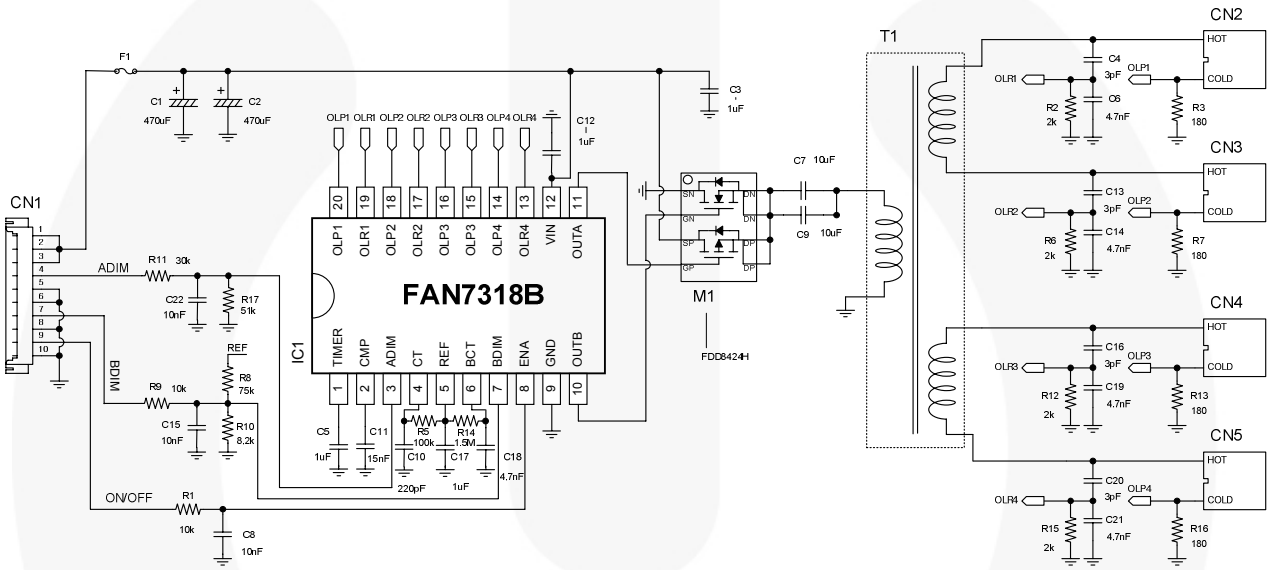

Figure 64. Typical Application Circuit

Physical Dimensions

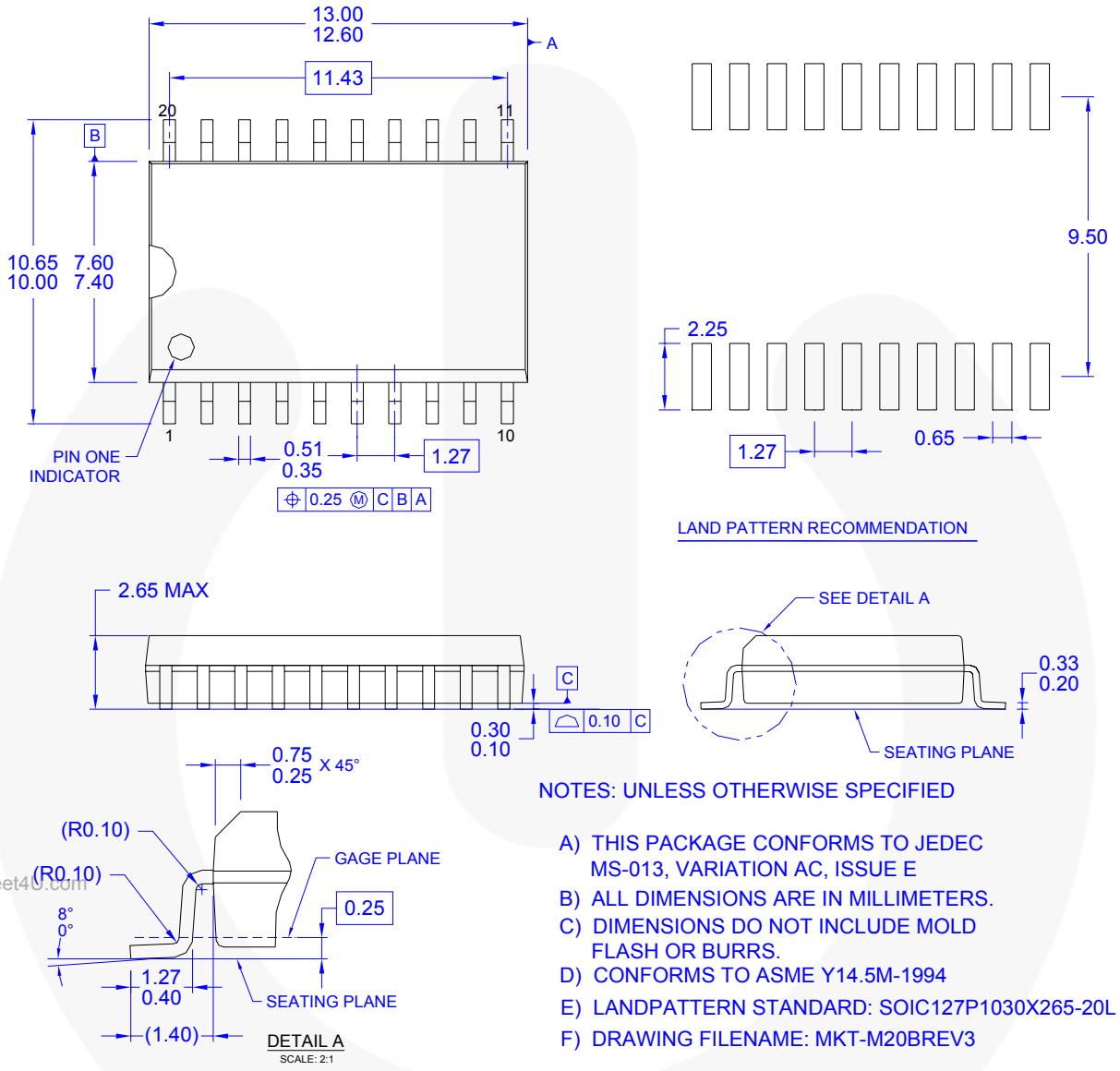

Figure 65. 20-Lead, Small Outline Integrated Circuit (SOIC) Package

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